IEICE TRANS. FUNDAMENTALS, VOL.E92–A, NO.4 APRIL 2009

PAPER Special Section on Advanced Technologies Emerging Mainly from the 21st Workshop on Circuits and Systems in Karuizawa

EMI Reduction by Spread-Spectrum Clocking in Digitally-Controlled DC-DC Converters

Ibuki MORI[†], Yoshihisa YAMADA[†], Santhos A. WIBOWO[†], *Nonmembers*, Masashi KONO[†], Haruo KOBAYASHI[†a)], *Members*, Yukihiro FUJIMURA[†], *Nonmember*, Nobukazu TAKAI[†], *Member*, Toshio SUGIYAMA[††], Isao FUKAI[††], Norihisa ONISHI[††], Ichiro TAKEDA[††], *and* Jun-ichi MATSUDA[††], *Nonmembers*

SUMMARY This paper proposes spread-spectrum clock modulation algorithms for EMI reduction in digitally-controlled DC-DC converters. In switching regulators using PWM, switching noise and harmonic noise concentrated in a narrow spectrum around the switching frequency can cause severe EMI. Spread-spectrum clock modulation can be used to minimize EMI. In conventional switching regulators using analog control it is very difficult to realize complex spread-spectrum clocking, however this paper shows that it is relatively easy to implement spread-spectrum EMI-reduction using digital control. The proposed algorithm was verified using a power converter simulator (SCAT).
key words: *PWM control, spread-spectrum clock modulation, EMI, digitally-controlled DC-DC converter*

1. Introduction

Most portable electronic devices have low-voltage high-current power supplies using high-efficiency switching regulators. However, the considerable switching noise (and EMI) that switching regulators produce is a big demerit. EMI-related regulations are becoming more severe [1]. Regulations prescribe limits on the generation of Electromagnetic Interference (EMI) and also noise-tolerance or Electromagnetic Susceptibility (EMS) requirements; the combination of both EMI and EMS is called EMC (Electromagnetic Compatibility). In many countries it is illegal to sell electrical and electronic devices that do not comply with local EMC standards (in many cases devices must be type-approved, or tested and certified as complying). In most conventional switching regulators, shielding and filtering are used to reduce EMI. While shielding and filtering are effective ways of reducing noise, penalties associated with this approach include the cost of transformers and coils and the size/weight of shielding.

We considered, as an alternative to extensive shielding and filtering, how to reduce EMI by switching regulator control-module design changes. After examining the possible application of digital control systems with spread-spectrum technology [2]–[5] to analog-controlled switching regulators [6]–[10], we considered two modulation algorithms that can only be realized using digitally-controlled switching regulators. With digitally-controlled switching regulators it is easier to change the control system design, and to introduce new control system topologies, than with analog-controlled switching regulators. In addition, complex modulation methods can be easily realized using a DSP device in the control section of a digitally-controlled switching regulator.

We also developed a technique for using SCAT (a high-speed Switching Converter Analysis Tool) [11], to simulate digitally-controlled switching regulators, and used this to confirm the EMI-reduction effects of the proposed algorithms.

Conventional spread-spectrum clock modulation methods are described in Sect. 2. The proposed spread-spectrum clock modulation methods are described in Sect. 3, and results of circuit simulations are explained in Sect. 4. Conclusions and proposed future work are described in Sect. 5.

2. Conventional Spread-Spectrum Clock Modulation Methods

Pulse Width Modulation (PWM) is the main method of clock modulation used for switching regulators.

Figures 1–4 show pseudo-random clocking schemes used for spreading the noise spectrum in power electron-

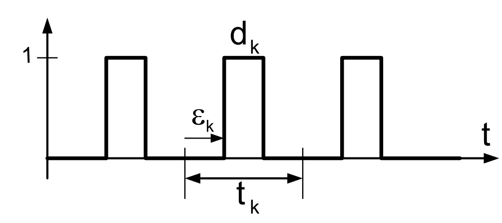


Fig. 1 Modulated clock waveform $q(t)$ for spectrum spreading.

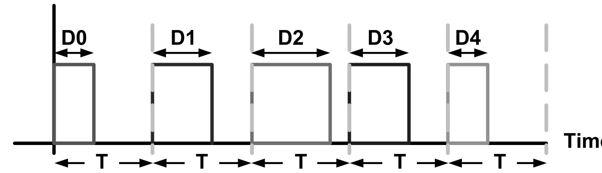


Fig. 2 Clock with PWM modulation.

Manuscript received June 17, 2008.
Manuscript revised October 30, 2008.
[†]The authors are with the Department of Electronic Engineering, Graduate School of Engineering, Gunma University, Kiryu-shi, 376-8515 Japan.
[††]The authors are with Toko, Inc., Tsurugashima-shi, 350-2281 Japan.
a) E-mail: k_haruo@el.gunma-u.ac.jp
DOI: 10.1587/transfun.E92.A.1004

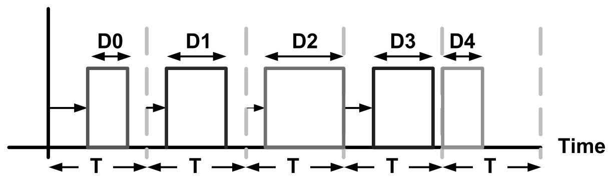


Fig. 3 Clock with PPM modulation.

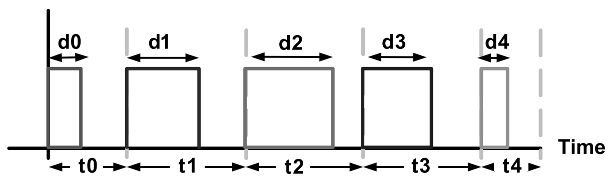


Fig. 4 Clock with ASM modulation.

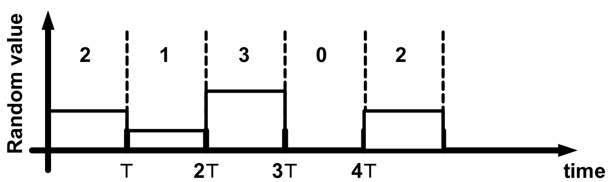


Fig. 5 Movement of pseudo-random values that are used in PPM modulation method.

ics; these clocking schemes modify the PWM by dithering t_k (clock period), d_k (duty ratio) or ϵ_k (clock rising-edge timing) [8]:

- For randomized Pulse Position Modulation (PPM): ϵ_k changes, while t_k and d_k are fixed.
- For Asynchronous Modulation (ASM): t_k changes while d_k is fixed and $\epsilon_k = 0$.
- For randomized PWM: d_k changes while t_k and ϵ_k are fixed.
- For Simplified ASM: t_k changes while d_k is fixed and $\epsilon_k = 0$.

Randomized PPM and Asynchronous Modulation (ASM) are often used for spread-spectrum modulation in DC-DC converters because the duty ratio d_k is kept the same as for conventional PWM [6]–[10]. PWM (shown in Fig. 2) uses a constant clock period, with fixed clock-cycle rise timing, and varying duty ratio. The PPM modulation method (illustrated in Fig. 3) also uses a constant clock period, but — for a given duty ratio — realizes spread-spectrum operation by pseudo-random offsets in the ON time (i.e. in both rise and fall timings of the clock-cycle). The ASM modulation method (shown in Fig. 4) — for a given duty ratio — realizes spread-spectrum operation by pseudo-random variations in the period (clock width). The operation of PPM and ASM modulation methods is as follows:

For the PPM method (shown in Fig. 5), a pseudo-random value (0-3) is generated in every cycle. The mode is decided by the pseudo-random value, and determines clock timing offset as illustrated in Fig. 6. Modulated clock output in each mode (0-3) is illustrated in Fig. 7, and the relationship between pseudo-random values and corresponding modes for the PPM modulation method is shown in Table 1.

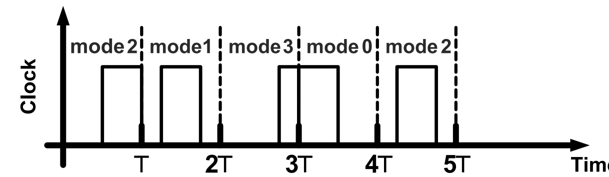
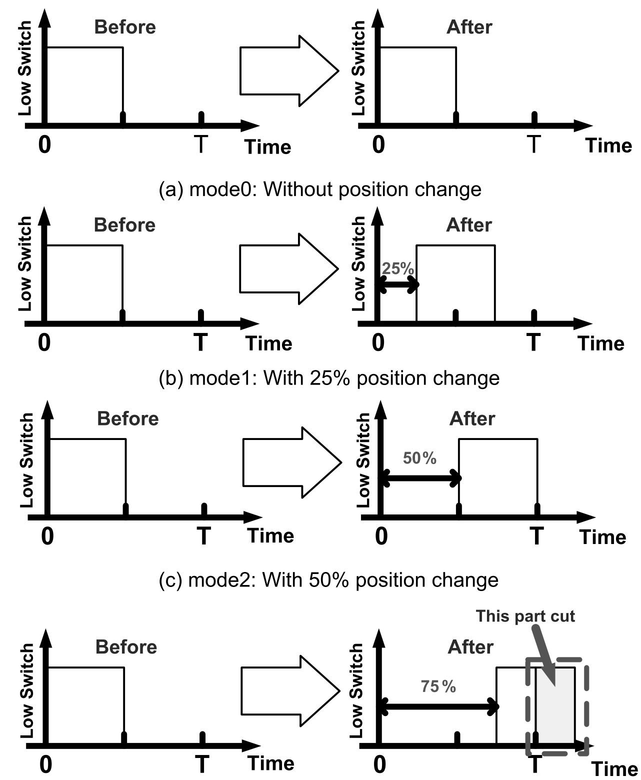


Fig. 6 Output clock of PPM modulation method.



(a) mode0: Without position change

(b) mode1: With 25% position change

(c) mode2: With 50% position change

(d) mode3: With 75% position change

Fig. 7 Operation of PPM modulation method for each mode.

Table 1 Relationship between pseudo-random values and corresponding modes for the PPM modulation method.

Random values and their corresponding modes			
Random I	Mode	Period	Rise-time of On-duty
0	0	T	No position change
1	1		25% position change
2	2		50% position change
3	3		75% position change

For the ASM method (shown in Fig. 8), a time delta of zero or either of two values is chosen in every cycle; this is either added to, or subtracted from, the period. The resultant five possible modes (A-E) are chosen depending on pseudo-random values, resulting in a clock output such as illustrated in Fig. 9. Chosen mode operation waveform is shown in Fig. 10. The relationship between pseudo-random

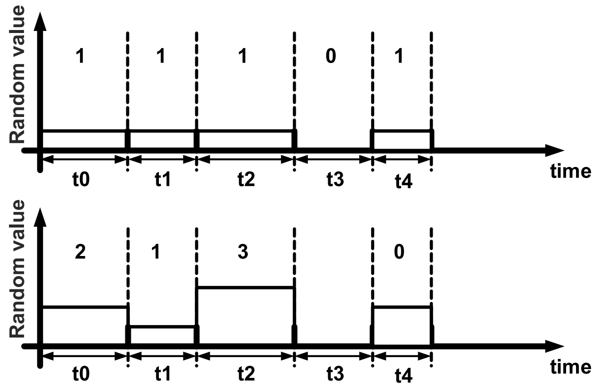


Fig. 8 Movement of pseudo-random values that are used in ASM modulation method.

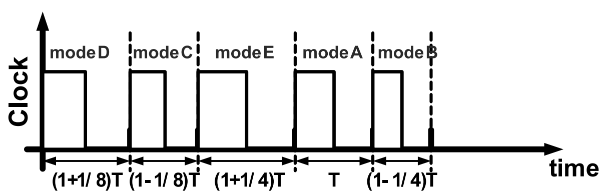


Fig. 9 Output clock of ASM modulation method.

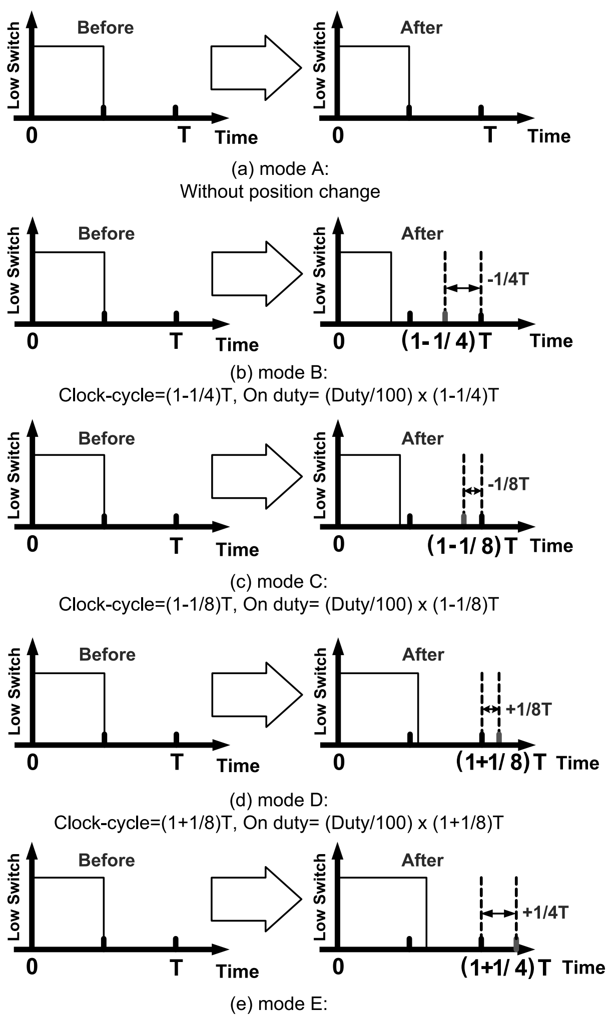


Fig. 10 Operation of ASM modulation method for each mode.

values and corresponding modes for the ASM modulation method is shown in Table 2.

We call our proposed spread-spectrum clock modulation methods PAS (PPM ASM Select) and PAF (PPM ASM Fused, which are composite of the two modulation methods PPM and ASM), and these two methods are described below.

3. Proposed Spread-Spectrum Clock Modulation Methods

This section describes the proposed spread spectrum modulation methods for our digitally-controlled switching converter in detail. First we describe the operation of the PAS modulation method in which PPM or ASM modulation is selected in a pseudo-random manner. Next we describe the operation of the PAF modulation method, which is a composite of the two different modulation methods, PPM and ASM.

- **PAS (PPM ASM Select) modulation method**
  For the PAS modulation method, either of two different modulation methods, PPM or ASM, is selected in a pseudo-random manner; in Fig. 1, either t_k or ϵ_k changes in each cycle while d_k is fixed (Fig. 12).

Table 2 Relationship between pseudo-random values and corresponding modes for the ASM modulation method.

Random values and their corresponding modes				
Random I	Random II	Mode	Period	On-time
0		A	T	(Duty/100) x T
1	0	B	(1-1/4)T	(Duty/100) x (1-1/4)T
1	1	C	(1-1/8)T	(Duty/100) x (1-1/8)T
1	2	D	(1+1/8)T	(Duty/100) x (1+1/8)T
1	3	E	(1+1/4)T	(Duty/100) x (1+1/4)T

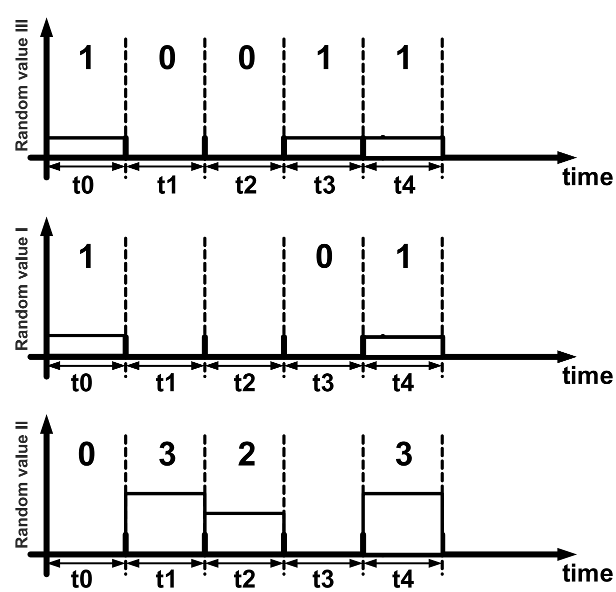


Fig. 11 Movement of pseudo-random values that are used in PAS modulation method.

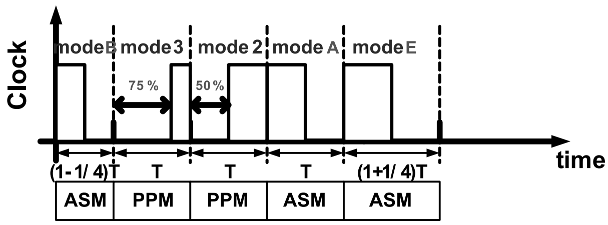


Fig. 12 Output clock of PAS modulation method.

Table 3 Relationship between pseudo-random values and corresponding modes for the PAS modulation method.

Random values and their corresponding modes						
Random III	Random I	Random II	Method	Mode	Period	On-time
0		0	PPM	0		No position change
		1		1		25% position change
		2		2		50% position change
		3		3		75% position change
1	0		ASM	A	T	(Duty/100) x T
	1	0		B	(1-1/4)T	(Duty/100) x (1-1/4)T
		1		C	(1-1/8)T	(Duty/100) x (1-1/8)T
		2		D	(1+1/8)T	(Duty/100) x (1+1/8)T
		3		E	(1+1/4)T	(Duty/100) x (1+1/4)T

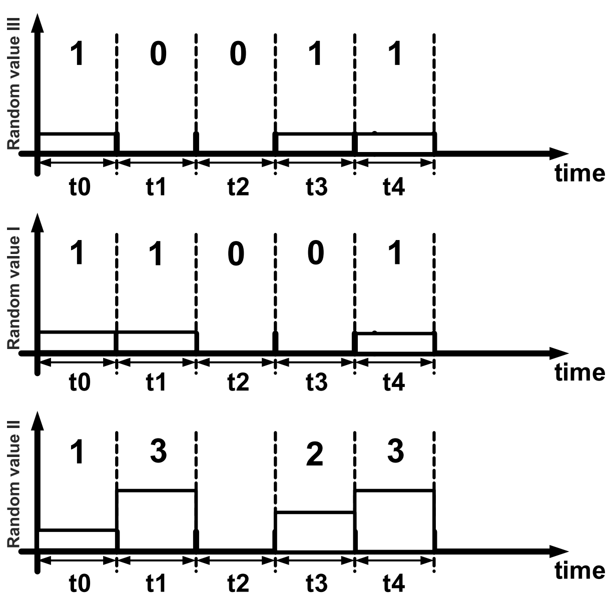


Fig. 13 Movement of pseudo-random values that are used in PAF modulation method.

Toggling between two modes can be easily realized in DSP. This modulation method operates by giving a pseudo-random value (shown in Fig. 11) to every clock-cycle which then provides an output clock as shown in Fig. 12. Since there are four PPM modes (0-3) and five ASM modes (A-E), there are nine possible output modes in total for this method. The relationship between the pseudo-random values and corresponding modes is shown in Table 3.

- **PAF (PPM ASM Fused) modulation method**
  The PAF modulation method combines two different modulation methods; in Fig. 1, both t_k and ϵ_k change in each cycle while d_k is fixed. Like PAS, it is generated by adding only one pseudo-random value. This modulation method operates by giving a pseudo-random value (shown in Fig. 13) to every clock-cycle which then provides an output clock shown in Fig. 14. From PPM modes (0-3) and ASM modes (A-E), the total output modes for this method are eleven modes as shown in Fig. 15. Table 4 shows the relationship between the pseudo-random values and corresponding modes.

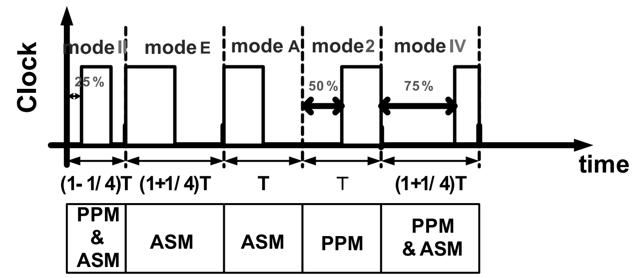


Fig. 14 Output clock of PAF modulation method.

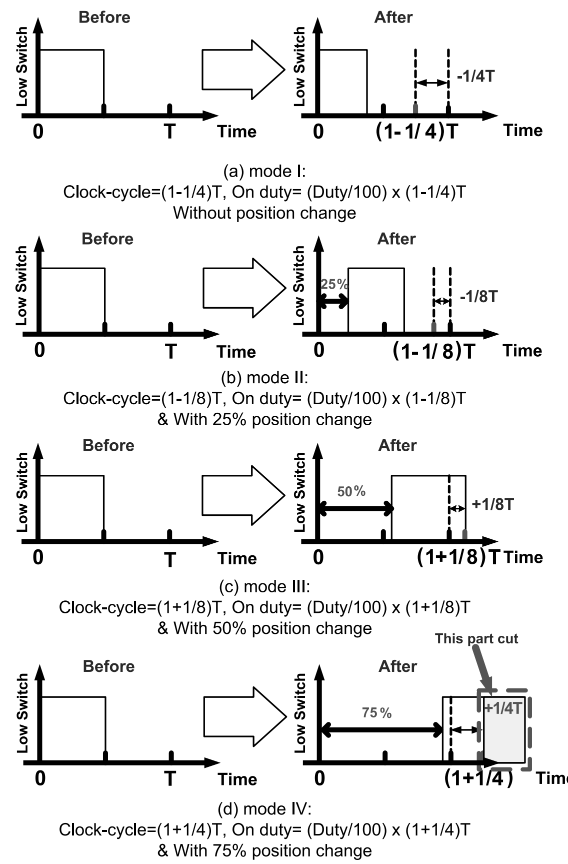


Fig. 15 Operation of PAF modulation method for each mode.

4. Simulation Verification

4.1 Technique for Simulating Digitally-Controlled DC-DC Converter

We have developed a technique for using SCAT (a high-

Table 4 Relationship between pseudo-random values and corresponding modes for the PAF modulation method.

Random values and their corresponding modes						
Random III	Random I	Random II	Method	Mode	Period	On-time
0	0		ASM	A	T	No position change
	1	0		B	(1-1/4)T	
		1		C	(1-1/8)T	
		2		D	(1+1/8)T	
		3		E	(1+1/4)T	
1	0	0	PPM	0	T	No position change
		1		1		25% position change
		2		2		50% position change
		3		3		75% position change
	1	0	PPM&ASM	I	(1-1/4)T	(Duty/100) x (1-1/4)T without position change
		1		II	(1-1/8)T	(Duty/100) x (1-1/8)T with 25% position change
		2		III	(1+1/8)T	(Duty/100) x (1+1/8)T with 50% position change
		3		IV	(1+1/4)T	(Duty/100) x (1+1/4)T with 75% position change

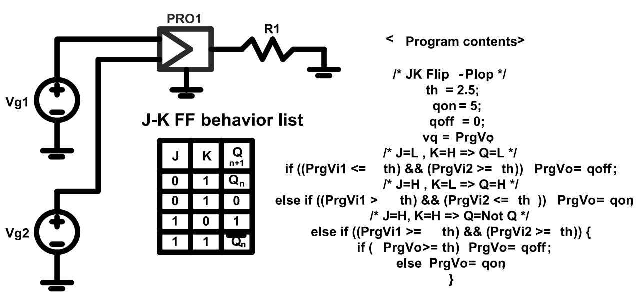


Fig. 16 Sample simulated device model.

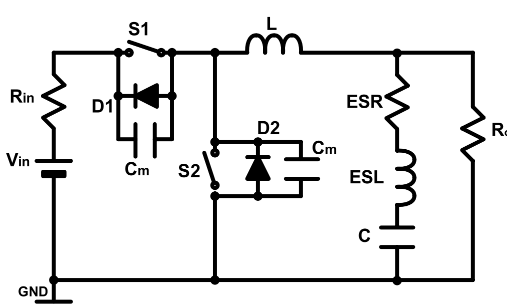


Fig. 17 Simulated circuit model.

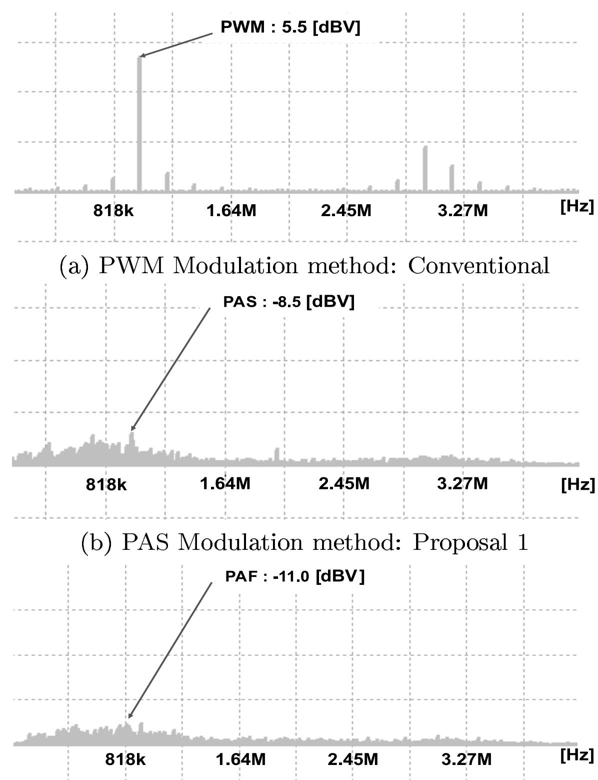
speed Switching Converter Analysis Tool) [11], to simulate digitally-controlled switching regulators, and used this to confirm the EMI-reduction effects of the proposed algorithms. SCAT can simulate circuits with various electronic elements and various clock modulations. Figure 16 shows an example of a device that can be simulated by this program. Figure 17 and Table 5 show the circuit model and parameters used for simulation of the proposed algorithms. Our program in SCAT enables parameter data to be stored for several different cycle types and each cycle time is changeable to simulate ASM operation by using "trigger elements" in SCAT.

In an actual digitally-controlled switching converter, DSP is used to emulate the SCAT program device.

Table 5 Circuit parameters used in the simulation.

Parameter item	Value
Rout	1 ohm
L	2uH
C	4.7uF
ESR	4m ohm
ESL	6.8nH
Cm (High Switch)	240nF
Cm (Low Switch)	100nF
Rin	1m ohm
Vin	6V
Fsw (Switching frequency)	1M , 2MHz
Dead time	10n/1MHz 5n/2MHz

Element	Ron	Roff
SwitchS1	0.4m	1M
SwitchS2	0.8m	1M
Element	Ron	Roff
DiodeD1	10m	1M
DiodeD2	10m	1M



(a) PWM Modulation method: Conventional

(b) PAS Modulation method: Proposal 1

(c) PAF Modulation method: Proposal 2

Fig. 18 Noise power in frequency domain (Duty=50%).

4.2 Simulation Results

We have performed circuit simulation with the SCAT simulator based on the circuit in Fig. 17 with parameters in Table 5, which is a widely-used type of buck converter on the market. Figure 18 shows a comparison of noise power for PWM modulation and for the two proposed noise-reduction modulation methods. Moreover, results of a simulation of the variation in noise power with clock duty cycle for PWM, PPM, ASM and the two proposed methods are shown in Fig. 19. We see that the proposed methods significantly reduce noise power compared to conventional methods.

4.3 Discussion

Let us consider why the proposed methods, PAS and PAF, are more effective for spectrum spreading. We see in Fig. 19 that at duty ratio of 50% the noise power for PWM and ASM is at a maximum, while it is at a minimum for PPM. On the other hand, the noise power is low over a wide range of duty ratio for PAS and PAF. This can be explained as follows:

(i) When duty ratio is 50%, for a PWM signal with a period of T, a Fourier series expansion shows that the signal frequency component at $1/T$ is large compared with the harmonic components of the PWM signal. However it is smaller when the duty ratio is much smaller or larger than 50%; this explains why, for PWM, the noise output is maximum at duty ratio of 50%.

(ii) ASM can be considered as frequency modulation, because the clock period t_k (which is the reciprocal of the frequency) changes in each cycle, which causes spectrum spreading from approximately $\min_k(f_0, f_1, \ldots f_k, \ldots)$ to $\max_k(f_0, f_1, \ldots f_k, \ldots)$ (where $f_k = 1/t_k, k = 0, 1, 2, \ldots$). Like the PWM case, the ASM signal has large signal components of $f_0, f_1, \ldots f_k, \ldots$ at duty ratio of 50% compared with harmonic components, and this is why — for ASM too — the noise output is a maximum at duty ratio of 50%. We note that a more detailed analysis of ASM is given in [7].

(iii) For PPM we can consider the clock to be phase modulated. For simplicity let us consider the case where the duty ratio is 50% and the PPM clock is approximated by a sinusoidal signal. The phase-modulated sinusoidal signal is given by

$$y(t) = \sin\left(2\pi\frac{t}{T} + \theta_n(t)\right).$$

It is known [12] that the spectrum is spread due to phase noise (or pseudo-random phase modulation) $\theta_n(t)$, which intuitively explains why PPM realizes spectrum spreading. Figure 20 shows the PWM signals with several duty ratios (top), the corresponding PPM signals (middle), and also the difference (exclusive OR) between the PWM and PPM signals (bottom). We see that the PPM signal most differs from the corresponding PWM signal (which means that the spectrum of the PPW signal spreads) at duty ratio of 50%; this explains why for PPM the noise power is minimum at duty ratio of 50% in Fig. 19.

(iv) For PAF, the clock can be considered to be simultaneously phase and frequency modulated; this explains qualita-

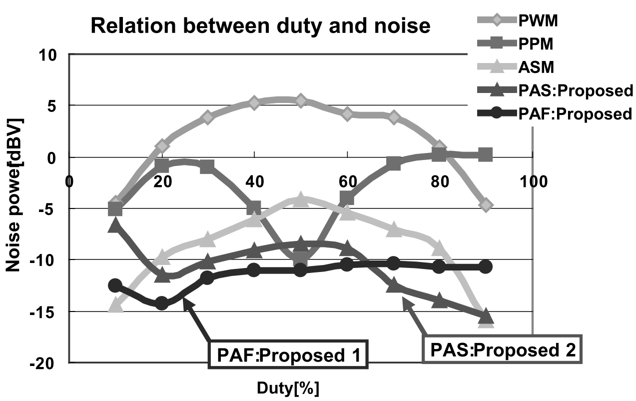


Fig. 19 Noise power comparison.

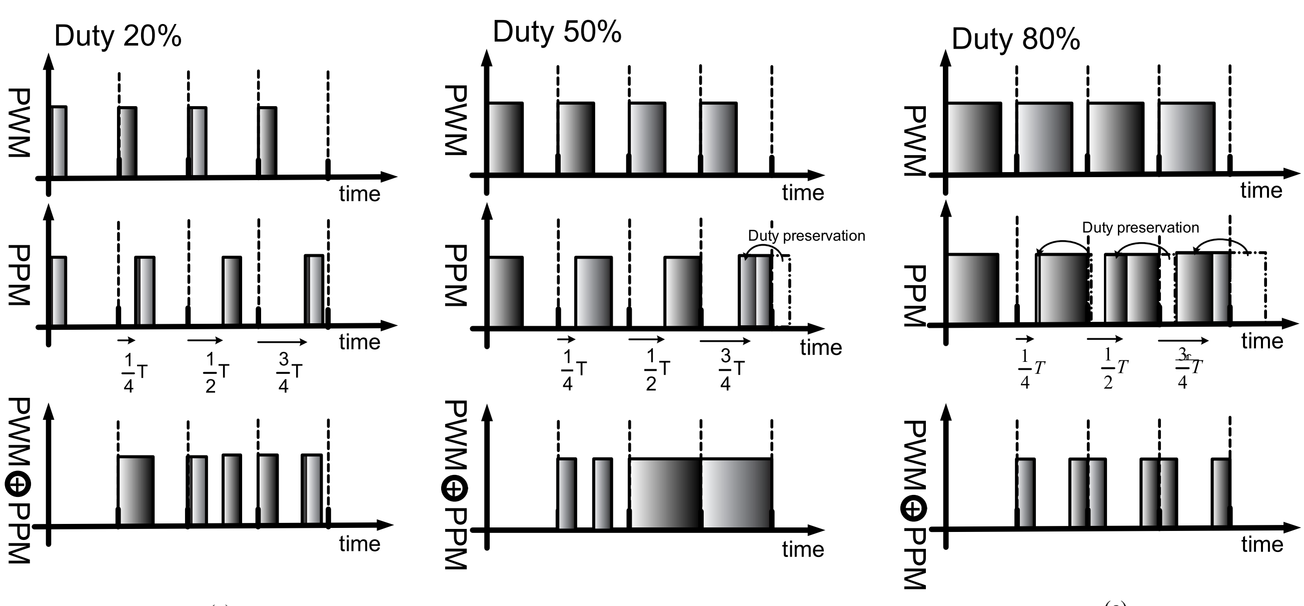


Fig. 20 PWM, PWM and their exclusive OR, where a PPM pulse is within one period. (a) Duty ratio 20%. (b) 50%. (c) 80%.

tively why PAF is more effective than PPM or ASM. PAS can be considered to be a special case of PAF where either frequency or phase modulation is performed in each cycle. Both PAF and PAS are composite modulation methods (combining ASM and PPM), and ASM is effective for spectrum spreading at small or large duty ratios while PPM is effective around duty ratio of 50%. Hence the proposed methods are effective over a wide range of duty ratios. We close this section by remarking that almost the same effectiveness as shown in Fig. 19 is obtained for simulations with various conditions.

5. Conclusions and Future Work

In this paper, we have proposed two effective spread-spectrum clock algorithms which are too complex to realize with conventional analog-controlled switching converter but which are easily realizable with digitally-controlled switching converters. In other words, we have shown that EMI can be reduced using spread-spectrum clocking in digitally-controlled switching converters. Moreover, we have also established a technique for simulating digital power converters using the SCAT simulator. We have verified by simulation that the proposed spread-spectrum clock modulation method algorithms had significant EMI reduction effect compared to conventional spread-spectrum clock modulation methods. However, we note that using spread-spectrum clocking in digital or analog control systems tends to increase the ripple of the output voltage. In future work, we plan to quantify the effect of spread-spectrum clocking on output ripple.

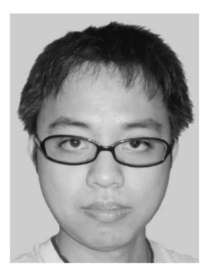
Acknowledgment

The authors would like to thank S. Suzuki, T. Odaguchi, Y. Koike of Toko Inc. and H. San, T. Komuro of Gunma University for valuable discussions. Thanks are also due to K. Wilkinson for improving English in the manuscript.

References

[1] H. Yamasaki, EMC of Digital Circuit, Ohm Publisher, 2002.
[2] M. He and J. Xu, "Nonlinear PID in digital controlled buck converters," IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, Feb. 2007.
[3] M. Kono, K. Kimura, I. Mori, Y. Yamada, H. Kobayashi, Y. Kobori, K. Shimizu, and K San, "High-resolution DPWM generator for digitally controlled DC-DC converters," IEICE Trans. Electron. (Japanese Edition), vol.J91-C, no.8, pp.418–427, Aug. 2008.
[4] I. Mori, K. Kimura, Y. Yamada, H. Kobayashi, Y. Kobori, S.A. Wibowo, K. Shimizu, M. Kono, and H. San, "High-resolution DPWM generator for digitally controlled DC-DC converters," IEEE Asia Pacific Conference on Circuits and Systems, Macao, China, Dec. 2008.
[5] K. Shimizu, K. Ando, I. Mori, H. Miyajima, H. Kobayashi, H. San, N. Takai, M. Moriguchi, Ch. Murayama, Y. Nishida, and H. Yoshida, "Digital PWM generator using ring oscillator circuit," Papers of Technical Meeting on Electronic Circuits, ECT-08-023, IEE Japan, Toyohashi, March 2008.
[6] T. Tanaka, H. Hamasaki, and H. Yoshida, "Random-switching control in DC-to-DC converters: An implementation using M-sequence," IEEE PESC, July 1992.
[7] T. Tanaka, H. Kameda, and T. Ninomiya, "Noise analysis of DC-to-DC converter with random-switching control," IEICE Trans. Commun., vol.E75-B, no.11, pp.1142–1150, Nov. 1992.
[8] A.M. Stankovic, G.C. Verghese, and D.J. Perreault, "Analysis and synthesis of randomized modulation schemes for power converters," IEEE Trans. Power Electron., vol.10, no.6, pp.680–693, Nov. 1995.
[9] T. Daimon, H. Sadamura, T. Shindou, H. Kobayashi, M. Kono, T. Myono, T. Suzuki, S. Kawai, and T. Iijima, "Spread-spectrum clocking in switching regulators for EMI reduction," IEICE Trans. Fundamentals, vol.E86-A, no.2, pp.381–386, Feb. 2003.
[10] H. Sadamura, M. Namekata, M. Kono, H. Kobayashi, and N. Ishikawa, "EMI reduction technique of switching regulators and its measurement verification," IEICE Trans. Electron. (Japanese Edition), vol.J86-C, no.11, pp.1169–1176, Nov. 2003.
[11] M. Nakagawa, SCAT Power Simulation Introduction, Nikkan-Kogyo Newspaper Publishing Company, 2004.
[12] T.H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Second Edition, Cambridge University Press, 2004.

Ibuki Mori received a B.S. degree (honored) in electronic engineering from Gunma University in 2007, and currently he is a graduate student in the Masters course there. His research interests include design of analog integrated circuit and switching power DC-DC converters such as DPWM generator for digitally controlled DC-DC converters.



Yoshihisa Yamada received B.S. and M.S. degrees in electronic engineering from Gunma University, Japan, in 2004 and 2006, respectively. He is currently working for MITSUBA Corporation.

Santhos A. Wibowo received a B.S. degree in electronic engineering from Gunma University in 2007, and currently he is a graduate student in the Masters course there. His research interests include switching power DC-DC power converters such as the analysis of coupled-inductor circuits used for fast-response low-ripple DC-DC converters.

Masashi Kono received B.S., M.S. and Ph.D. degrees in electronic engineering from Gunma University, Kiryu, Japan, in 2003, 2005 and 2008 respectively. In 2008, he joined the Central Research Laboratory, Hitachi, Ltd., Tokyo, Japan, where he is engaged in research for analog integrated circuit design. He is a member of the IEEE and the Institute of Electrical Engineers of Japan (IEEJ). He received a Young Researcher Encouragement Award from the Institute of Electrical Engineers of Japan in 2003.

Haruo Kobayashi received B.S. and M.S. degrees in information physics from University of Tokyo in 1980 and 1982 respectively, an M.S. degree in electrical engineering from the University of California at Los Angeles (UCLA) in 1989, and the Dr. Eng. degree in electrical engineering from Waseda University in 1995. He joined Yokogawa Electric Corp. Tokyo, Japan in 1982, and was engaged in research and development related to measuring instruments and mini-supercomputers. From 1994 to 1997, he was involved in research and development of ultra-high-speed ADCs/DACs at Teratec Corp. and was also an adjunct lecturer at Waseda University. In 1997, he joined Gunma University and presently is a Professor in the Electronic Engineering Department there. His research interests include mixed-signal integrated circuit design and signal processing algorithms. He received the Best Paper Award from the Japanese Neural Network Society in 1994, and the Yokoyama Award in Science and Technology in 2003.

Yukihiro Fujimura received a B.S. degree in electronic engineering from Gunma University in 2007, and he is currently a Master course student there. His research interests include design techniques for switching regulators with fine CMOS processes such as high-frequency ramp wave generator circuits.

Nobukazu Takai received B.E. and M.E. degrees from Tokyo University of Science, Tokyo, Japan, in 1993 and 1995 respectively, and a Doctor of Engineering degree from Tokyo Institute of Technology, Tokyo, Japan, in 1999. He worked at Tokyo Polytechnic University from 1999 to 2004. In 2004, he became an Assistant Professor of Gunma University. His main interests lie in the field of analog integrated circuit design, especially ultra-low-voltage amplifiers, filter design, and power supply circuitry. He was awarded the Best Paper Prize from the Institute of Electrical Engineers of Japan in 1999. Dr. Takai is a member of the Institute of Electrical Engineers of Japan, and the Institute of Electrical and Electronics Engineers.

Toshio Sugiyama received a B.E. degree in electrical engineering from Tokyo Denki University, Tokyo, Japan, in 1997. He joined Toko Inc., Saitama, Japan, in 1997, and was initially engaged in developing AM/FM IF ICs for receivers. He is currently engaged in the development of DC-DC converter ICs.

Isao Fukai received a B.E. degree in electronic engineering from Tokyo Polytechnic University (Tokyo Kougei Daigaku), Kanagawa, Japan, in 1989. He joined Toko Inc., Saitama, Japan, in 1989, where he was engaged in the development of AM/FM IF ICs for receivers, and DC-DC converter ICs. Currently he manages IC development for DC-DC converters. He is interested in DC-DC converter ICs and RF ICs.

Norihisa Onishi received a B.S. degree in electronics from Okayama University of Science, Okayama, Japan, in 1978. He joined Tokyo Sanyo Electric Co., Ltd., Gunma, Japan, in 1979, which merged with Sanyo Electric Co., Ltd., Gunma, Japan, in 1986. At these companies he was engaged in developing and designing MOS LSIs. In 2005 he joined Toko Inc., Saitama, Japan, where he has been engaged in the management of bipolar and MOS IC development.

Ichiro Takeda received a B.E. degree in electronic engineering from Osaka Electro-Communication University, Osaka, Japan, in 1970. He joined San-esu Co., Ltd., Tokyo, Japan, in 1970, and was engaged in designing VHF/UHF band electronically-tuned front-end modules for TVs. In 1973 he joined Toko Inc., Tokyo, Japan, and was engaged in designing PLL ICs for frequency synthesizers and function generator ICs for numerical control. He was also involved in CAD work on Vax11/780 for ten years. He is currently working for Toko Inc.

Jun-ichi Matsuda received a B.E. degree in electronic engineering, an M.E. degree in electrical engineering and a D.E. degree in electrical engineering from Doshisha University, Kyoto, Japan, in 1977, 1979, and 1995, respectively. In 1979 he joined Tokyo Sanyo Electric Co., Ltd., Gunma, Japan, which merged with Sanyo Electric Co., Ltd., in 1986. At these companies he was engaged in research and development of small-feature-size CMOS devices for VLSIs. In 2005 he joined Toko Inc., Saitama, Japan, where he has been engaged in the management of analog IC and discrete device development. He has also been a visiting professor of Gunma University, Gunma, Japan, since 2002. He is a member of the Japan Society of Applied Physics and the Physical Society of Japan.