Architecture of Wideband High-Efficiency Envelope Tracking Power Amplifier for Base Station

Masato KANETA[†] Akihiro KANBE[†] Fuminori YUI[†] Haruo KOBAYASHI[†]

Hitoshi HIRATA[‡] Tatsuhiro SHIMURA[‡] Kentarou YAMAGISHI[‡]

† Faculty of Engineering, Gunma University 1-5-1 Tenjincho, Kiryu, Gunma, 105-0123 Japan
‡ Sumitomo Electric Industries,Ltd 1-1-3 Shimaya, Konohana-ku, Osaka, 565-0456 Japan

E-mail: †m08e614@gs.eng.gunma-u.ac.jp,

Abstract This paper proposes a new architecture for envelope-tracking power supplies for base stations. The proposed multiphase DC-DC converter circuit uses multiple switching circuits (as well as a voltage follower circuit), each optimized for a different envelope frequency, to realize both high efficiency and wide bandwidth. The operation of the circuit, and simulation results, are described.

Keyword Power Amplifier, Power Supply, Envelope Tracking, Base Station

1. Introduction

Power amplifiers for base stations require both high efficiency and wide bandwidth. Fig.1 shows a history of recent advances in design techniques for high-efficiency power amplifiers. One such technique for efficiency improvement is to use a class AB amplifier and digitally precompensate for distortion. However, efficiency gains from such techniques have reached a limit.

The efficiency of an RF amplifier is given by

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{DD} \times I_{DD}} \quad (1)$$

This paper proposes a promising new envelope-tracking power supply architecture using multiple switching circuits, each optimized for a different frequency, to realize both high efficiency and wide bandwidth. This power supply tracks the RF input signal envelope and provides a variable supply voltage V_{DD} to the RF power amplifier. Both V_{DD} and V_{OUT} vary together (see Fig. 2), greatly increasing power efficiency compared with using a fixed-voltage power supply. This technique is especially effective for W-CDMA and OFDM where the peak signal power is much higher than the average power.



Fig.1. High efficiency techniques for power amplifiers

2. Principles of envelope-tracking power supply

Fig.2 illustrates the principles of an envelope tracking power supply, which detects the envelope of the RF amplifier input signal and controls the RF power amplifier power supply voltage accordingly. Using a variable V_{DD} reduces average power dissipation and increases permissible peak output, and thus enables higher amplifier power efficiency than is possible with a fixed power supply voltage. This technique is especially effective for W-CDMA and OFDM, where the peak signal power is much higher than the average power. This circuit consists of an operational amplifier, used as a wideband voltage source, plus a DC-DC converter used as a high-efficiency current source.



Fig.2. Envelope-tracking power supply.

Fig.3 illustrates W-CDMA envelope power spectrum density; most of the envelope power is found in a narrow

frequency band around the center frequency. The DC-DC converter of the envelope-tracking power supply needs to have high efficiency over the frequency range of the modulation envelope.



Fig.3. W-CDMA envelope power spectrum [2]



Fig.4. Conventional envelope tracking power supply circuit [1].

3. Operation of conventional envelope tracking power supply

Fig.4 shows the conventional envelope tracking power supply circuit, with the RF amplifier we modeled as a resistance load. This circuit has only five parameters: supply voltage, load resistance, current sense resistance, inductance, and width of hysteresis band. When we input a DC signal, the operational amplifier provides current to the load resistance such that the output voltage equals the input voltage, and the voltage across the sense resistor terminals increases. When a comparator turns on the MOSFET switch, the current in the inductance increases gradually and the operational amplifier current decreases. The voltage across the sensing resistor decreases until the comparator turns the MOSFET switch off. Then the current in the inductance decreases gradually, and accordingly the voltage follower output current increases to make up the output current. These actions are repeated (in other words, the circuit oscillates). The hysteresis band determines the gap between switch-on and switch-off points. The larger the hysteresis band, the

longer the switching interval. Also, the larger the inductance the longer the switching interval. Therefore, we see that the switching frequency is inversely proportional to both the inductance value and the hysteresis band. Fig.8 shows simulation results for the circuit in Fig.4 where the input is a DC signal, while Fig.9 shows results when the input is a sine wave signal.



Fig.5. Operation of conventional circuit in Fig.4 at initial state.



Hysteresis Band

Fig.6. Steady-state operation of conventional circuit in Fig.4.



Fig.7. Switching frequency with respect to h and L.



Fig.8. Simulation results for Fig.4 where the envelope signal is a DC signal.



Fig.9. Simulation results for Fig.4 where the envelope signal is a sine wave signal.

4. Design techniques for envelope-tracking power supply

The circuit in Fig.4 has five parameters. The specifications determine the values of the power supply and the load resistance. The sense resistance value is chosen to be much smaller than the load resistance. Therefore, the circuit designer can determine only the values of two parameters — inductance, and width of the hysteresis band. We want to provide as much power as possible to the load resistance from the DC-DC converter, because the efficiency of the DC-DC converter is much higher than that of the operational amplifier. Setting a small inductance value, to increase the bandwidth of the DC-DC converter, increases the switching frequency. Setting a smaller hysteresis band, to increase efficiency, also increases the switching frequency. Therefore, we fix the switching frequency at the maximum value determined

by both comparator and FET switch capacitance: the value of (inductance) x (hysteresis band) is set to a constant. With this circuit, there is a tradeoff between efficiency and bandwidth, and the circuit designer should choose the optimum value of inductance and hysteresis. Efficiency of this circuit is maximum when the average slope of input envelope signal is equal to the slope of the DC-DC converter output current. We can optimize circuit parameters; the optimum inductance is given by

$$L_{match_{SR}} = \frac{2(1-D)V_{S_{DC}}R_{Load}}{\left|\overline{\Delta V_{S} / \Delta t}\right|} \quad (2)$$

All of the right-side terms are known. In addition, the switching frequency is given by

$$f_{SW} = \frac{R_{sence}}{L} \frac{V_{DD}}{h} D \left(1 - D \frac{V_{S_RMS}^2}{V_{S_DC}^2} \right) (3).$$

Right-side terms except hysteresis are known. Therefore, the hysteresis band value is decided by the maximum switching frequency.

5. Problems with the conventional envelope tracking circuit

The above circuit is optimized only for average input slope value. The efficiency of this circuit falls when the average slope of the input envelope signal is not equal to the slope of the DC-DC converter output current: the efficiency of this circuit falls when the input slope is greater than the slope of the DC-DC converter output, because the operational amplifier provides all of the output current (Fig.10). The efficiency of this circuit also falls when the input slope is less than the slope of the DC-DC converter output, because hysteresis is larger than the optimum value.



Fig.10. In the case that the input slope surpasses the slope of DC-DC converter output.

6. Proposed envelope-tracking circuit

Fig.11 shows an improved circuit, using two DC-DC converters with comparator hysteresis. The proposed circuit switches from single-phase operation to two-phase operation depending on the slope of the envelope input. We fix the value of (inductance) x (hysteresis) for a given switching frequency. We change the ratio of inductance to hysteresis for dual phases. A "slow-phase" DC-DC converter with large inductance has high efficiency and narrow bandwidth, while a "fast-phase" DC-DC converter with small inductance has low efficiency and wide bandwidth. These circuits sense the input slope and switch the DC-DC converter modes accordingly. The proposed circuit maintains high efficiency over a wide range of input envelope slopes. When the input slope is small, only the slow phase operates. When the input slope is high, then the voltage follower provides more current. If the voltage follower current exceeds the hysteresis threshold, both slow phase and fast phase DC-DC converter circuits operate.



Fig.11. Proposed envelope-tracking circuit.

Opamp Current



Fig.12. Switching method in the proposed circuit.

7. Operation of the proposed circuit

We have performed simulation using SIMPLIS to confirm operation of the proposed circuit. Fig.13 shows

waveforms when the input signal slew rate is low. Fig.14 shows waveforms when the input slew rate is high. The simulation results agree with the theory. This confirms operation of both slow phase and fast phase. As a more realistic example, when we vary the input slope periodically (Fig.15), the proposed circuit switches its operation instantaneously depending on the input slope (Fig.16). We therefore expect that the proposed circuit will improve amplifier efficiency for W-CDMA and OFDM signals.



Fig.13. Operation waveforms when the input slew rate is low.



Fig.14. Operation waveforms when the input slew rate is high.



Fig.15. Input envelope signal used for simulation.



Fig.16. Simulation results for Fig.11 where the input slew rate is varying as in Fig.15.

8. Interleaved Architecture with PWM Signal

In this section, we describe a method using triangular or sawtooth modulation of the hysteresis signal controlling the PWM DC-DC converter, instead of using just the hysteresis comparator alone. Fig.17 shows a single-phase architecture [8], and Fig.18 shows its simulated current and PWM signal waveforms. For given bandwidth, it appears that this circuit operates more reliably than the two-inductor circuit of Fig. 11.

Fig.17. Envelope-tracking power supply using DC-DC converter with PWM signal.

Fig.18. Current and PWM signal waveforms in Fig.17.

We further propose the multi-phase architecture of Fig.19, with two (or multiple, N) DC-DC converters and triangular-wave modulation with 180° (or 360/N degree) phase difference, so that voltage ripple is cancelled; bandwidth is also increased, as the inductors are effectively in parallel. Fig.20 shows simulated OpAmp current, inductor current, output current and PWM signals.

Fig.19. Proposed multi-phase architecture.

Fig.20 Simulated current and PWM signal waveforms for Fig.19.

Fig.21 Comparison of OpAmp currents in the single-phase and multi-phase architectures.

Fig.21 shows a comparison of OpAmp currents for the single-phase and multi-phase architectures; we see that the OpAmp current of the multi-phase architecture is smaller than that for the single-phase architecture, which means higher efficiency.

9. Conclusions

This paper proposes new architectures for envelope-tracking power supplies for base stations. The proposed circuits have two DC-DC converters as well as a voltage follower, and can realize both high efficiency and wide bandwidth. Operation switches automatically between the two DC-DC converters depending on the slope of the input signal envelope. This improves the power efficiency of W-CDMA and OFDM transmitters. We have described a circuit with two DC-DC converters, but three or more DC-DC converters could be used to further improve the efficiency. Further studies of the proposed circuits are underway.

Acknowledgments

The authors would like to thank N. Ishihara, K. Totani, D. F. Kimball, L. E. Larson, T, Nabeshima and K. Wilkinson for valuable discussions.

References

- [1] D. F. Kimball, J. Jeong "High-Efficiency Envelope-Tracking W-CDMA Base-Station Amplifier Using GaN HFETs", IEEE Trans. on Microwave Theory and Techniques, vol.54, no.11 (Nov. 2006).
- [2] F. Wang, "High Efficiency Linear Envelope Tracking and Envelope Elimination and Restoration Power Amplifier for WLAN OFDM Applications," Ph.D. Dissertation, University of California, San Diego (2006).
- [3] P. Asbeck, D. Kimball, "Next Generation High-Efficiency RF Transmitter Technology for Base stations", Extended Abstracts of 2007 International Conference on Solid State Devices and Materials, pp. 146-147, Tsukuba (Sept. 2007).
- [4] P. Draxler, S. Lanfranco, et.al., "High Efficiency Envelope Tracking LDMOS Power Amplifier for W-CDMA", IEEE MTT-S International Microwave Symposium, pp.1534-1537 (June 2006).
- [5] S.C.Cripps, RF Power Amplifier for Wireless Communications, Artec House (1999).
- [6] S.C.Cripps, Advanced Techniques in RF Power Amplifier Design, Artec House (2002).
- [7] A. Kanbe, M. Kaneta, H. Kobayashi, H. Yui, YUI, N. Takai, H. Hirata, T. Shimura, K. Yamagishi, "New Architecture of Envelope Tracking Power Amplifier for Base Station" IEEE Asia Pacific Conference on Circuits and Systems, Macao, China, pp.296-299, Dec. 2008.
- [8] B. Bakkaloglu, C. Chu, S. Kiaei, "A 10MHz Bandwidth 2mV Ripple PA Supply Regulator for CDMA Transmitters," ISSCC, pp.448-449 (Feb, 2008).