Invited Paper

A CMOS Multibit Complex ΔΣAD Modulator

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Abstract

We have designed, fabricated and measured a second-order multibit switched-capacitor complex bandpass ΔΣAD modulator to evaluate our new algorithms and architecture. We propose a new structure of a complex bandpass filter in the forward path with I, Q dynamic matching, that is equivalent to the conventional one but can be divided into two separate parts. As a result, the ΔΣ modulator, which employs our proposed complex filter can also be divided into two separate parts, and there are no signal lines crossing between the upper and lower paths formed by complex filters and feedback DACs. Therefore, the layout design of the modulator can be simplified. The two sets of signal paths and circuits in the modulator are changed between I and Q while CLK is changed between high and low by adding multiplexers. Symmetric circuits are used for I and Q paths at a certain period of time, and they are switched by multiplexers to those used for Q and I paths at another period of time. In this manner, the effect of mismatches between I and Q paths is reduced. Two nine-level quantizers and four DACs are used in the modulator for low-power implementations and higher signal-to-noise-and-distortion (SNDR), but the nonlinearities of DACs are not noise-shaped and the SNDR of the ΔΣAD modulator degrades. We have also employed a new complex bandpass data-weighted averaging (DWA) algorithm to suppress nonlinearity effects of multibit DACs in complex form to achieve high accuracy; it can be realized by just adding simple digital circuitry. To evaluate these algorithms and architecture, we have implemented a modulator using 0.18μm CMOS technology for operation at 2.8V power supply; it achieves a measured peak SNDR of 64.5dB at 20MS/s with a signal bandwidth of 78kHz while dissipating 28.4mW and occupying a chip area of 1.82mm^2. These experimental results demonstrate the effectiveness of the above two algorithms, and the algorithms may be extended to other complex bandpass ΔΣAD modulators for application to low-IF receivers in wireless communication systems.

I. Introduction

In the RF receiver of communication systems, low-IF receiver architecture is frequently used so that more receiver functions, such as multi standard and automatic gain control, can be moved to the digital part to provide more programmability. In conventional low-IF receiver architectures, two real (one input and one output) ΔΣAD modulators are used for in-phase (I) and quadrature (Q) paths. Its disadvantage is that not only input signals but also image signals are converted by ADCs. On the other hand, a complex bandpass ΔΣAD modulator can provide superior performance to a pair of real bandpass ΔΣAD modulators of the same order. It processes just input I and Q signals, not image signals, and AD conversion can be realized with low power dissipation. Thus, they are desirable for such low-IF receiver applications[1]–[5].

The use of a low-order multibit ΔΣAD modulator makes higher resolution possible with a low oversampling ratio (OSR), and the stability problem is alleviated. It is attractive for low-power implementations because it alleviates the slew-rate requirements of operational amplifiers with a high dynamic range in the modulator. However, multibit DACs cannot be made perfectly linear and their nonlinearity in the feedback paths are equivalent to errors added directly to the input signals; hence, they may degrade the SNDR of the ΔΣAD modulator. Then we developed a data-weighted averaging (DWA) algorithm for complex bandpass modulators [6], [7], which is implemented by just adding simple digital circuitry to suppress nonlinearity effects of multibit DACs in a complex form.

The performance of the complex bandpass ΔΣAD modulator is degraded by mismatches between I and Q paths, which cause both signal and quantization noise in the mirror image band and aliasing in the design signal band, thereby decreasing the SNDR of the complex modulator.

On the basis of the above consideration, we proposed new algorithms and a new architecture. We propose a new switched-capacitor topology architecture, that is suitable for complex bandpass ΔΣAD modulators and compensates for mismatches between I and Q paths. The new architecture reduces the amount of mirror image band quantization noise aliased into the signal band. Moreover, this technique can be extended to multibit modulators suitable for complex bandpass DWA algorithm[8], [9]. Furthermore, in the realization of complex ΔΣAD modulators, their layout design becomes complicated because of signal lines made to cross by complex filters and feedback from DACs for I and Q paths in the modulator, and this increases the required chip area. We propose a new structure for a complex bandpass ΔΣAD modulator, which has a symmetrical configuration that can be divided into two separate paths without crossing signal lines between the upper and lower circuit parts; thus, the required chip area is reduced and its layout design can be simplified.

In this paper, we present the chip implementation of a complex bandpass ΔΣAD modulator with switched-capacitor circuits, in order to evaluate the effectiveness of the above-mentioned two algorithms using a real chip.

II. Complex Bandpass ΔΣAD Modulator Architecture

A complex bandpass ΔΣAD modulator gains its advantage by implementing the poles and zeros of its loop filter without their conjugates, which are leaked in the image band for a complex single-side band signal. Fig.1 shows a simplified block diagram of the proposed complex bandpass ΔΣAD modulator (whose topology is derived from modifying that of a real

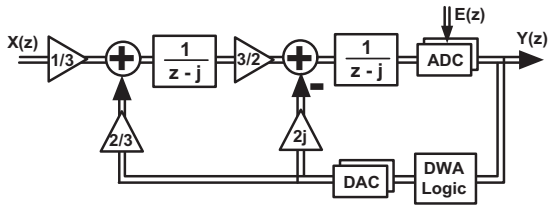

Fig. 1. Block diagram of the complex bandpass ΔΣAD modulator.

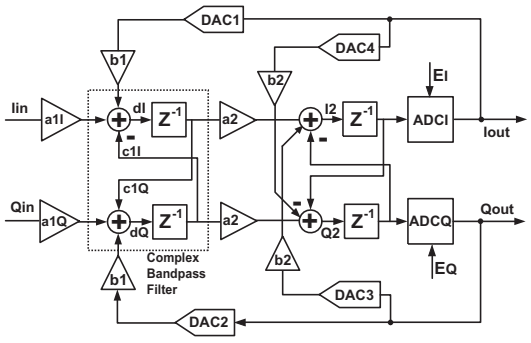

Fig. 2. Conventional complex bandpass ΔΣAD modulator.

lowpass ΔΣAD modulator in [10] by replacing z^{-1} with jz^{-1}); it is a second-order structure with two discrete-time complex integrators (or complex bandpass filters) and two nine-level quantizers surrounded by two feedback loops. The input and output of the complex bandpass ΔΣAD modulator can be expressed as

$$Y(z) = 0.5z^{-2}X(z) + (z-j)^2 z^{-2}E(z). \tag{1}$$

Then the signal transfer function (STF) and noise transfer function (NTF) of the complex modulator can be given by

$$STF(z) = 0.5z^{-2} \tag{2}$$
$$NTF(z) = (z-j)^2 z^{-2}. \tag{3}$$

Here, the passband center of the modulator is at $f_s/4$ (f_s is the sampling frequency of the modulator). Complex poles of the filter ($z = j$) can be implemented either with real integrators [4], or with a cascade of unit delay-cell architecture [13] (Fig.2). In our modulator design, we choose the delay-cell architecture since it operates fast and has simple coefficient values. DWA logic circuits are used to realize our proposed complex DWA algorithm, which will be described in section IV.

III. New Structure of Complex Bandpass Filter

Fig.2 shows a conventional structure of a second-order complex bandpass ΔΣAD modulator, which is composed of a second-order complex bandpass filter, two ADCs and four DACs. The modulator has I and Q signal crossing lines inside as shown in Fig.2; it has not only signal crossings between the I and Q paths of the complex filter, but also signal crossings between the feedback paths through two DACs to the second stage of the complex filter in I and Q paths.

Fig.3(a) shows a basic complex bandpass filter in the modulator (Fig.2) in the case of c1I = c1Q = 1, while Fig.3(b) shows its proposed equivalent implementation, where four multiplexers (MUXs) are added and their select signal (SEL) toggles at half the rate of CLK in the z^{-1} block, after which they are synchronized. The proposed complex filter is divided into two separate parts without any crossing of signal lines.

The proposed complex filter operates with two states; in state 1 (in Fig.3(c)), the upper part of the circuit is used for the I path, while the lower part is for the Q path. In state 2 (in Fig.3(d)), the upper part of the circuit is used for the Q path, while the lower part is for the I path. In our proposed configuration, the input I and Q signals are alternated between the upper and lower parts of the complex filter by the SEL signal, so that it is equivalent to the conventional configuration when the circuits in both configurations are ideal with the same transfer function given by

$$H(z) = \frac{1}{z-j}. \tag{4}$$

Fig.4 shows the complex bandpass ΔΣAD modulator with two proposed complex filters. We have eliminated two MUXs from the back end of the first-stage filter and the front end of the second-stage filter, so that there are no signal crossing lines from DACs at the second-stage filter. We have also added MUXs to change the sign for inputs of DAC3 and DAC4 to keep the signal flow the same as that of the conventional modulator. As a result, only two MUXs are used to change the I and Q signals at the inputs and outputs of the modulator. The complex filter in the modulator can be divided into two separate parts without signal line crossing between the upper and lower paths, and its layout design can be simplified. Furthermore, the two sets of signal paths and circuits in the modulator are changed between I and Q when CLK is changed. Symmetric circuits are used for I and Q paths at a certain period of time, and they are switched by multiplexers to those used for Q and I paths at another period of time. Therefore, the effect of mismatches between I and Q paths is reduced by dynamic matching.

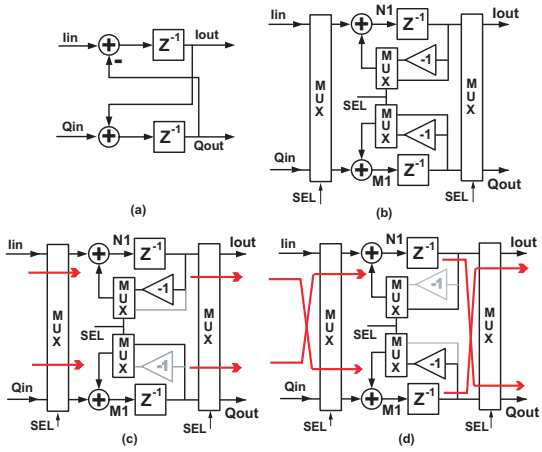

Fig. 3. (a) Basic complex bandpass filter. (b) Proposed equivalent implementation of a complex bandpass filter. (c) Operation of the proposed complex bandpass filter (state 1). (d) Operation of the proposed complex bandpass filter (state 2).

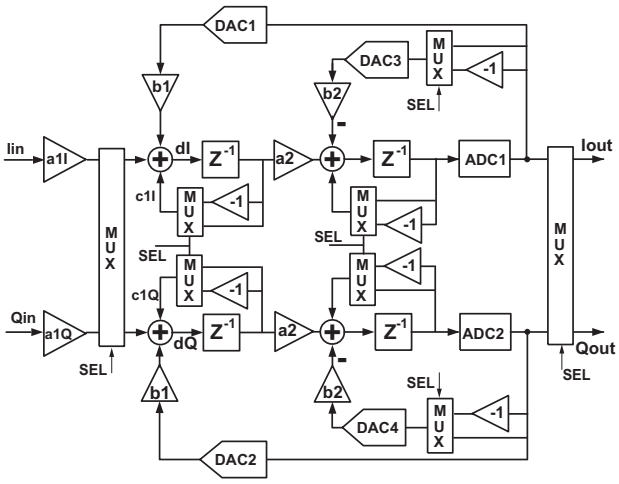

Fig. 4. Complex bandpass ΔΣAD modulator with proposed complex filter.

TABLE I

PARAMETERS FOR MISMATCHES BETWEEN I AND Q PATHS.

a1I=1×(1-0.03)	a1Q=1×(1+0.03)
c1I=3×(1+0.014)	c1Q=3×(1-0.03)
dI=1/3×(1-0.03)	dQ=1/3×(1+0.02)

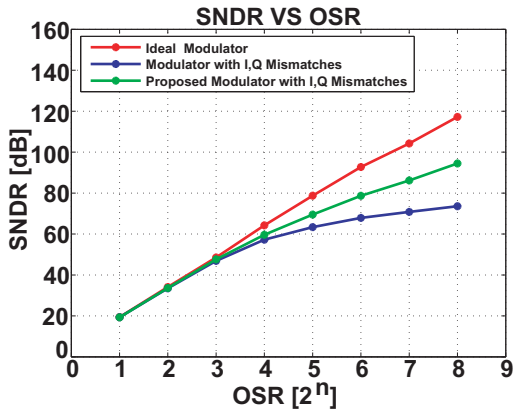

Fig. 5. Comparison of SNDRs of modulators with ideal DACs in three cases (parameters are those in Table 1).

We have conducted MATLAB simulations to evaluate the effectiveness of the proposed architecture. Second-order complex bandpass modulators with internal ADCs/DACs of 9-level resolution (in Fig.2 and 4) were used for the simulation with the following three cases:

1) An ideal modulator (in Figs.2 or 4) without mismatches and nonlinearities.
2) A modulator in Fig.2 with I and Q path mismatches whose parameters are shown in Table I. Since the effect of mismatches in the second-stage filter is smaller, we form mismatches only for the first-stage filter in our simulation.
3) A modulator that employs the proposed architecture (in Fig.4) and whose mismatches and nonlinearities are the same as those in case 2.

Fig.5 shows the simulation result comparison for the SNDRs of the modulators in these three cases. In case 1, the SNDR of the ADC increases as OSR increases. However, in case 2 (where mismatch parameters between I and Q paths are shown in Table I), SNDR saturates as OSR increases. On the other hand, in case 3, SNDR improves because the mismatch effects are taken out of the signal band by dynamic matching.

IV. COMPLEX BANDPASS DWA ALGORITHM

In ΔΣAD modulators, oversampling and noise shaping techniques are used to achieve high accuracy. When a single-bit modulator (i.e., internal ADC and DAC are 1-bit) is used to achieve a high SNDR, a higher OSR is needed, which demands a higher sampling rate, and/or a high-order filter inside a modulator (as well as a high-order digital filter following the ΔΣAD modulator) is required, which may cause modulator stability problems. On the other hand, when multibit ADCs/DACs are used inside the modulator, it can obtain a high SNDR with a low-order loop filter and improve the stability problem. Smaller steps

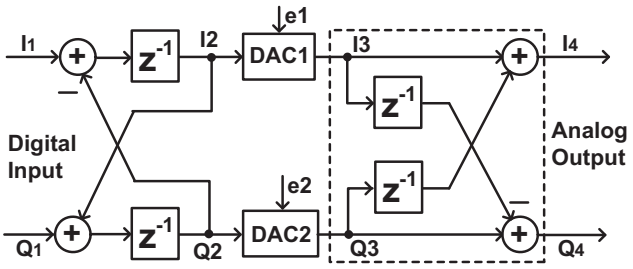

Fig. 6. Proposed architecture of DAC nonlinearity noise shaping for a complex bandpass modulator. I1 is the I-channel ADC output and Q1 is the Q-channel ADC output, while I4 is the I-channel DAC output and Q4 is the Qchannel DAC output. e1 and e2 denote the nonlinearities of DAC1 and DAC2, respectively. Note that this architecture cannot be implemented directly.

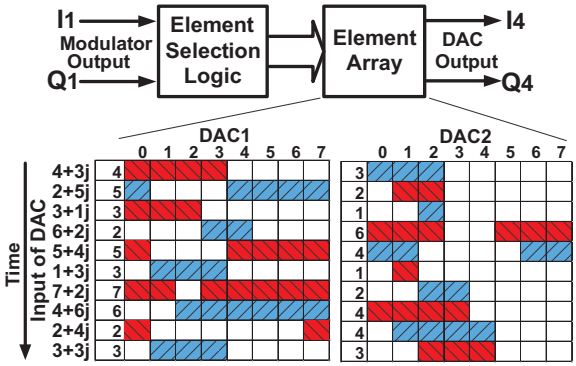

Fig. 7. Explanation of our complex bandpass DWA algorithm. The unit current cells in the ON state are filled in black for a real part (I-path) and in gray for an imaginary part (Q-path), when the complex input data are sequentially given by 4+3j, 2+5j, 3+j, 6+2j, ...

of the quantizer result in a lower quantization error, and relax the required performance for opamps with a larger overload level.

A multibit DAC cannot be made perfectly linear, while a 1-bit DAC is inherently linear. Multibit DAC nonlinearity is equivalent to errors added directly to the input signal - it is not reduced by noise shaping, and hence they may degrade the SNDR of the $\Delta\Sigma$ADC. In our implementation, multibit ADCs/DACs are used. Each DAC in our modulator has a nine-level resolution with the segmented switched-capacitor architecture. Nonlinearities of the DAC due to mismatches of capacitors introduce errors in the feedback loop and appear directly at output; this results in an almost flat power spectrum in the entire band, and the SNDR of the modulator degrades.

We proposed a new noise shaping algorithm to reduce the effects of nonlinearities in multibit DACs of complex bandpass $\Delta\Sigma$AD modulators. Fig.6 shows our proposed architecture for complex bandpass noise shaping of DAC nonlinearities. It consists of a digital complex bandpass filter at the front end, two DACs, and an analog complex band elimination filter at the back end. The transfer function of the digital complex bandpass filter at the front end is the same as Eq.(4), whereas the transfer function of the analog complex band elimination filter at the back end is given by

$$H(z) = 1 - jz^{-1}. \tag{5}$$

Therefore, the nonlinearity errors of the two DACs $e1 + je2$ can be noise-shaped in a complex form at $f_s/4$, the notch of Eq.(5). In practice, however, this structure cannot be realized because the input signals may be infinite (out of DAC input range). Thus, the equivalent implementation called the complex DWA algorithm is proposed to realize the architecture of DACs shown in Fig.6.

Our implementation uses only a digital filter at the front end of 2-channel DACs and does not require an analog filter at the back end. Element selection logic circuits (DWA1 and DWA2) are added between the two ADC outputs and DAC inputs to select the DAC unit elements in a rotational manner [7] as shown in Fig.7. For the I-channel DAC output I_4, we apply a *highpass* DWA algorithm [11] with internal interaction between I and Q modulator outputs. For the Q-channel DAC output Q_4, we apply a *lowpass* DWA algorithm [12] with internal interaction between I and Q modulator outputs. DAC1 and DAC2 are used alternately for I and Q-channels; hence, mismatch effects between two DACs $e1 + je2$ are first-order complex bandpass noise-shaped at $f_s/4$. Our algorithm can be implemented using simple circuitry; analog and digital multiplexers, barrel shifters and adders/subtractors.

V. Circuit Implementation

Fig.8 shows the entire proposed complex bandpass $\Delta\Sigma$AD modulator. We see that the proposed second-order complex bandpass filter, which shares several MUXs, is used so that the proposed modulator has no crossing signal lines for either the forward paths of the z^{-1} block or the feedback paths from DACs. Hence, the proposed modulator can be completely divided into two separate parts and its layout design can be greatly simplified. Then its internal signal lines can be shorter, which leads to a smaller chip area.

For the proposed architecture, we note that MUXs can be easily realized using MOS switches. We add MUXs that alternate the polarity of the feedback signals between +1 and –1 at every sampling time to the feedback paths of filters and DACs. This maintains the polarity of internal complex signals so that they are processed as a complex signal form [14]. In fact, we can realize this by simply chopping the two differential outputs at every sampling time.

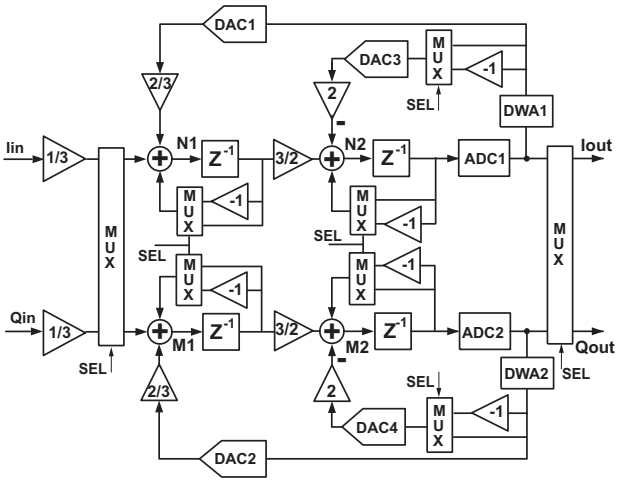

Fig. 8. Architecture of our complex bandpass ΔΣAD modulator.

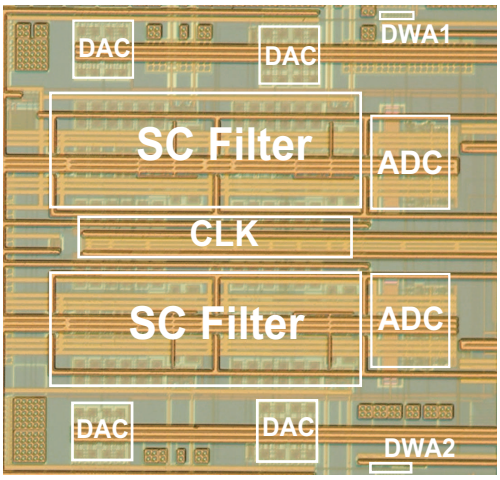

Fig. 9. Chip photopragh.

The proposed modulator was designed with fully differential switched capacitor circuits. z^{-1} block in the modulator realized by using a switched-capacitor delay cell [13]. Gate-boosted NMOS switches and dummy switches are used at the input sampling parts to cancel the effect of charge injection and clock feedthrough, while the rest of the elements are CMOS switches. $ck1$ and $ck2$ are nonoverlapping clocks to minimize the charge injection caused by sampling switches. Latched comparators with input offset storage are used in the flash-type nine-level ADCs, where offset cancellation is applied to both the preamplifier and the latch.

VI. Experimental Results

The proposed complex bandpass ΔΣAD modulator was fabricated using 1P6M 0.18μm CMOS technology without any option for precision capacitors and low threshold voltages. Fig.9 shows its chip microphotograph; the core size is 1.4 × 1.3 mm^2. The capacitors were realized using multiple unit-capacitor cells for accurate ratio matching of coefficients. Unit-capacitor cells were realized using the MIM structure for high capacitance density in a small chip area.

Fig.10 shows a comparison of the output power spectrum results of the modulator for zero input between ON and OFF states of DWA logic. We see that while DWA logic is in the ON state, the noise floor at the band of interest is about 3dB lower than that when DWA logic is in the OFF state; this validates the effectiveness of the proposed algorithm.

Fig.11 shows the measured output power spectrum for a 4.92MHz sinusoidal input, where the sampling frequency of CLK was 20MHz, and the reference voltages of the modulator were fixed at $V_{ref+} = 1.9$V and $V_{ref-} = 0.9$V. The degree of the mirror image signal suppression in the modulator was evaluated by demodulating the complex IF signal down to the baseband with quadrature carriers in the digital domain and performing an FFT on the resulting complex-valued signal. The spectrum of the demodulated, complex-valued baseband signal is shown in Fig.12 which just shifts the center of the signal band from fs/4 to DC in the frequency domain; the scale of the frequency axis is expanded around DC and the value of the power spectrum is the same as that in Fig.11. It is observed that the image signal is suppressed by 46dB with respect to the desired signal. Fig.13 shows SNDR vs OSR; the peak SNDR is 64.5dB. Clocked at 20MHz, the modulator consumes 28.4mW at a power supply voltage of 2.8V.

VII. Conclusion

We have designed, fabricated and tested a second-order multibit switched-capacitor complex bandpass ΔΣAD modulator to demonstrate the effectiveness of two new algorithms:

1) A complex bandpass filter with I, Q dynamic matching to reduce the effect of mismatch between I and Q paths. The complex filter in the modulator can be divided into two separate parts without requiring sensitive signal lines of the upper and lower paths to cross.
2) A new complex bandpass DWA algorithm is implemented to suppress nonlinearity effects of multibit DACs in complex form.

The effectiveness of the proposed architecture and circuit technique has been demonstrated by measured results.

Acknowledgment

The authors would like to thank STARC which supported this research. Thanks are also due to T. Kozawa, E. Imaizumi, H. Sugihara, I. Sakurazawa H. Konagaya, F. Xu and K. Wilkinson for valuable discussions. A part of this work was performed at Gunma University Advanced Technology Research Center and Incubation Center.

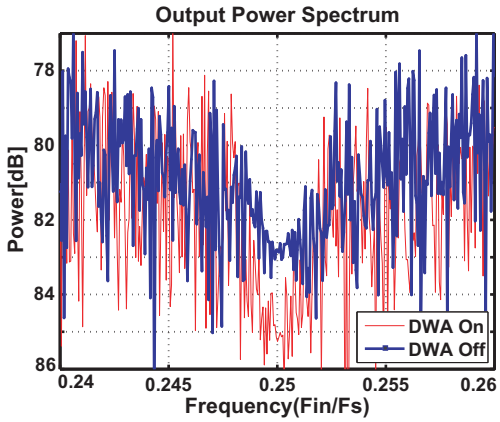

Fig. 10. Comparison of power spectrum bwtween DWA on and off.

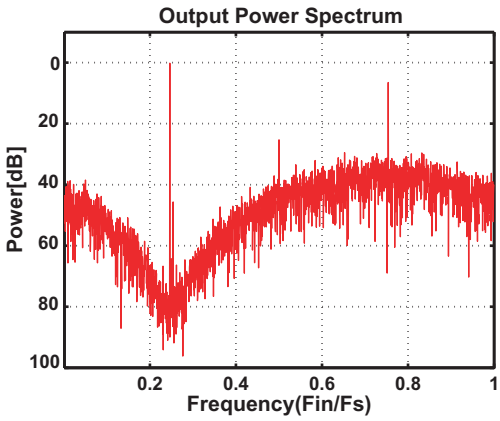

Fig. 11. Measured output power spectrum of the proposed modulator.

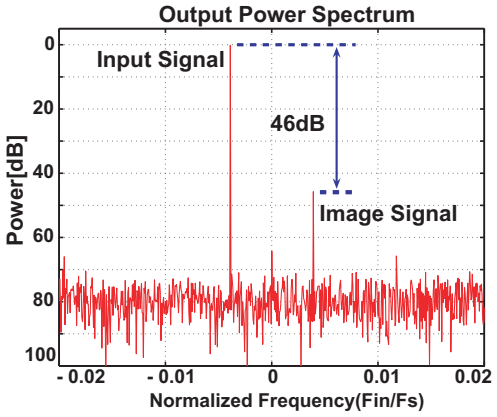

Fig. 12. Measured output power spectrum of the proposed modulator.

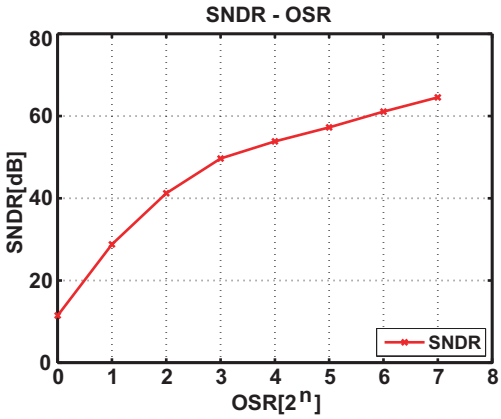

Fig. 13. Measured SNDR vs OSR of the proposed modulator.

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