Delta-Sigma ADC Architecture for Power Meter Application

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Abstract

This paper proposes novel ΔΣADC architecture for power meter application. ΔΣAD modulator realizes high resolution by oversampling and noise shaping technique, which is suitable for high resolution measurement application. However, its SNDR (Signal to Noise and Distortion Ratio) is limited by the dynamic range of the input signal and non-idealities of building blocks, particularly by the harmonic distortion in amplifier circuits. Compared with a feedbacked ΔΣAD modulator, in a full feedforward ΔΣAD modulator structure, the signal transfer function is unity under ideal circumstances. It means that the signal swings through the loop filter become smaller. Therefore, the harmonic distortion generated inside the loop filter can be significantly reduced because the effect of non-idealities in amplifiers can be suppressed when signal swing is small. Moreover, the reduction of the internal signal swings also relaxes output swing requirement for amplifiers in low-voltage design. However, in conventional feedforward ΔΣAD modulator, an analog adder is needed before quantizer. Especially in a multibit modulator, an additional amplifier is necessary to realize the summation of feedforward signals, which leads to large chip area and extra power dissipation. In this paper, we propose a novel architecture of a feedforward ΔΣAD modulator. It realizes the summation of feedforward signals without additional amplifier that is equivalent to the conventional one but smaller chip area and low-power dissipation. We also conducted MATLAB and SPICE simulations to verify the proposed architecture and modulator circuits.

I. Introduction

As an interface between the analog world and the digital domain, the ADC (Analog-to-Digital Converter) is widely used for mesurement appilication such as power meter. The perfomance of ADC in power meter are required for higher accuracy, lower power dissipation and large dynamic range. However, in deep-submicron CMOS technology, the decrease of the supply voltage evidently degrades the accuracy of ADC. ΔΣAD modulators realize high resolution by oversampling and noise shaping technique, which are the most suitable for high resolution application in the deep-submicron CMOS technology. The performance of ΔΣAD modulators is limited by dynamic range of input signal and non-idealities of building blocks. In nano-meter CMOS technology, the performance of analog circuits is greatly degraded because the devices mismatch grows much with scaling down. Therefore, non-idealities of building blocks, especially non-linearities of amplifiers generate more harmonic distortion. Furthermore, since signal swings are reduced due to lower supply voltage, the dynamic range will be decreased for the same noise floor, and the performance of the modulator is degraded. Circuit level challenge for high resolution with low-voltage operation is limited in the nano-meter CMOS technology. The best solution for the problems is at system level. By applying direct feedforward of input signal to a quantizer, the signal swings in the modulator are significantly reduced. Hence the drawbacks of ΔΣAD modulators can be overcome.

II. Feedback & feedforward ΔΣAD modulators

Figs.1 and 2 show second-order feedback and feedforward ΔΣAD modulators respectively. They have similar structure with two integrators, ADC and DAC, but their signal paths are different.

- **Feedback ΔΣAD modulator**

The input and output of the feedback ΔΣAD modulator shown in Fig.1 can be expressed as

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^2 E(z) \tag{1}$$

Here $X(z)$ is input signal, $Y(z)$ is output signal and $E(z)$ is quantization noise of the modulator. Then the signal transfer function (STF) and noise transfer function (NTF) of the modulator are given by

$$STF(z) = z^{-2} \tag{2}$$

$$NTF(z) = (1 - z^{-1})^2. \tag{3}$$

The NTF provides a second-order noise-shaping function for the quantization noise of the modulator. The feedback architecture is the most commonly used topology to ΔΣAD modulators. The output signals of the first and second integrators, y_1 and y_2 are as follows:

$$y_1 = z^{-1}(1 - z^{-1})X(z) - z^{-1}(1 - z^{-1})E(z) \tag{4}$$

$$y_2 = z^{-2}X(z) - z^{-1}(2 - z^{-1})E(z) \tag{5}$$

From Eqs.(4) and (5), we see that the output signals of two integrators y_1 and y_2 are the functions of $X(z)$, the input signal to the modulator. Then the signal swing at the output of amplifiers becoming large which makes their implementation in

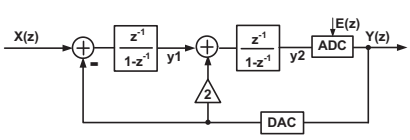

Fig. 1. Second-order feedback ΔΣAD modulator.

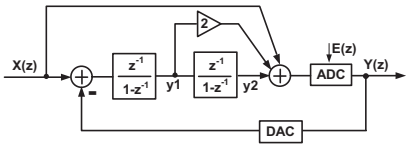

Fig. 2. Conventional second-order feedforward ΔΣAD modulator.

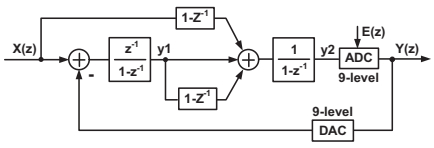

Fig. 3. Proposed second-order feedforward ΔΣAD modulator.

the low-voltage more difficult. The harmonics generated by the amplifier non-linearities also depends on the signal swing of integrator, which severely reduces the SNDR of the modulator with feedback topology.

- **Feedforward ΔΣAD modulator**

The input and output of the feedforward ΔΣAD modulator shown in Fig.2 can be expressed as

$$Y(z) = X(z) + (1 - z^{-1})^2 E(z) \quad (6)$$

$$STF(z) = 1 \quad (7)$$

$$NTF(z) = (1 - z^{-1})^2. \quad (8)$$

Compared with feedbacked ΔΣAD modulator shown in Fig.1, the NTF given by Eq.(8) is the same as Eq.(3), while the STF is unity under ideal circumstances and not delayed. The output signals of the first and second integrators, y_1 and y_2 are as follows:

$$y_1 = -z^{-1}(1 - z^{-1})E(z) \quad (9)$$

$$y_2 = -z^{-2}E(z). \quad (10)$$

Throuth Eqs.(9) and (10), we see that the output signals of two integrators y_1 and y_2 are free of the input signal $X(z)$, which means that the feedforward ΔΣAD modulator processes quantization error only [1], [2]. Therefore, the signal swings passing through the integrator are smaller and the distortion generated by the non-linearities effect of the amplifiers is input signal independent. It can be significantly reduced. Furthermore, in this topology, the signal amplitude of the amplifiers is reduced and that eases implementation of amplifier design. Hence, it is more suitable for low-power applications.

III. Proposed Novel Feedforward ΔΣAD modulator Architecture

Note the summation point of feedforward paths in front of the quantizer in Fig.1(b), an adder circuit is necessary to realize all the feedforward signals summed together, which creates complication for full feedforward ΔΣAD modulators. In some implementations, this adder is realized by passive switched-capacitor network. However, this approach reduces the signal level into the quantizer and it is only suitable for single-bit implementation. In a multibit implementation of the full feedforward ΔΣAD modulators, the switched-capacitor adder is used and a weighted summation amplifier is required before the quantizer [3], that leads to increased circuit complexity, large chip area and extra power dissipation [4], [5]. Some ideas have been proposed to solve this problem. However, they require a distributed DAC-feedback [4] or high-order(≥3rd-order) loop filter [4], [5]; which significantly increases the complexity of the analog circuit to implement the modulator. We propose here a novel architecture of feedforward ΔΣAD modulators. It is a single DAC-feedback, second-order ΔΣAD modulator without an additional amplifier. Circuits' complexity is reduced and it is more suitable for low-power applications.

Fig.3 shows the proposed architecture of feedforward ΔΣAD modulator. It is a 3-bit second-order structure with single-loop single-DAC-feedback topology. To get higher SNDR with low-power dissipation, proposed modulator has following features:

- **One amplifier saving:** Compared with the conventional feedforward modulators shown in Fig.2, in our proposed novel architecture, we moved the summation point of feedforward path from input node of quantizer to the input node of the second-stage loop filter. The feedforward signals can be merged into the output of the first integrator, then fed to the second stage. By this way, the amplifier in second stage can be shared to realize signal summation and integration. Therefore, circuits' complexity is reduced by not requiring an additional weighted summation amplifier before the quantizer.
- **Lower-order loop filter and multibit architecture:** Second-order loop filter reduces the complexity of the analog circuit and power dissipation. Multibit quantizer not only reduces quantization noise, but also relaxes the required slew rate of amplifier in the filter. Therefore, the modulator becomes more linear, stability is improved and power dissipation is lower also[6].
- **Single DAC-feedback and single-loop topology:** Furthermore, with a single DAC-feedback, a single-loop topology, rather than a distributed DAC-feedback [7], a cascaded architecture [8], the complexity of the analog circuit and DAC linearization in the ΔΣ modulator is reduced, and modulator is much less sensitive to the finite dc gains of the amplifiers. They are more suitable for low-power dissipation.

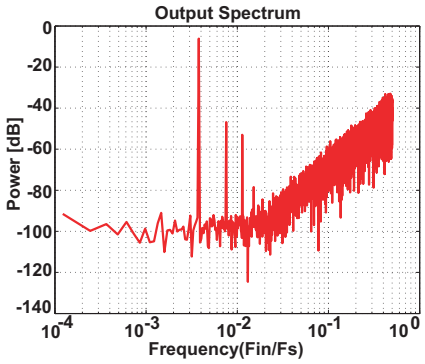

Fig. 4. Simulated output power spectrum of second-order feedback $\Delta\Sigma$AD modulator in Fig.1 with harmonic distortions.

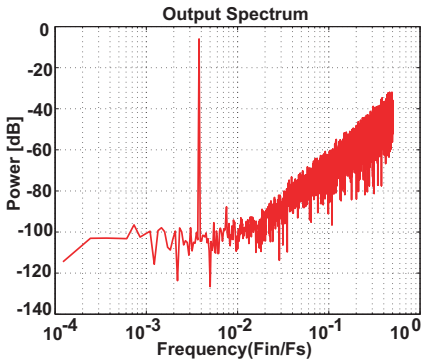

Fig. 5. Simulated output power spectrum of proposed second-order feedforward $\Delta\Sigma$AD modulator in Fig.3 with harmonic distortions.

The input and output transfer function, STF and NTF of proposed modulator are the same as Eqs.(6), (7) and (8). The output signals of the first and second integrators in proposed modulator, y_1 and y_2 are as follows

$$y_1 = -z^{-1}(1-z^{-1})E(z) \quad (11)$$

$$y_2 = X(z) - z^{-1}(1-z^{-1})E(z). \quad (12)$$

From Eqs.(11) and (12), we see that the output signal of first integrators y_1 is free for the input signal while the output signal of second integrator y_2 contains a input signal component. However, any non-idealities of the second integrator can be noise-shaped by feedback loop in the modulator, and their effects are not dominant for second order modulator [9]. It should be noted that the $(1-z^{-1})$ term in the feedforward path of proposed modulator can be implemented just by a simple capacitor.

Fig.4 shows the output spectrum of a feedback $\Delta\Sigma$AD modulator in Fig.1 including a nonlinear amplifier model with harmonic distortion. It is clear that the gain non-linearities of amplifiers cause large harmonic distortion and it appears at the output of the feedback $\Delta\Sigma$AD modulator. Fig.5 shows the output spectrum of a feedforward $\Delta\Sigma$AD modulator in Fig.3 including a nonlinear amplifier model with harmonic distortion. Compared with Fig.4, the same nonlinear gain coefficients are used, but it is clear that in our proposed feedforward modulator, the harmonic distortion is greatly suppressed.

From above discussion, it suggests that the proposed modulator can realize equivalent noise shaping function of conventional one with less hardware low-power dissipation and less sensitive to the non-idealities of amplifier, which is more suitable for nano-meter CMOS technology.

Fig.6 shows the full-differential switched-capacitor (SC) circuit implementation of the proposed feedforward $\Delta\Sigma$AD modulator with loop filters and feedback DACs. Parasitic-incentive switched-capacitors structures are used for integrators [10]. Negative capacitors in the modulator are easily implemented by changing the polarity of input signals in a fully differential circuit. Feedforward signals are summed at input node of the second stage integrator, and no more additional summation amplifier is necessary. The coefficients in Fig.3 are realized by the ratios of capacitors around the amplifier. In our proposed modulator, all coefficients are 1 which are easily implemented with the same capacitor size. Nine-level DAC are implemented by 8 capacitors which unit size is 1/8 of the input sampling capacitor. Therefore, the size of all capacitors can match well.

IV. Simulation Results and Conclusion

We have conducted MATLAB and SPICE simulations to verify the proposed architecture and the modulator circuits. Matlab behavioral model is shown in Fig.3 and SPICE behavioral circuit is shown in Fig.6.

In SPICE simulation, ideal amplifiers and switches are used. The values of capacitors are shown in Fig.6. We assume that supply voltage is $V_{dd} = 1.8V$, reference voltages are $V_{refp} = 1.8V$, $V_{cm} = 0.9V$ and $V_{refm} = 0V$, input signals are differential sine waves that $V_{pp} = 1.0V$ and offset at 0.9V. Fig.7 shows SPICE simulation results of two integrators' output waveform respectively. The output voltage of both integrators is in a range of 0 to V_{dd}, which means that the two amplifiers work well without any saturation. Especially, the output voltage swing of the first integrator is very small; it eventually reduces the power consumption and simply eases the amplifier design in a low voltage. We also made the simulation results comparison between MATLAB and SPICE. Fig.8 shows compared simulation results of output spectrum, and Fig.9 shows compared results of SNDR-OSR. The SPICE behavioral results are similar to MATLAB simulated results. It suggests that the proposed circuit realizes the noise shaping as well as proposed at system level.

As a result, we have proposed novel feedforward architecture and its implementation circuits of a second-order $\Delta\Sigma$AD modulator. In our proposed novel architecture, an amplifier can be shared so that the circuits' complexity can be reduced. It suggests small chip area and low-power dissipation. MATLAB and SPICE simulations results show the efficiency of proposed architecture and modulator circuits.

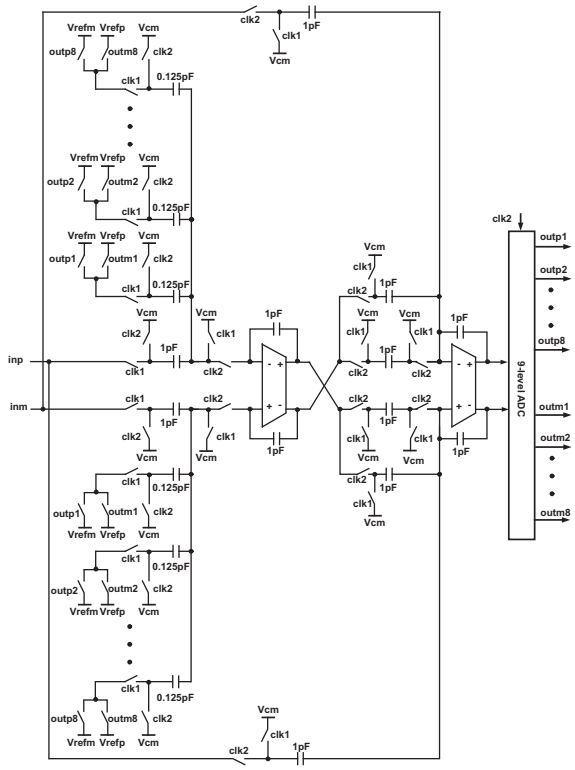

Fig. 6. SC implementation of proposed feedforward ΔΣAD modulator.

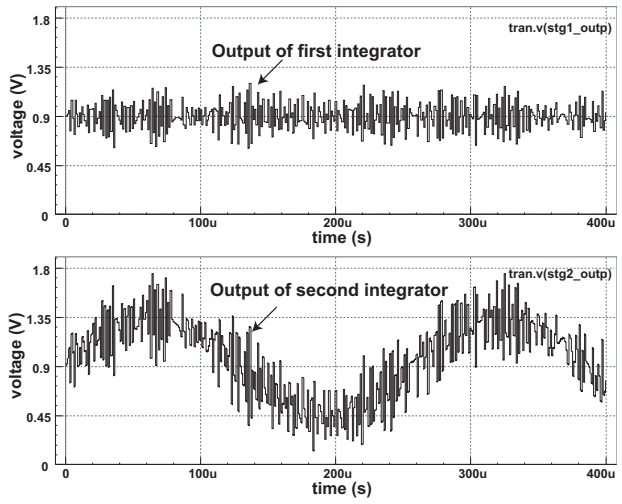

Fig. 7. SPICE simulation results of integrator outputs in proposed ΔΣAD modulator.

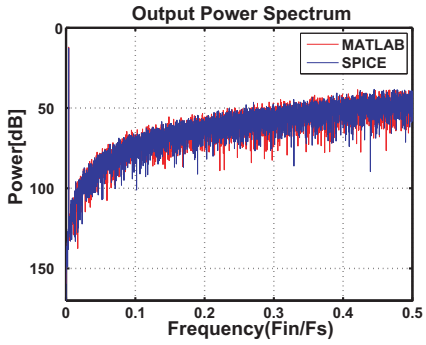

Fig. 8. Compared output power spectrum of proposed multibit ΔΣAD modulator.

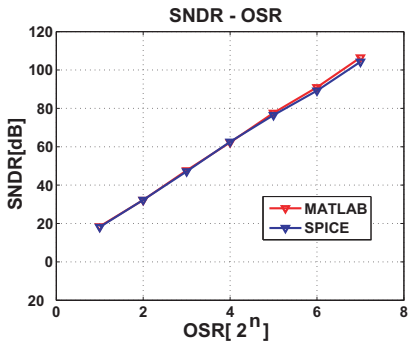

Fig. 9. Compared SNDR-OSR of proposed multibit ΔΣAD modulator.

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