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A High-Speed 6-Bit ADC Using SiGe HBT

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SUMMARY This paper describes the design and performance of a high-speed 6-bit ADC using SiGe HBT for measuring-instrument applications. We show that the Gummel-Poon model suffices for SiGe HBT modeling and then we describe that the folding/interpolation architecture as well as simple, differential circuit design are suitable for ADC design with SiGe HBT. Measured results show that the nonlinearity of the ADC is within $\pm 1/2LSB$, and the effective bits are 5.2 bits at an input frequency of 100 MHz and 4.2 bits at 200 MHz with 768 MS/s. We also describe some design issues for folding/interpolation ADC.

key words: *A/D converter, folding/interpolation, analog circuit, SiGe HBT, modeling*

1. Introduction

Electronic devices are continuously getting faster, and accordingly there is a growing need for instruments to measure their performance. We describe here the design and measured results of a high-speed 6-bit Analog-to-Digital Converter (ADC) implemented with SiGe Heterojunction Bipolar Transistor (HBT) process. SiGe HBT has potentially higher f_T than Si Bipolar Junction Transistor (Si BJT) while providing the similar advantages such as large g_m, good device matching, good yield and relatively low cost. Recent SiGe HBT research activity has covered the SiGe HBT process, device and circuit technology [1], [2]. We consider that this SiGe HBT technology is a good candidate for very high-speed ADCs for measuring-instrument applications, and we have designed and fabricated a 6-bit folding/interpolation ADC chip with an *in-house* SiGe HBT process to investigate its technological potential.

Section 2 provides a comparison of high-speed ADCs using CMOS, GaAs MESFET, GaAs HBT, Si BJT and SiGe HBT processes, and Sect. 3 describes the SiGe HBT process and modeling. Section 4 presents the ADC design while Sect. 5 describes some measurement results.

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2. Technology Comparison for High-Speed ADC System

There are several technology candidates for implementing very high-speed (>GS/s) ADC systems; CMOS is the most dominant semiconductor technology, but the speed of CMOS ADCs is currently limited to $\approx$ 200–300 MS/s even for 6-bit resolution See, e.g., [3]. GaAs MESFET has very high f_T, i.e., high-speed, but the poor device matching and relatively small g_m are disadvantages for our purposes. Si BJT has high f_T, good device matching and large g_m, so are suitable for a high-speed ADC and there are many examples of successful high-speed Si BJT ADCs [4]–[6]. However the speed limit of Si BJT has been addressed and attention is being paid to HBT technology for making even faster devices and circuits [1], [2], [7]. Recently very high-speed ADCs with GaAs HBT were introduced [8], [9], and we reported on an ADC with this technology [10], [11]. Advantages of GaAs HBT are high f_T (higher than Si BJT), large g_m, and good device matching, while disadvantages are low yield, large $V_{be}(\approx 1.4\,\mathrm{V})$, thermal problems and high cost. On the other hand, SiGe HBT has potentially higher f_T than Si BJT (but lower than GaAs HBT) and the other characteristics are similar to Si BJT (i.e., relatively easy to use, unlike GaAs HBT).

Based on the above considerations, we have used SiGe HBT to investigate the potential for high-speed ADC systems.

3. SiGe HBT Process and Modeling

In our SiGe HBT process, npn transistors, thin-film

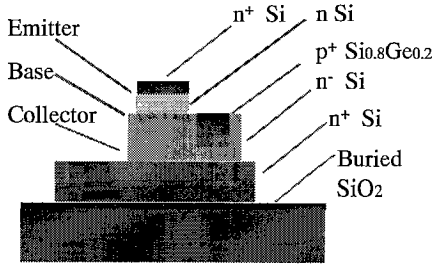


Fig. 1 Cross section of SiGe HBT.

resistors, metal-insulator-metal capacitors and double metal for interconnection are available. Figure 1 shows the cross section of our HBT.

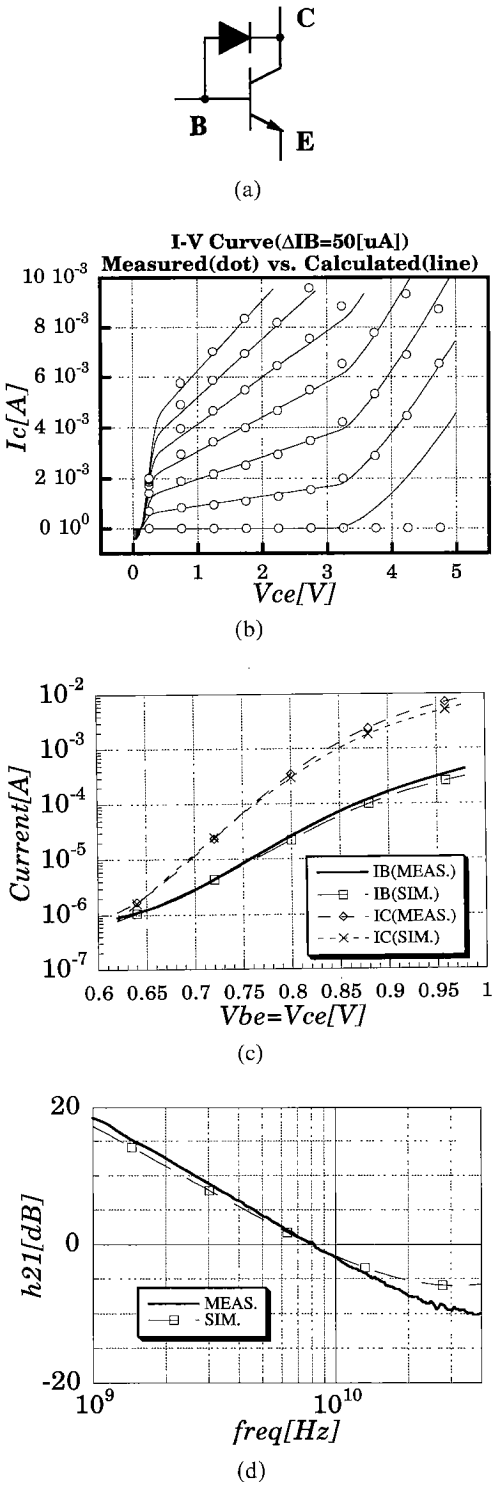


Fig. 2 SiGe HBT simulation and measured result comparison. (a) A diode is added between base and collector to represent the breakdown voltage of SiGe HBT. (b) $V_{ce} - I_c$ characteristics with the parameter of I_b. (c) V_{be} vs. I_c, and V_{be} vs. I_b. (d) AC characteristics.

We have used, as our HBT model, a bipolar transistor with Gummel-Poon model and a diode between its base and collector to represent the breakdown voltage of the HBT (Fig. 2 (a)). We found that the calculated device parameter values, based on doping concentration and device geometry, and the extracted parameter values matched well, and the circuit simulation and measurement results matched fairly well in all aspects of DC, AC and transient behaviors; Fig. 2 (b) shows the $V_{ce} - I_c$ plot with varying I_b while Fig. 2 (c) shows the Gummel plot and h_{FE} is ≈ 20. Figure 2 (d) shows the frequency characteristics and f_T is about 8 GHz. The simulated oscillation frequency of a ring oscillator was 386 MHz while the measured frequency was 350 MHz. We see that, unlike GaAs HBT which has several different characteristics from Si BJT, the basic Gummel-Poon model suffices for our SiGe HBT modeling.

4. ADC Design

A. Design Philosophy: Our SiGe HBT is in the development phase and so far it is not mature technology. We are trying different device structures; some wafers have used abrupt-junction-base structure while others have used graded-base structure. Also some have used silicon substrate while others have used SIMOX substrate. Hence their parameters can differ significantly; f_T was 8 GHz on the test wafer from which SPICE parameters were extracted while actual f_T of the HBT in the ADC reported here is now $\approx$ 20 GHz. (The ADC was fabricated in SiGe HBT process with abrupt-junction-base structure and SIMOX substrate.) Also yield and device matching are so far not consistent. Circuit design methods for such devices are quite different from those for mature technologies such as CMOS and Si BJT. We use robust circuit design and do not use fancy circuitry, and the architecture is designed for minimum hardware. Our first priority is a functional ADC chip and the second is high-speed. So far low-power design is not our major concern.

B. ADC Architecture Design: The ADC employs the folding/interpolation architecture [5], [12], [13] to reduce hardware and power (about 1/3 of the flash ADC) while maintaining high-speed operation. A differential resistor string is used in the ADC input stage (Fig. 3 (a)) to cancel the reference DC bowing effects [12], [14]. The folding circuits perform analog encoding and generate G5 (MSB) and G4 of Gray code and O/U (overflow/underflow) bit (Fig. 3 (b)) [15]. Four sinusoidal wave generators (Fig. 3 (c)) and the resistor interpolation circuit (Fig. 3 (d)) produce sixteen sinusoidal waves with different phases with respect to the input voltage. Following the interpolation circuit, XOR-tree type digital encoder circuits generate lower 4 bits (G3, G2, G1, G0 (LSB)) of Gray code from $M_0, \ldots M_f$ in Fig. 3 (d). We note that Gray code reduces the metastability effects of the latched-comparators [12],

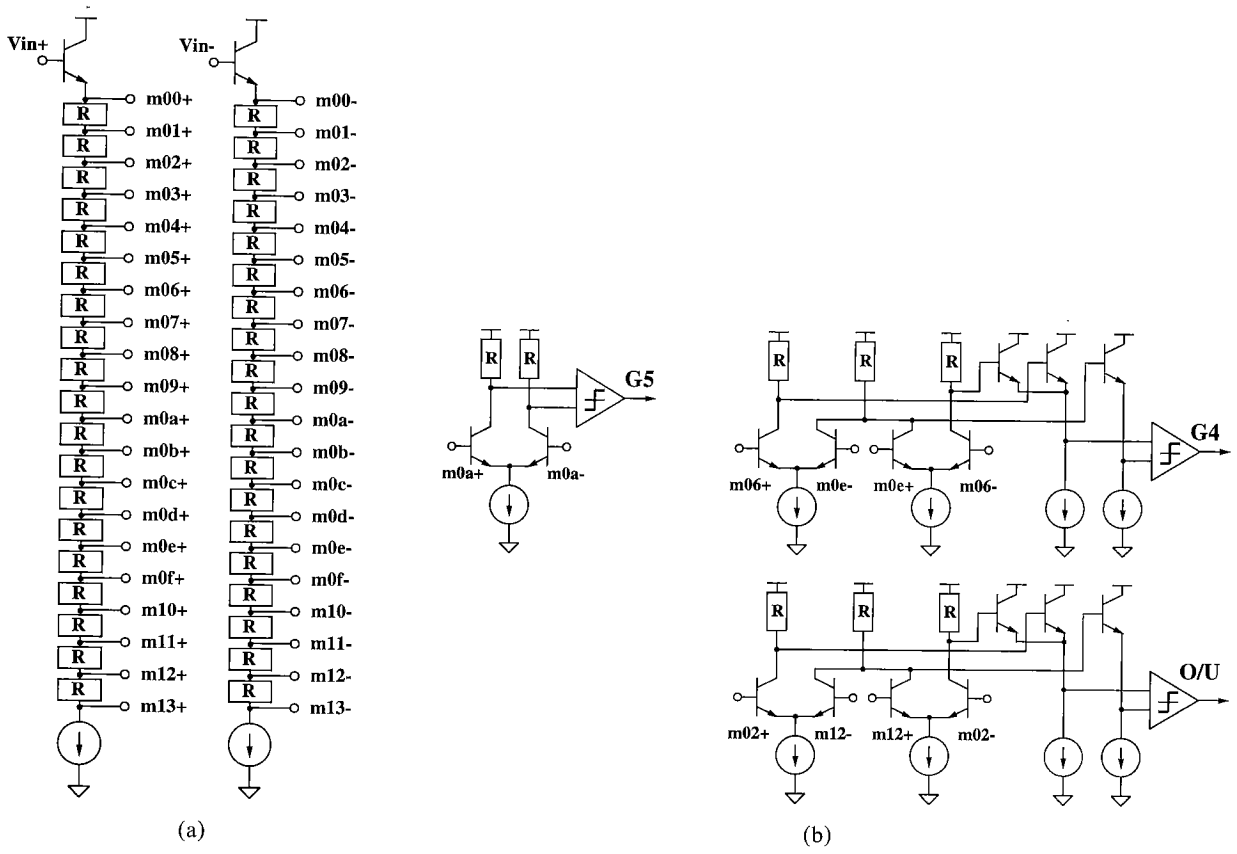


Fig. 3 ADC circuits. (a) Differential resistor string. (b) Folding circuits which generate $G5$, $G4$ and O/U.

[14].

All of the internal signals are differential, and all of the internal analog and digital circuits are basically composed of differential pairs and emitter followers, while the digital outputs are single-ended (open-collector). Several design issues for folding/interpolation ADC are described in the follwoing.

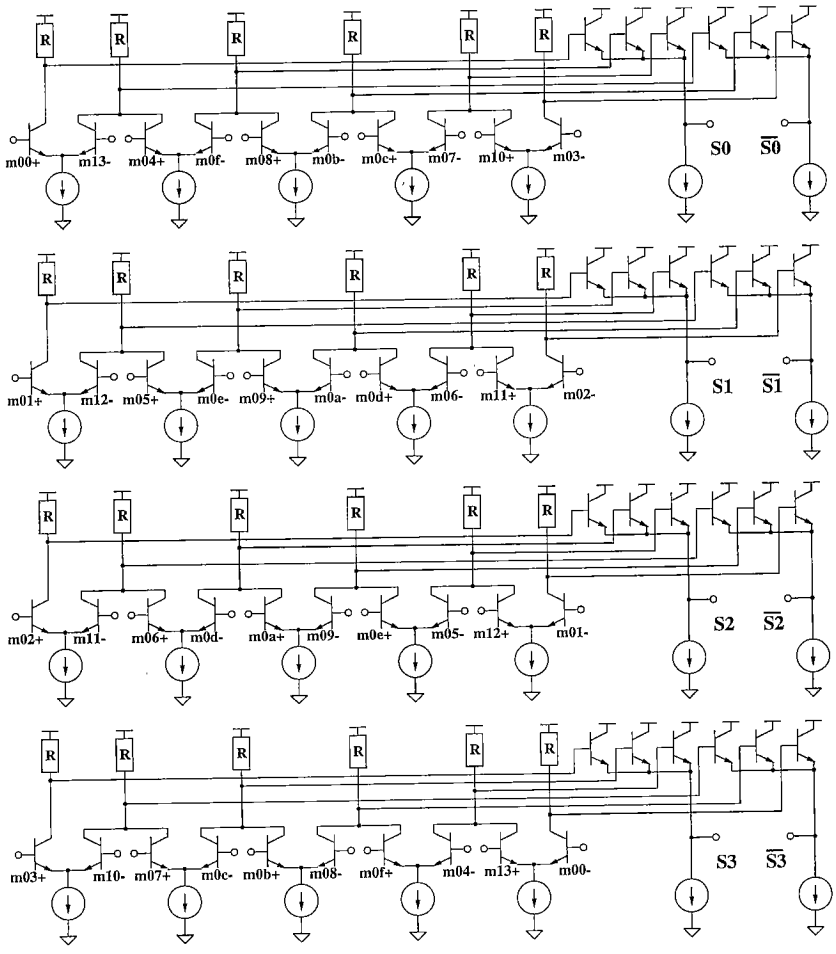
C. Analog and Digital Encoding: In our 6-bit ADC, MSB and MSB-1 are generated by analog encoding (folding circuit) while the other lower 4-bits are generated by digital encoding (interpolation circuit). Also the 6-bit folding ADC in [8] uses the similar configuration. For most of 8-bit folding ADCs [17], [19], [20], MSB, MSB-1 and MSB-2 are generated by analog encoding while the other lower 5-bits are generated by digital encoding. Flash ADCs may be considered that their all bits are generated by digital encoding. Qualitatively speaking, as the number of bits by analog encoding increases, the hardware and power of the ADC decrease while the analog encoding circuit generates higher frequency signals which may degrade the ADC high frequency performance. However in many cases the configuration of analog and digital encoding in folding ADCs may be decided by design experiences and its quantitative design methodology is left for future work. We close this section by remarking that the AC performance of the folding/interpolation ADCs may be degraded by the high frequency signal generated by analog encoding, however the interpolation circuit reduces the ADC input capacitance, which gives a positive impact on the AC performance. Hence in some cases the folding/interpolation ADC can have better AC performance than the flash ADC [7].

D. High Speed Differential Resistor String: The differential resistor string in the ADC input stage (Fig. 3 (a)) is known to cancel the reference DC bowing effects [14]. However we have found that this circuit has a disadvantage for high-speed operation: the input signal goes through the buffer and propagates an RC delay line where R is the unit resistor of the resistor string and C is the input capacitance of the comparator. The propagation time t_{pd} to reach at the end of the resistor string is given by

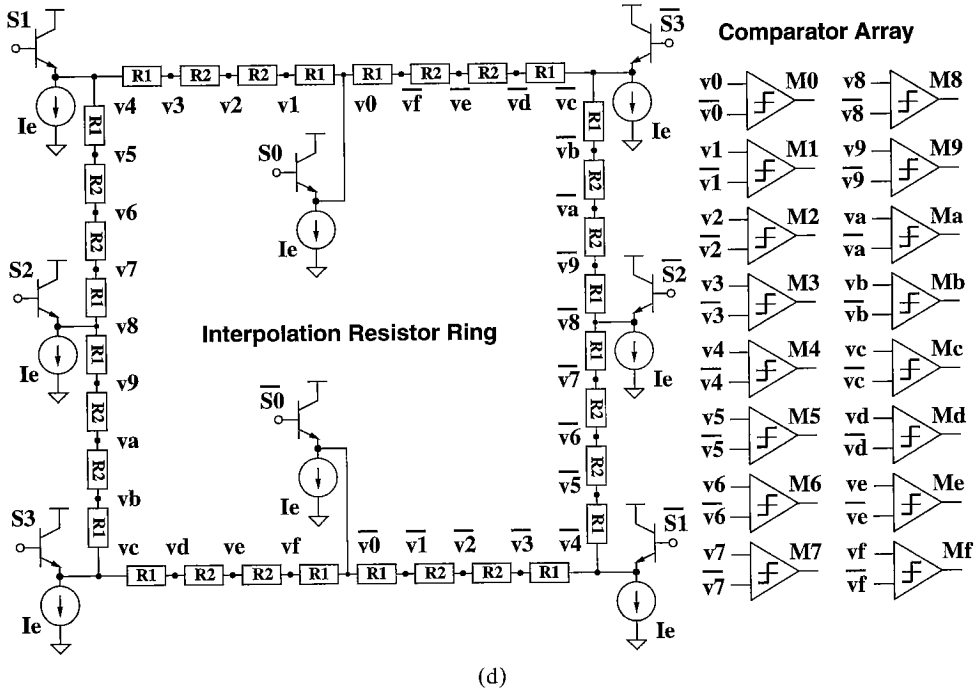
$$t_{pd} \approx KN^2RC,$$

where K is a constant and N is the number of comparators connected to the resistor string [16]. We propose using the circuit shown in Fig. 4, where the resistor string is driven from both sides†. The propagation time

†This time the proposed circuit is not used in the ADC chip, but in the next ADC design, we will incorporate this circuit.



(c)



(d)

Fig. 3 (c) Sinusoidal wave generators. Four-phase sinusoidal waves $S0$, $S1$, $S2$ and $S3$ with respect to the input voltage are generated. (d) Resistive interpolation circuit and the following comparators.

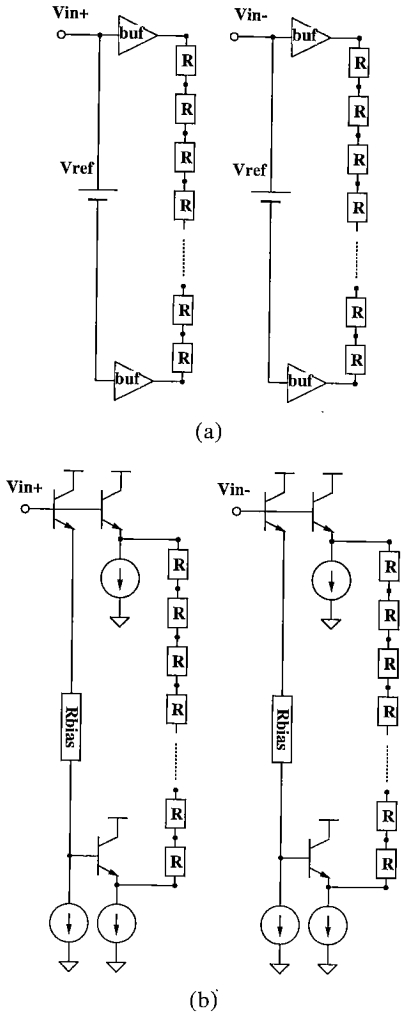


Fig. 4 Proposed high-speed differential resistor string. (a) Equivalent circuit. (b) Actual circuit.

t'_{pd} to reach at the middle of the resistor string (where the signal is most delayed) is given by

$$t'_{pd} \approx K(N/2)^2 RC$$

and we see that

$$t'_{pd} \approx t_{pd}/4.$$

E. Interpolation Circuit Characteristics: We have derived some characteristics of the interpolation circuit. Consider the resistor interpolation ring in Fig. 3 (d) and Fig. 5. Each node of the interpolation resistor ring is connected to the comparator input (usually base of an emitter follower) and then the base current i_b of the emitter follower may degrade the accuracy of the interpolation. However this section shows that the interpolation resistor ring cancels the base current effect thanks to its differential structure. Suppose that

$$S0 = -\overline{S0} := \sin(kV_{in} - (3/4)\pi),$$
$$S1 = -\overline{S1} := \sin(kV_{in} - (1/4)\pi),$$

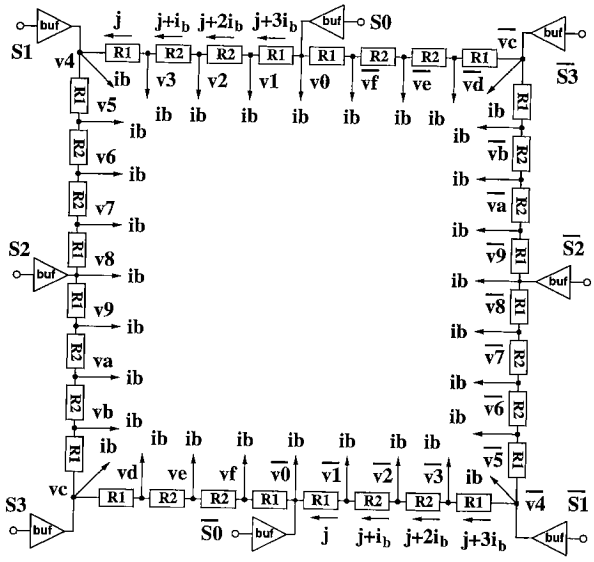


Fig. 5 Resistor interpolation ring with the base current effect.

$$S2 = -\overline{S2} := \sin(kV_{in} + (1/4)\pi),$$
$$S3 = -\overline{S3} := \sin(kV_{in} + (3/4)\pi).$$

Then in Fig. 5

$$\begin{aligned} S0 - S1 &= \overline{S1} - \overline{S0} \\ &= R_1(j + 3i_b) + R_2(j + 2i_b) \\ &\quad + R_2(j + i_b) + R_1 j \\ &= (2j + 3i_b)(R_1 + R_2) \end{aligned}$$

where

$$2j + 3i_b = \frac{S0 - S1}{R_1 + R_2}$$

and hence

$$j = \frac{S0 - S1}{2(R_1 + R_2)} - \frac{3}{2} i_b.$$

Each node voltage of $v_0, \overline{v_0}, v_1, \overline{v_1}, v_2, \overline{v_2}, v_3, \overline{v_3}, v_4$ and $\overline{v_4}$ is given by as follows:

$$v_0 = S0, \quad \overline{v_0} = \overline{S0},$$
$$v_1 = S0 - R_1(j + 3i_b), \quad \overline{v_1} = \overline{S0} + R_1 j,$$
$$v_2 = S0 - R_1(j + 3i_b) - R_2(j + 2i_b),$$
$$\overline{v_2} = \overline{S0} + R_1 j + R_2(j + i_b),$$
$$v_3 = S0 - R_1(j + 3i_b) - R_2(2j + 3i_b),$$
$$\overline{v_3} = \overline{S0} + R_1 j + R_2(2j + 3i_b),$$
$$v_4 = S1, \quad \overline{v_4} = \overline{S1},$$

From the above equations, we obtain the following differential signals:

$$v_0 - \overline{v_0} = 2S0,$$
$$v_1 - \overline{v_1} = \frac{R_1 + 2R_2}{R_1 + R_2} S0 + \frac{R_1}{R_1 + R_2} S1,$$

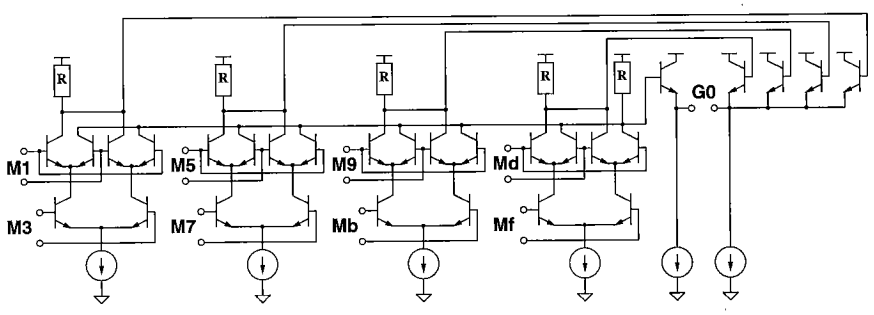


Fig. 6 Digital encoder circuit.

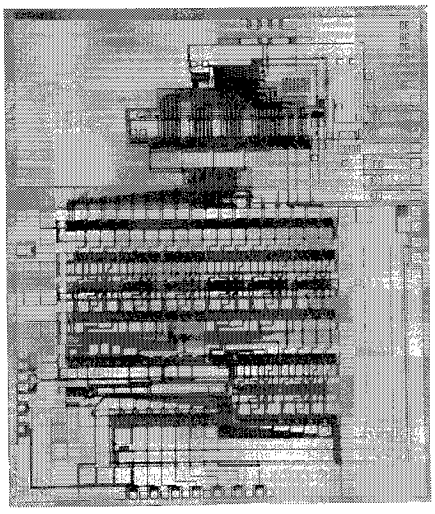


Fig. 7 ADC chip photo.

$$v_2 - \overline{v_2} = S0 + S1,$$
$$v_3 - \overline{v_3} = \frac{R_1}{R_1 + R_2} S0 + \frac{R_1 + 2R_2}{R_1 + R_2} S1,$$
$$v_4 - \overline{v_4} = 2S1.$$

The same approach can be applied for $v_5, \overline{v_5}, \ldots, v_f, \overline{v_f}$. We see that the base current effect is cancelled in the differential signals and the interpolation works correctly.

We also remark that the common-mode mismatch effects among $(S0, \overline{S0})$, $(S1, \overline{S1})$, $(S2, \overline{S2})$ and $(S3, \overline{S3})$ are cancelled in the interpolation resistor ring.

F. Digital Encoder Design: We have developed a simplified encoder circuit equivalent to EXOR-tree circuit utilizing the cyclic nature of interpolation circuit outputs; Fig. 6 shows the digital encoder for G0 and the differential outputs of EXOR circuits are connected to minimum or maximum signal detection circuit, and this circuit converts the inputs of circular code to the outputs of Gray code. This circuit is smaller and faster than the conventional EXOR-tree circuit.

G. ADC Layout Design: Figure 7 shows the ADC chip photo ($4.7 \times 4.0\,\mathrm{mm}^2$), and 1,740 HBT's, 741 resistors and 49 capacitors are integrated. The upper metal is extensively used for interconnection due to its smaller wiring capacitance with respect to the substrate while the lower metal is mainly used for power, ground and bias voltage lines. Also to compensate for the voltage drops of the negative power supply line and the bias voltage line for many current sources and to keep their currents almost the same, the layout topology shown in Fig. 8 is used. Separate power supply lines are used for analog circuit, digital circuit and output buffers.

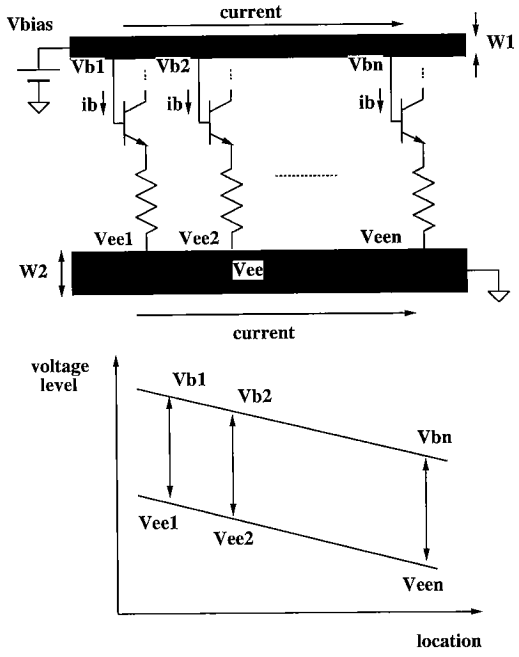


Fig. 8 Layout topology of power supply line and bias line. $W_2/W_1 \approx h_{FE}$ and the voltage drops of power supply and bias lines are almost the same at each location; $V_{b1} - V_{ee1} \approx V_{b2} - V_{ee2} \approx \ldots \approx V_{bn} - V_{een}$ and the currents are almost the same among many current sources.

5. Measured Results

Figure 9 shows the differential and integral nonlinearities and we see that they are within $\pm 1/2LSB$. A sinusoidal input was applied to the ADC and its effective bits were calculated using 2 K-point FFT. Figures 10 (a) and (b) show the effective bits with respect to the input frequency at the sampling rates of 256 MHz and 768 MHz respectively. We see that the effective bits are

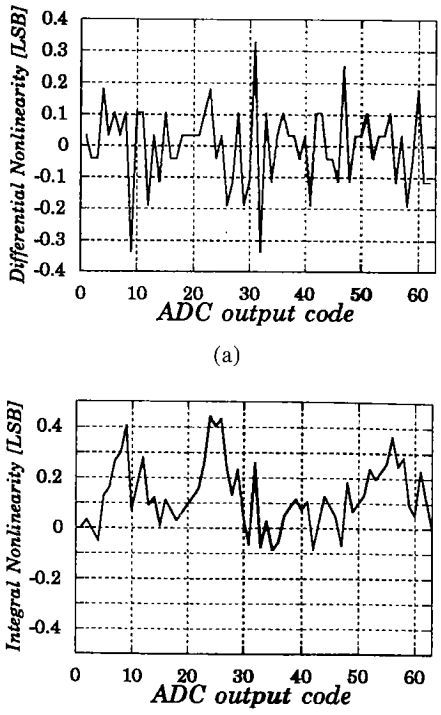


Fig. 9 (a) Differential nonlinearity. (b) Integral nonlinearity.

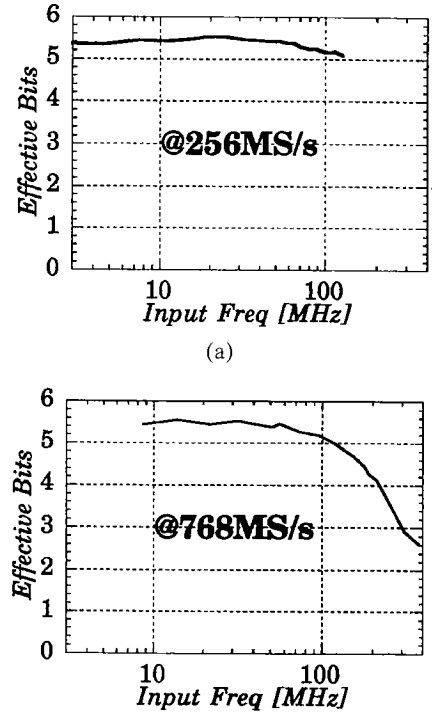


Fig. 10 Measured ADC AC characteristics. (a) Input frequency vs. effective bits @256 MS/s. (b) Input frequency vs. effective bits @768 MS/s.

more than 5 bits upto the input frequency of 128 MHz in both cases. At 896 MS/s the effective bits drop to

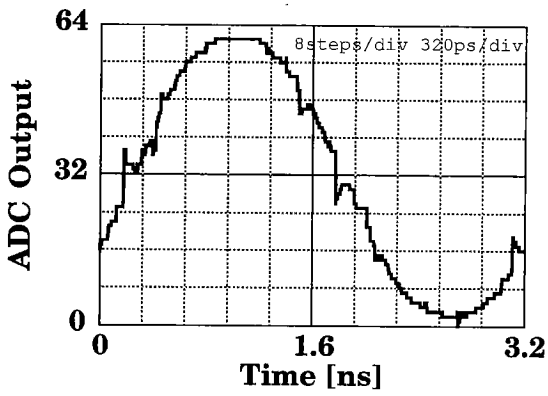


Fig. 11 Measured reconstructed ADC output waveform for a sinusoidal input of 312.4 MHz with 768 MS/s. We recognize some glitches which degrade the effective bits of the ADC at a high-frequency input.

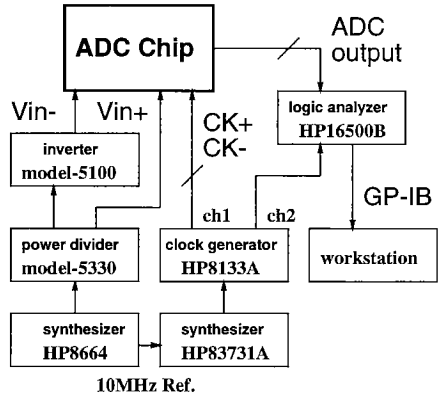


Fig. 12 ADC AC measurement setup.

4.4 bits even at an input frequency of 60 MHz.

The main part to limit the AC performance of the ADC is the analog circuit; Fig. 11 shows the measured reconstructed ADC output for a high frequency sinusoidal input and we recognize some glitches. These are due to the timing skew among folding circuits and sine wave generators. SPICE simulation showed that when a bit synchronizer circuit [13], [15] is incorporated, the timing skew problem is alleviated and the effective bits are more than 5.0 bits upto the input frequency of 500 MHz. We also remark that the folding circuits and sine wave generators produce higher frequency than the input frequency, and to achieve the better AC performance we are considering using a T/H circuit in front of the ADC [14], [17].

All measurements were performed by on-wafer probing and Fig. 12 shows the AC measurement setup. Table 1 summarizes the ADC performance.

6. Conclusions

This paper has described the design and performance of a 6-bit ADC with SiGe HBT. We showed that the Gummel-Poon model suffices for SiGe HBT modeling,

Table 1 ADC performance.

Resolution	6 bits
Sampling frequency	768 MS/s
Effective bits	5.2 bits @100 MHz
Analog input (differential)	1.6 V_{p-p}
Linearity	$\pm 1/2$ LSB
Power (w/o output buffers)	2.8 W
Power supplies	0.5 V, −4.5 V, −5.0 V
HBT count	1,740
Resistor count	731
Capacitor count	49
Chip size	$4.7 \times 4.0\,mm^2$

and using the folding/interpolation architecture as well as simple, differential circuit design developed a functioning ADC chip. We have also discussed some design issues for folding/interpolation ADC. The measured nonlinearity is within $\pm 1/2$ LSB and the effective bits are 5.2 bits at 100 MHz with 768 MS/s. Recently a 4-bit ADC with SiGe HBT was reported in [18], however, to the best of our knowledge, this paper may be the first report of a 6-bit ADC with SiGe HBT.

Acknowledgments

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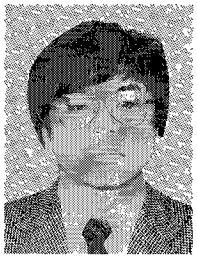
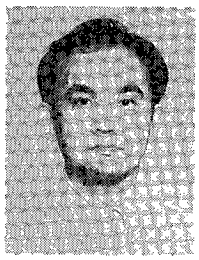
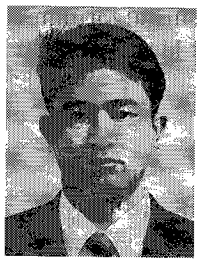


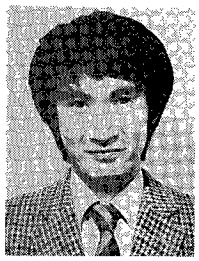
Haruo Kobayashi was born in Utsunomiya, Japan in 1958 and received the B.S. and M.S. degrees in information physics and mathematical engineering from the University of Tokyo in 1980 and 1982 respectively, and the Dr.Eng. degree in electrical engineering from Waseda University in 1995. From 1987 to 1989, he was at UCLA and received the M.S. degree in electrical engineering in 1989. He joined Yokogawa Electric Corp. Tokyo, Japan in 1982, where he was engaged in the research and development related to measuring instruments and a mini-supercomputer. From 1994 to 1997 he was involved in the research and development of ultra-high-speed ADCs and DACs at Teratec Corporation. In 1997 he joined Gunma University and presently is an Associate Professor there. He has been also an adjunct lecturer at Waseda University from 1994. Dr.Kobayashi is a member of the IEEE and the Society of Instrument and Control Engineers of Japan. He is a recipient of the 1994 Best Paper Award from the Japanese Neural Network Society.



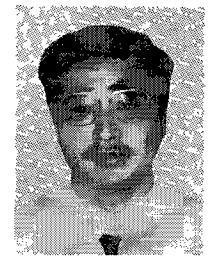
Toshiya Mizuta received the B.S. and M.S. degrees in electronic engineering from Tokyo Institute of Technology, Tokyo, Japan, in 1984 and 1986, respectively. In 1986 he joined Yokogawa Electric Corporation, Tokyo, Japan. From 1992 he has been engaged in the circuits design for high-speed/high-frequency measuring instruments in Teratec Corporation, Tokyo, Japan.



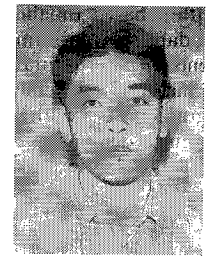
Kenji Uchida received the B.E. and M.E. degrees in electrical engineering from Waseda University in 1990 and 1992 respectively. In 1992, he joined Yokogawa Electric Corporation, Tokyo, Japan. Since 1993, he has been involved in the research and development of wide bandwidth sampling systems in Teratec Corporation, Japan.



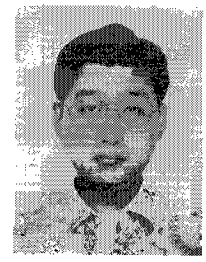
Hiroyuki Matsuura received the B.S. and M.S. degrees in electronic engineering from Tokyo Institute of Technology, Tokyo, Japan, in 1978 and 1980, respectively. In 1980 he joined Yokogawa Electric Corporation, Tokyo, Japan. He was engaged in the research of medical imaging apparatuses and measuring instruments. From 1990 to 1992 he was a visiting scholar of Stanford University, Palo Alto, California. From 1992 he has been engaged in the circuits design for high-speed/high-frequency measuring instruments in Teratec Corporation, Tokyo, Japan. Mr. Matsuura received the Society of Instrument and Control Engineers' Best Paper Award in 1988. He is a member of Society of Instrument and Control Engineers.



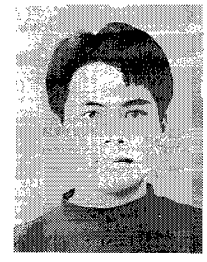
Akira Miura was born in Japan, on November 5, 1955. He received the M.S.E. degree from Waseda University, Tokyo, Japan, in 1980. In 1980 he joined the Yokogawa Electric Corporation, Tokyo, Japan, where he was engaged in the research and development of compound semiconductor devices and circuits. From 1992 he has been engaged in research of III–V HBT's/Si-HBT's devices in Teratec Corporation. His research interests center on the analysis and design of the band engineering for quantum electronics.



Tsuyoshi Yakihara was born in Nagasaki, Japan, on July 25, 1961. He received the B.E. and M.E. degrees from the Nagaoka University of Technology, Niigata, Japan, in 1984 and 1986, respectively. In 1986 he joined the Yokogawa Electric Corporation, Tokyo, Japan. From 1992 he has been engaged in the research and development of III–V compound semiconductor devices in Teratec corporation, Tokyo, Japan. His current research interests are in the development of Si compound semiconductor (SiGe etc.) devices for high-frequency systems.



Sadaharu Oka was born in Tokyo, Japan, in 1963. He received his B.E. and M.E. degrees in instrumentation engineering from Keio University, Yokohama, Japan, in 1986 and 1988, respectively. In 1988 he joined the Yokogawa Electric Corporation, Tokyo, Japan. He was engaged in the research of high-speed compound semiconductor devices. In 1993 he joined Teratec Corporation. His current research interests focus on the development of high-speed Si compound semiconductor devices.



Daisuke Murata was graduated from Sagamidai Technical High School in 1991. He joined Yokogawa Electric Corporation in 1991 and joined Teratec corporation in 1994. He has been engaged in the process engineering.