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Track/Hold Circuit in GaAs HBT Process

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SUMMARY This paper reports on the design and performance of a very fast Track/Hold (T/H) circuit with GaAs Heterojunction Bipolar Transistor (HBT) to precede a 3 GS/s 6 bit ADC. The T/H circuit employs a differential open-loop architecture for high-speed operation, and it consists of diode bridge switches, hold capacitors and output buffers. The differential structure as well as the output buffers suppress droop effects due to the small h_{FE} ($\approx$20) of our HBT. Measured results show that the T/H circuit has better than 6 bit linearity within an input range of 1.0 V_{p-p} with power dissipation of 990 mW, and the bandwidth is 6 GHz in the track mode. The measured droop rate is 2.1 mV/ns, the feedthrough is -46 dB at 500 MHz and the hold pedestal is less than 10 mV. Also a 3 GHz sampling operation of the T/H circuit was measured. The T/H circuit uses 43 HBTs, 24 Schottky barrier diodes and occupies a chip area of 1.4×1.75 mm^2. We also describe the design and performance of a variable gain amplifier with GaAs HBT to precede the T/H circuit as an input buffer and adjust its gain. These results support the possibility of meeting the requirements for a high-speed ADC system.

key words: *track-hold, sample-hold, analog-to-digital converter, HBT, GaAs*

1. Introduction

Electronic devices are continuously getting faster and, accordingly, there is a growing need for instruments to measure their performance. We describe here the design and performance of a very fast Track/Hold (T/H) circuit to precede a 3 GS/s 6 bit ADC [1]–[3] for future measuring instrument applications. A T/H circuit is necessary *in practice* to improve the AC performance of the following ADC even if the ADC employs a flash or folding/interpolation architecture which *in principle* does not require a T/H circuit [4], [5]. T/H circuits are also key components for a time-interleaved ADC system [6].

We chose the GaAs Heterojunction Bipolar Transistor (HBT) to implement the ADC system because of its good device matching, large g_m and high f_T, and now we are trying to integrate T/H and ADC circuits on an AlGaAs/GaAs HBT IC. Recently a couple of institutions have implemented very fast ADCs [7], [8] with this technology, and their figures of the merits compete with Si Bipolar ADCs. The technological potential of GaAs HBT to T/H circuits has been addressed [9]; however, only a limited number of implementations have been reported [7], [8], [10]–[12]. In this paper we investigate the technological potential of GaAs HBT for realizing a very fast T/H circuit, and report on its design and measured performance. We also describe the design and performance of a variable gain amplifier (VGA) with GaAs HBT to precede the T/H circuit and adjust its gain.

GaAs MESFET and Si Bipolar are also technology candidates to realize a high-speed T/H circuit and the T/H circuit design issue comparison among GaAs HBT, GaAs MESFET and Si Bipolar is as follows: since the gate current of GaAs MESFET is negligible, the droop rate of a T/H circuit with GaAs MESFET is very small, which is an advantage of GaAs MESFET. However GaAs MESFET suffers from the trap effects and g_m is smaller compared to GaAs HBT and Si Bipolar, and the challenge in the T/H circuit design with GaAs MESFET is to overcome them [13], [14]. Also since the device matching of GaAs MESFET is poor compared to GaAs HBT and Si Bipolar, monolithic integration of a high accuracy T/H and ADC system will be difficult. The f_T of GaAs HBT is higher than that of Si Bipolar but the device matching of Si Bipolar is better. Then GaAs HBT will be suitable for the very high-speed but relatively lower accuracy T/H and lower resolution ADC system compared to Si Bipolar [15], [16]. Also the thermal conductivity of GaAs substrate is one-third of Si Bipolar and thermal problems should be taken into account more in GaAs HBT circuit design [17].

2. GaAs HBT Process

In our AlGaAs/GaAs HBT process, npn transistors and Schottky barrier diodes (SBDs), thin-film resistors (25 $\Omega/\square$) and metal-insulator-metal capacitors (31 nF/cm^2) are available and a cross section of the devices is shown in Fig. 1. In our HBT, h_{FE} is 20, f_t = 40 GHz and f_{max} = 40 GHz with an emitter current

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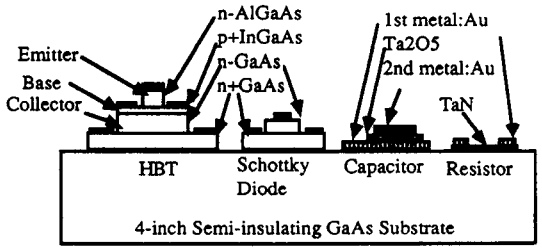


Fig. 1 Cross section of the devices.

Table 1 HBT characteristics (SPICE parameters).

Emitter size	$2\times10\,\mu m^2$	I_{MAX}	10 mA
τ_F	2.12 ps	C_{JC}	60 fF
C_{JE}	83 fF	R_B	68.5 Ω
R_E	9.05 Ω	R_C	20.0 Ω

Table 2 SBD characteristics.

Junction size	$2.1\times20\,\mu m^2$		
Series L	30 pH	Stray C	50 fF
C_{jo}	30 fF	R_s	5.5 Ω
M	0.35	N	1.11

density of 5.0×10^4 A/cm^2, and $BV_{CEO} > 10$ V. Table 1 shows its other characteristics. In our SBD $R_{on} = 4.0\,\Omega$ and $C_{vo} = 30$ fF and Table 2 shows its other characteristics. We consider GaAs HBT to be suitable for realizing a very high-speed T/H circuit because f_T of HBT is high, GaAs substrate is semi-insulating and SBDs can realize very fast diode bridge switches.

3. T/H Circuit

Architecture: The T/H circuit employs a differential open-loop architecture [4], [5] for high-speed operation, and it consists of diode bridge switches, hold capacitors and output buffers (Fig. 2). A VGA circuit described in Sect. 4 precedes the T/H circuit as an input buffer.

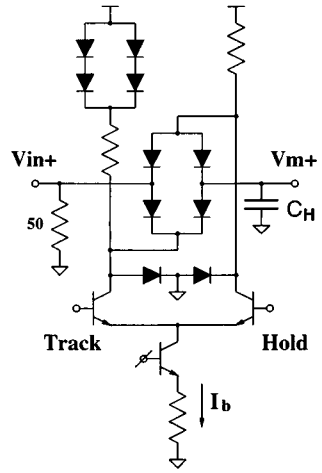
We consider the main challenge in our T/H circuit design to be reducing the droop rate while maintaining high-speed operation because of the small h_{FE} of our HBT, while other nonidealities are relatively insignificant because GaAs substrate is semi-insulating and, thus, the associated parasitic capacitances of active and passive elements are small.

Acquisition Time and Bandwidth: The output $V_{out}(t)$ and input $V_{in}(t)$ of the T/H circuit in the track mode are given by the following relationships provided that it is a first-order system:

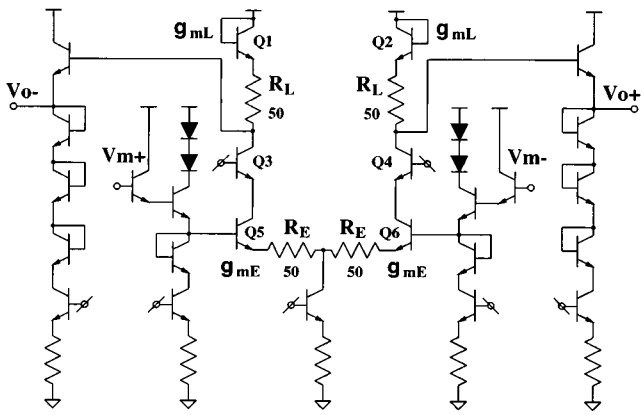
$$V_{out}(t) = V_{in}(t)\exp(-t/\tau)$$

where τ is a time constant. For a 3 GS/s operation, we set the acquisition time to 124 ps and during this time $V_{out}(t)$ should reach $V_{in}(t)$ with better than a 6 bit accuracy (0.78%) which demands

$$\tau \leqq 25.5\,\text{ps}.$$



(a)



(b)

Fig. 2 Track/hold circuit schematics. (a) Core of track/hold circuit. The actual circuit is differential but is shown single-ended for simplicity. (b) Output buffer.

Hence the requirement of the analog bandwidth in the track mode f_{total} is given by

$$f_{total} = \frac{1}{2\pi\tau} \geqq 6\,\text{GHz}.$$

The T/H circuit consists of diode bridge switches and an output buffer and we assign their bandwidth to 10 GHz and 8 GHz as design specifications, respectively, to achieve a total bandwidth of 6 GHz according to the following equation:

$$\frac{1}{6\,\text{GHz}} \approx \sqrt{\frac{1}{(10\,\text{GHz})^2} + \frac{1}{(8\,\text{GHz})^2}}.$$

Diode Bridge Gate Switch: SBDs are used for the diode bridge switches as they have small parasitic capacitances and can provide high-speed switching. As the hold capacitance C_H increases, the effects of droop, feedthrough and hold pedestal are reduced but bandwidth decreases. We chose a hold capacitor C_H of 0.6 pF as a best compromise and set the diode bridge tail

current I_b to 25 mA in Fig. 2 (a) so that the bandwidth f_{bridge} of the diode bridge reaches 10 GHz:

$$f_{bridge} = \frac{1}{2\pi R_s C_H} = 10\,\text{GHz},$$

where

$$R_s = 26.5\,\Omega \text{ at } I_b = 25\,\text{mA}.$$

Also note that the slew rate $V_{out_{max}}$ is given as follows:

$$\frac{dV}{dt} = \frac{I_b}{2C_H} = 2\pi f_{bridge} V_{out_{max}},$$

then

$$V_{out_{max}} = \pm 0.33\,V.$$

Output Buffer: The output buffer in Fig. 2 (b) consists of differential Darlington emitter followers and an open-loop amplifier with a gain of one. The Darlington emitter followers decrease the base currents which flow from the nodes of V_{m+} and V_{m-}, and this reduces the droop effect as described later. We use an open-loop unity gain amplifier because it is faster than a closed-loop one. In our open-loop amplifier (Fig. 2 (b)), Q_1 and Q_2 are added to improve the linearity, and the gain of the open-loop amplifier is given by

$$Gain := \frac{R_L + 1/g_{mL}}{R_E + 1/g_{mE}},$$

where g_{mL} is the transconductance of Q_1, Q_2 and g_{mE} is the transconductance of Q_5, Q_6. Since $R_L = R_E = 50\,\Omega$ and $g_{mL} = g_{mE}$, the gain is set to one. Also the current buffers Q_3, Q_4 enhance the AC performance of the unity gain amplifier. We see that $V_{o+} - V_{o-} = V_{m+} - V_{m-}$ and the common mode voltage between V_{o+} and V_{o-} is constant and level-shifted appropriately regardless of that between V_{m+} and V_{m-}.

Operation: Figure 3 shows measured waveforms of the T/H circuit for a sinusoidal input with f_{in} = 750 MHz and a sampling clock of f_s = 3 GS/s. In the track mode, *Track* signal is high and *Hold* signal is low (Fig. 2 (a)), and the diode bridge switch is ON. Hence the output signal follows the input signal. On the other hand, in the hold mode, *Track* signal is low and *Hold* signal is high, and the diode bridge switch is OFF. The input voltage just before switching from the track to hold modes is stored in the hold capacitor, and thus the output voltage is constant in the hold mode; this helps improve the AC performance of the following ADC. Also the measured error between the input and output just before switching from the track to hold modes is within 1/2 LSB.

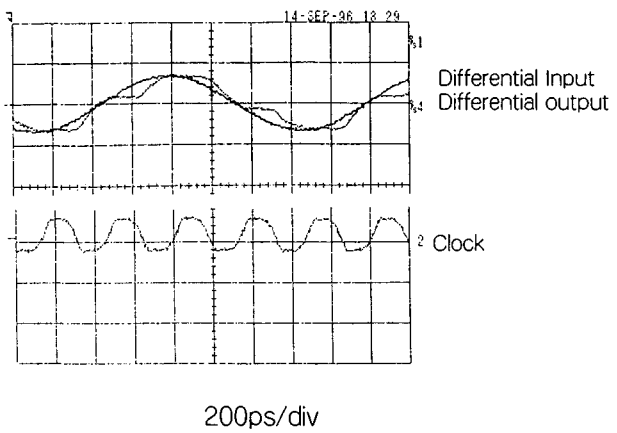


Fig. 3 Measured waveforms for a sinusoidal input with f_{in} = 750 MHz, and a sampling clock of f_s = 3 GS/s. When the clock is high (low), the T/H circuit is in hold (track) mode respectively.

Implementation: The differential core part in Fig. 2 (a) uses 16 HBTs and 20 SBDs dissipating 570 mW, and the output buffer in Fig. 2 (b) uses 27 HBTs and 4 SBDs dissipating 420 mW. The whole T/H circuit occupies a chip area of $1.4 \times 1.75\,\text{mm}^2$ (Fig. 10), and its layout is rather conservative to avoid thermal problems due to the low thermal conductivity of GaAs substrate [17].

Input Range: The measured results show that the T/H circuit has better than 6 bit linearity within the differential input range of $1.0\,V_{p-p}$.

Droop: The input bias current flowing to the output buffer in the hold mode discharges the hold capacitor C_H and the held voltage drops; this is called *droop* [18]. The differential structure, as well as the output buffers, suppress droop effects due to the small h_{FE} ($\approx$20) of our HBT. Suppose that currents I_{b+} and I_{b-} flow from the nodes of V_{m+} and V_{m-} to the output buffer respectively. Then voltage drops ΔV_{m+} and ΔV_{m-} at nodes V_{m+} and V_{m-} during the hold time T_H are given by

$$\Delta V_{m+} = -\frac{I_{b+}}{C_H} T_H, \quad \Delta V_{m-} = -\frac{I_{b-}}{C_H} T_H,$$

respectively. Since the h_{FE} is rather small, I_{b+}, I_{b-} are relatively large and the voltage drops may be considerable. In other words, the single-ended structure suffers from significant droop effects. On the other hand, the differential voltage drop is given by

$$\Delta(V_{m+} - V_{m-}) = -\frac{I_{b+} - I_{b-}}{C_H} T_H.$$

Since the values of I_{b+} and I_{b-} are almost the same and thus $\Delta(V_{m+} - V_{m-})$ is very small compared to ΔV_{m+} and ΔV_{m-}, we see that the differential structure reduces the droop effect significantly. The Darlington emitter followers reduce I_{b+}, I_{b-} and hence also $I_{b+} - I_{b-}$, which further reduces the droop rate. The unity gain open-loop amplifier maintains the common mode voltage between the differential outputs V_{o+} and V_{o-} even if the common mode voltage between V_{m+} and V_{m-} decreases in the hold mode.

The measured results show that the droop rate is less than 2.1 mV/ns (Fig. 4), which is small enough for 3 GS/s 6 bit applications. The main reason for droop

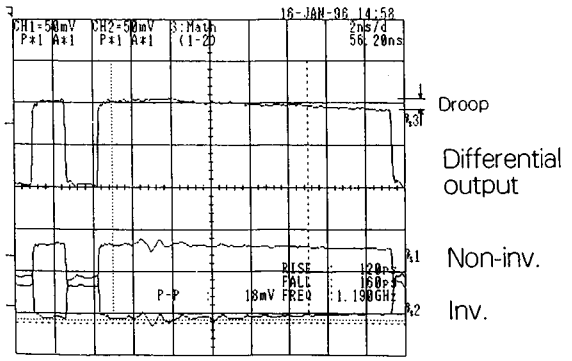


Fig. 4 Droop measurement. A pulse input with $f_{in} = 500\,\text{MHz}$ is applied with a sampling speed of $f_s = 62.5\,\text{MS/s}$.

even in a differential structure is the collector-emitter voltage dependence of base currents in HBTs.

Feedthrough: Ideally no current flows through the diode bridge switch in the hold mode and its impedance is infinite, and thus the hold capacitor is isolated from the input signal. However, in reality because of nonidealities such as junction capacitances in bridge diodes, isolation is not complete. The extent to which an input signal affects the hold output in the hold mode is characterized by *feedthrough* [18].

Since the junction capacitance of SBDs in the diode bridge is small (30 fF), feedthrough is not expected to be a problem: the calculated feedthrough [18] is $-54.5\,\text{dB}$ at 500 MHz while the measured result is $-46.0\,\text{dB}$ at 500 MHz, which is less than 1/2 LSB of 6 bits.

Hold Pedestal: While the bridge diodes are ON in the track mode, they store charge in both their depletion capacitance and their diffusion capacitance. After the bridge switches to the hold mode and all transients settle, the bridge diodes conduct no current. In this state, reduced charge is stored in the depletion capacitance and the diffusion storage is zero. The difference in charge stored during the track mode and the hold mode is from each diode during the turn-off transient. If the charges expelled from the two diodes connected from the hold capacitor are not equal, the net charge injected onto that capacitor imparts an output voltage perturbation called *hold pedestal* [18]. This introduces a distortion in the sampled output if it is nonlinearly dependent on the input signal. In other words, the hold pedestal does not need to be zero if it is proportional to the input signal, and we have to consider its nonlinearity. Thanks to the differential structure, even harmonics are negligible and the third harmonic is dominant. The measured pedestal is 10 mV and its third harmonic distortion is $-53.0\,\text{dB}$ ($< 1/4$ LSB of 6 bits). This result is due to the small junction capacitance of SBDs.

Pulse and Frequency Responses: Figure 5 shows the pulse response of the T/H circuit in the track mode. Its rise time (10%–90%) is 62 ps while the fall time is 72 ps, and we see that there is little overshoot in the pulse response, which means that the output signal can follow the input signal properly in the track mode. Also, Fig. 6 shows the measured frequency response of the T/H circuit; a sinusoidal input was applied and its frequency was swept from 10 MHz to 8 GHz. We see that the bandwidth is 6 GHz.

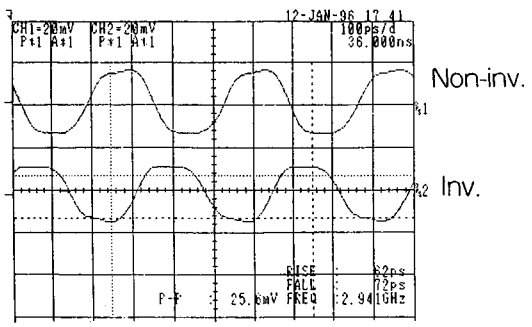


Fig. 5 Pulse response in the track mode. Rise time (10%–90%) is 62 ps while fall time is 72 ps.

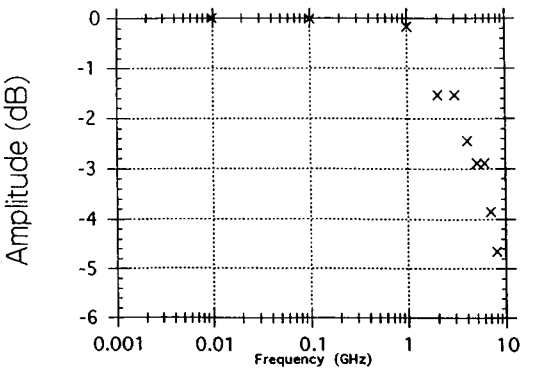


Fig. 6 Frequency response. A sinusoidal input was applied to the T/H circuit and its frequency was swept from 10 MHz to 8 GHz.

3 GHz Sampling: We use the principle of *equivalent time sampling* for a 3 GS/s operation measurement of the T/H circuit [19]. Figure 7 (a) shows its setup where a sampling clock with f_s and a sinusoidal input with f_{in} are synchronized and the output spectrum of the T/H circuit is measured by a spectrum analyzer. The signal frequency f_{out} of the T/H circuit output is given by $f_{out} = f_s - f_{in}$, and it is near the baseband if f_s and f_{in} are close. Figure 7 (b) shows the measured power spectrum of the T/H circuit output with $f_s = 3.000\,\text{GS/s}$ and $f_{in} = 2.997\,\text{GHz}$, and we see that the second harmonic is $-83\,\text{dBm}$ and the third harmonic is $-95\,\text{dBm}$. This measurement was performed for the single-ended output V_{o+} due to the restriction of measurement instruments, but the actual T/H circuit has the differential output V_{o+}, V_{o-}, which is expected to further improve the total harmonic distortion (even harmonics will be cancelled).

All measurements are performed by on-wafer probing, and the summary of the T/H circuit performance is given in Table 3.

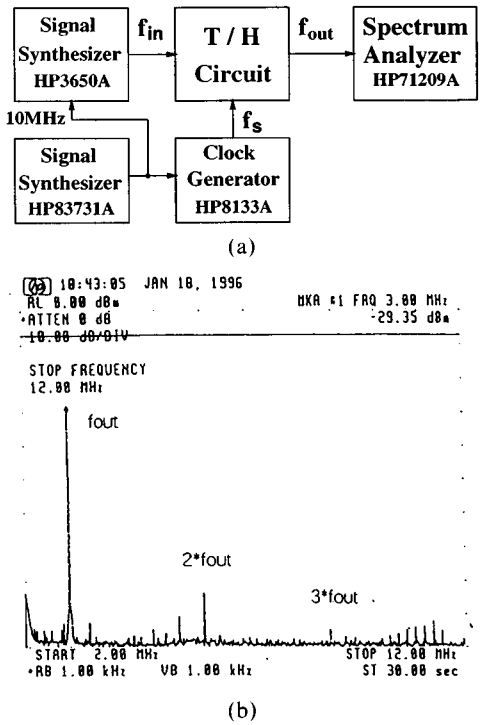


Fig. 7 3 GS/s measurement. (a) Measurement setup where f_{in} and f_s are synchronized. (b) Measured power spectrum of the T/H circuit output.

Table 3 Measured performance of T/H circuit.

Clock frequency	3 GS/s
Analog bandwidth	6 GHz
Analog input	1.0 V_{p-p}
Droop rate	2.1 mV/ns
Feedthrough	−46.0 dB at 500 MHz
Hold pedestal	$< \pm$ 10 mV
Power supplies	3.1 V,−4.5 V
Power consumption	990 mW
HBT count	43
SBD count	24
Chip size	1.4×1.75 mm^2

4. Variable Gain Amplifier

Circuit: A VGA to precede the T/H circuit as an input buffer and adjust the gain of the T/H circuit was also designed and fabricated with GaAs HBT. Figure 8 shows its circuit diagram. If Q_3 and Q_4 are not incorporated and the $1/g_m$'s of Q_1, Q_2, Q_5 and Q_6 are much less than R_E and R_L, then the gain is given by

$$Gain := \frac{V_o}{V_{in}} = \frac{R_L}{R_E}.$$

Q_3 and Q_4 steer the current of I_E from the load resistors R_L and the gain is varied by changing I_E:

$$Gain := \frac{V_o}{V_{in}} = \frac{R_L}{R_E}\left(1 + \frac{I_E}{I_B}\right).$$

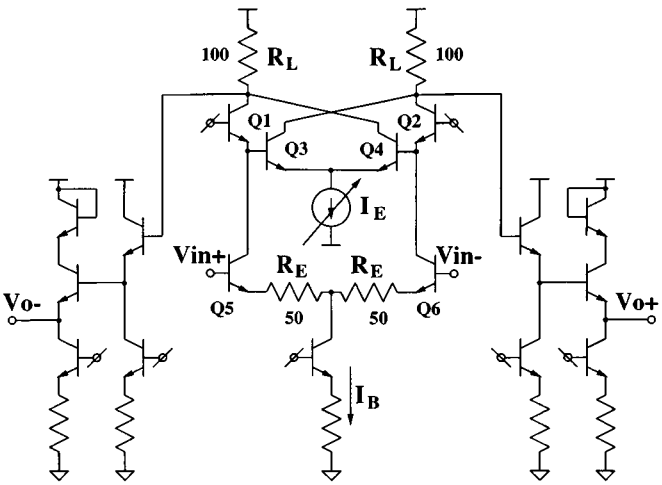


Fig. 8 Variable gain amplifier circuit schematics.

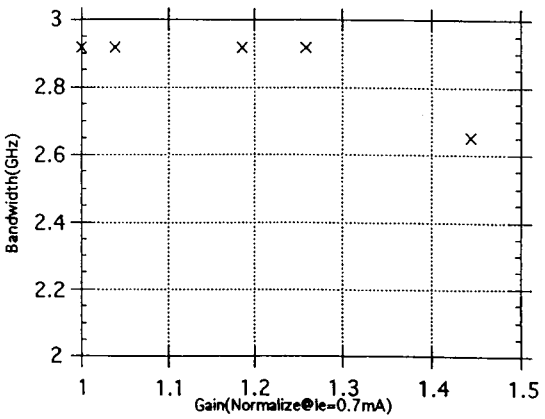


Fig. 9 Measured variable gain amplifier performance. Gain is normalized.

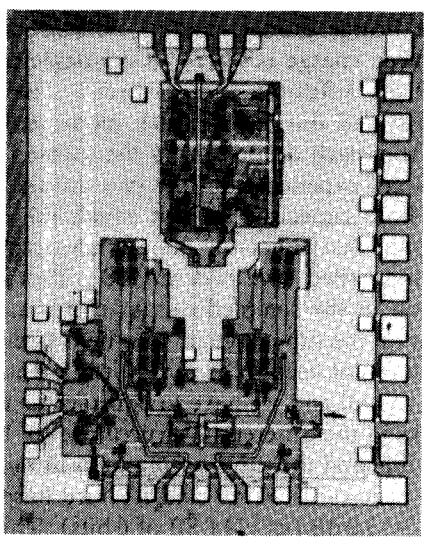


Fig. 10 Track/Hold circuit chip photo.

The differential outputs of the current gain cell are buffered with Darlington emitter followers to minimize

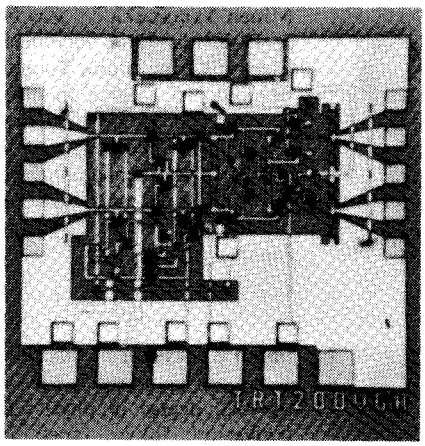


Fig. 11 VGA chip photo.

their base currents.

Since the current buffers Q_1, Q_2 are incorporated, changing the gain does not affect the bandwidth. In many VGA topologies, the gain-bandwidth products are constant, which means that the bandwidth changes according to the gain. However, the bandwidth of VGAs in the front-end of measuring instruments has to be constant regardless of the gain [20], and the circuit in Fig. 8 satisfies this requirement.

Measured Results: The VGA consists of 24 HBTs and 3 SBDs, and it occupies a chip area of $1.0 \times 0.9\,mm^2$ (Fig. 11). The measured results showed that the gain is set to two, and it can be increased by 30% without changing the bandwidth of 2.9 GHz (Fig. 9), and it dissipates power of 155 mW.

5. Conclusion

We have described the design and performance of a very high-speed T/H circuit with GaAs HBT technology and shown that it meets the requirements to precede a 3 GS/s 6 bit ADC. We have also developed a VGA circuit which works as an input buffer of the T/H circuit and adjusts its gain.

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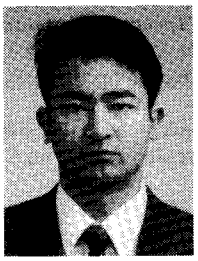

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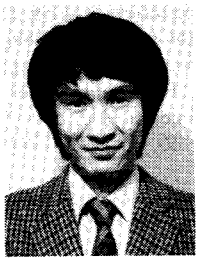

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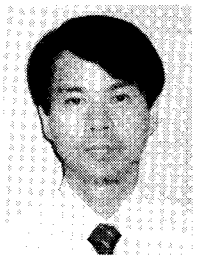

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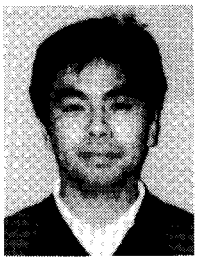

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