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High-speed ADC systems with HBTs for measuring instrument applications

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Abstract

This paper presents very high-speed Analog-to-Digital Converter (ADC) systems for measuring instrument applications, and also related theoretical results. First we describe the design, testing and performance of ≈ 1 GS/s 6-bit and 7-bit ADCs using SiGe heterojunction bipolar transistor (SiGe HBT), and a 3 GS/s 6-bit ADC and Track/Hold (T/H) circuit using GaAs heterojunction bipolar transistor (GaAs HBT). We show that SiGe HBTs and GaAs HBTs have technological potential, and that the folding/interpolation architecture is suitable for high-speed ADC systems. Next, we derive three theoretical results aimed at very high-speed, wideband ADC systems.

- A folding/interpolation architecture is suitable for very high-speed ADCs implemented with HBTs, and digital error correction is required to improve their AC performance. We show an error correction algorithm, as well as its effectiveness and limitation for high-frequency inputs.
- Aperture jitter is crucial in wideband ADC systems, and we have derived very general results about aperture jitter effects of such systems.
- A time-interleave ADC system can realize very high-speed ADC system, but timing skews in the system degrade its overall accuracy. We have derived the error power corresponding to timing skews.

Finally, we discuss several issues relating to standardizing the specifications of very high-speed ADCs targeted at measuring instrument applications.

Keywords: ADC; T/H circuit; Error correction; Jitter; HBT

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1. Introduction

Electronic devices are continuously getting faster, and accordingly there is a growing need for instruments to measure their performance. Digital measuring instruments — which convert analog input signals to be measured to digital signals, and digital signal processors perform some signal processing on them — are becoming popular; hence, ADCs are essential components, and higher performance ones are being demanded. This paper describes high-speed ADC systems implemented with SiGe HBTs and GaAs HBTs for measuring instrument applications, and some theoretical results.

ADCs for measuring instruments are somewhat different from those for consumer electronics, for example. For consumer electronics, low cost and low power consumption design ADCs are very important and monolithic complementary metal-oxide-semiconductor (CMOS) ADC-integrated circuits are mandatory. On the other hand, for measuring instrument applications, high performance (high speed and/or high precision) design is important, and also hybrid implementation with rather special technologies such as GaAs metal-semiconductor field-effect transistor (GaAs MESFET), HBT and Si bipolar junction transistor (Si BJT) is often used to achieve high performance. This is because measuring instruments have to be designed with currently available devices to measure next-generation devices; in other words, the devices to be measured may have higher performance than the devices used in the measuring instrument, and thus the designer has to use rather special approaches — which often sacrifice cost and power consumption — to achieve high performance.

In Section 2, several technologies to implement high-speed ADC systems are compared, and in Section 3, our SiGe HBT and GaAs HBT processes are described. In Sections 4 and 5, high-speed ADCs implemented with SiGe HBTs are presented, while in Section 6, a high-speed ADC with GaAs HBT is described. In Section 7, an error-correction algorithm for ADCs is shown, and in Section 8, roles and implementation of a T/H circuit for ADC systems are described. In Section 9, aperture jitter effects in high-speed ADC system are theoretically derived, and in Section 10 timing skew effects in time-interleaved ADC systems are shown. Based on this, several issues related to standardizing specifications of high-speed ADC for measuring instrumentation applications are discussed in Section 11.

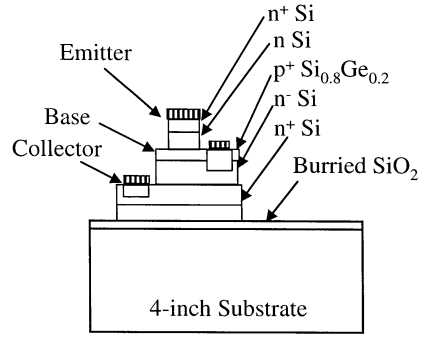


Fig. 1. Cross-section of SiGe HBT.

Table 1
SiGe HBT characteristics

Emitter size	$1.1\times10\ \mu m^2$		
f_T	20 GHz	h_{FE}	20
f_{MAX}	20 GHz	BV_{CEO}	> 8 V

Table 2
GaAs HBT characteristics (SPICE parameters)

Emitter size	$2\times10\ \mu m^2$	I_{MAX}	10 mA
T_F	2.12 ps	C_{JC}	60 fF
C_{JE}	83 fF	R_B	68.5 Ω
R_E	9.05 Ω	R_C	20.0 Ω

2. Technology comparison for high-speed ADC system

There are several technology candidates for implementing very high-speed (> GS/s) ADC systems; CMOS is the most dominant semiconductor technology, but the speed of CMOS ADCs is currently limited to ≈ 500 MS/s even for 6-bit resolution See, e.g., Refs. [32,37]. GaAs MESFET has very high f_T, i.e., high-speed, but the poor device matching and relatively small g_m are disadvantages for our purposes. Si BJT has high f_T, good device matching and large g_m, so are suitable for a high-speed ADC and there are many examples of successful high-speed

Table 3
SBD characteristics in GaAs HBT process

Junction size	$2.1\times20\ \mu m^2$		
Series L	30 pH	Stray C	50 fF
C_{jo}	30 fF	R_S	5.5 Ω
M	0.35	N	1.11

Si BJT ADCs [25,34,36]. However, the speed limit of Si BJT has been addressed and attention is being paid to HBT technology for making even faster devices and circuits [7,8,12]. Recently, very high-speed ADCs with GaAs HBT were introduced [22,24]. Advantages of GaAs HBT are high f_T (higher than Si BJT), large g_m, and good device matching, while disadvantages are low yield, large V_{be} (≈ 1.4 V), thermal problems and high cost. On the other hand, SiGe HBT has potentially higher f_T than Si BJT (but lower than GaAs HBT) and the other characteristics are similar to Si BJT (i.e., relatively easy to use, unlike GaAs HBT) [7,8,31,38].

Based on the above considerations, we have used SiGe HBT and GaAs HBT to investigate their potential for high-speed ADC systems.

3. SiGe HBT and GaAs HBT processes

In our SiGe HBT process, *npn* transistors, thin-film resistors and metal insulator–metal capacitors are available. Our SiGe HBT process uses abrupt-junction-base structure and SIMOX (separation by implanted oxygen) substrate, and f_t of the SiGe HBT is 20 GHZ. Table 1 describes their characteristics and Fig. 1 shows the cross-section of our SiGe HBT.

In our AlGaAs/GaAs HBT process used for the ADC system presented here, *npn* transistors and Schottky barrier diodes (SBDs), thin-film resistors and metal insulator–metal capacitors are available. In our GaAs HBT, h_{FE} is 20, $f_t = 40$ GHz and $f_{max} = 40$ GHz with emitter current density of 5.0×10^4 A/cm^2. In our SBD, $R_{on} = 4.0\ \Omega$ and $C_{vo} = 30$ fF. Tables 2 and 3 describe their characteristics and Fig. 2 shows the cross-section of our GaAs HBT.

4. A 6-bit folding/interpolation ADC with SiGe HBT

This section describes a 768 MS/s 6-bit ADC implemented with SiGe HBT [16,17].

4.1. SiGe HBT modeling

We have used, as our SiGe HBT model, a bipolar transistor with Gummel–Poon model and a diode between its base and collector to represent the breakdown voltage of the HBT. We found that the calculated device parameter values, based on doping concentration and device geometry, and the extracted parameter values matched well, and the circuit simulation and measurement results matched fairly well in all aspects of DC, AC and transient behaviors.

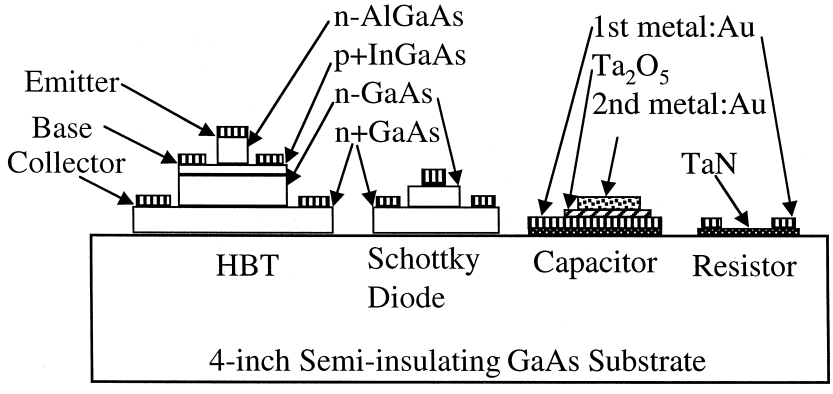
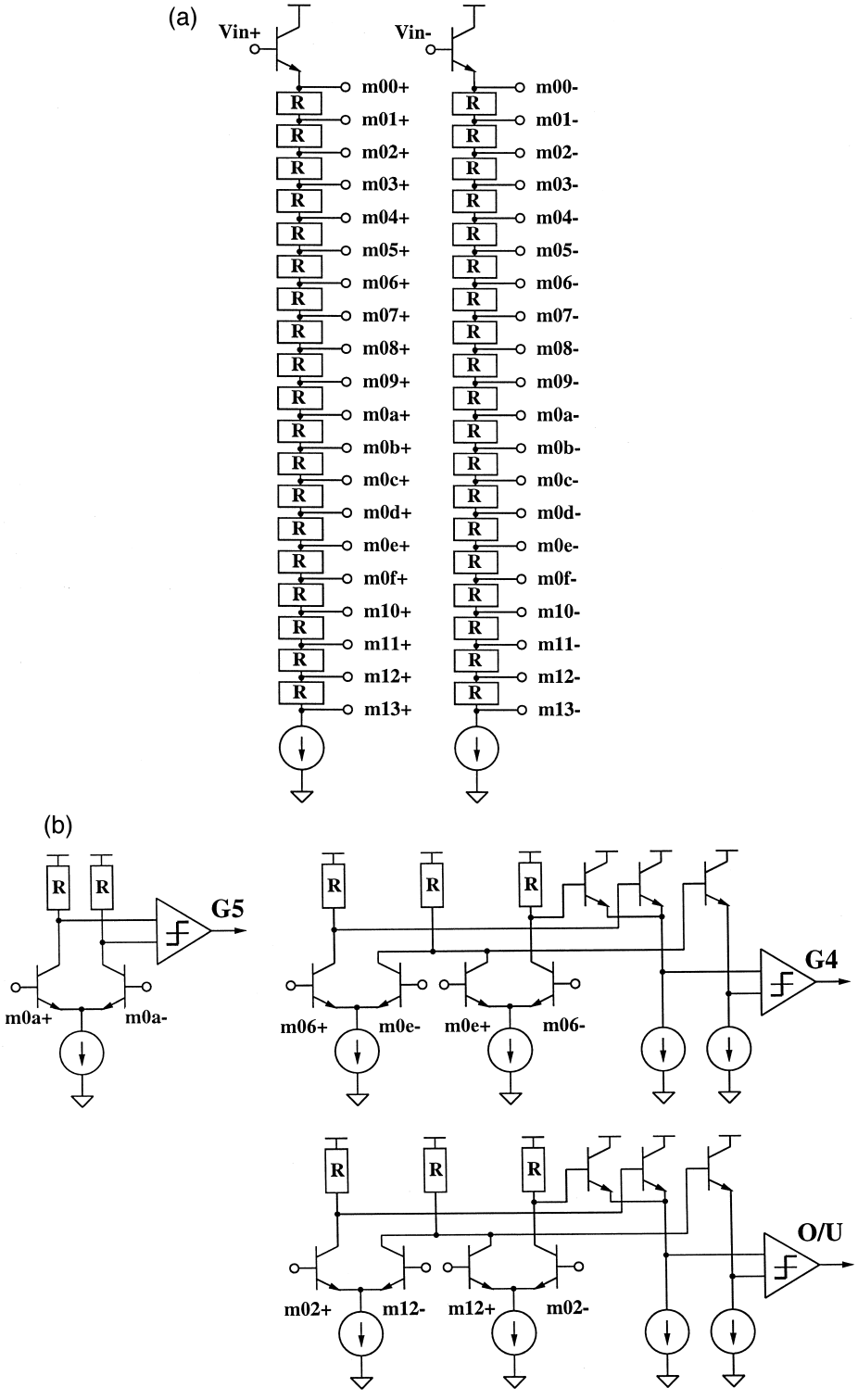


Fig. 2. Cross-section of GaAs HBT.


(a)
Vin+
Vin-
m00+
m01+
m02+
m03+
m04+
m05+
m06+
m07+
m08+
m09+
m0a+
m0b+
m0c+
m0d+
m0e+
m0f+
m10+
m11+
m12+
m13+
m00-
m01-
m02-
m03-
m04-
m05-
m06-
m07-
m08-
m09-
m0a-
m0b-
m0c-
m0d-
m0e-
m0f-
m10-
m11-
m12-
m13-
R
(b)
G5
m0a+
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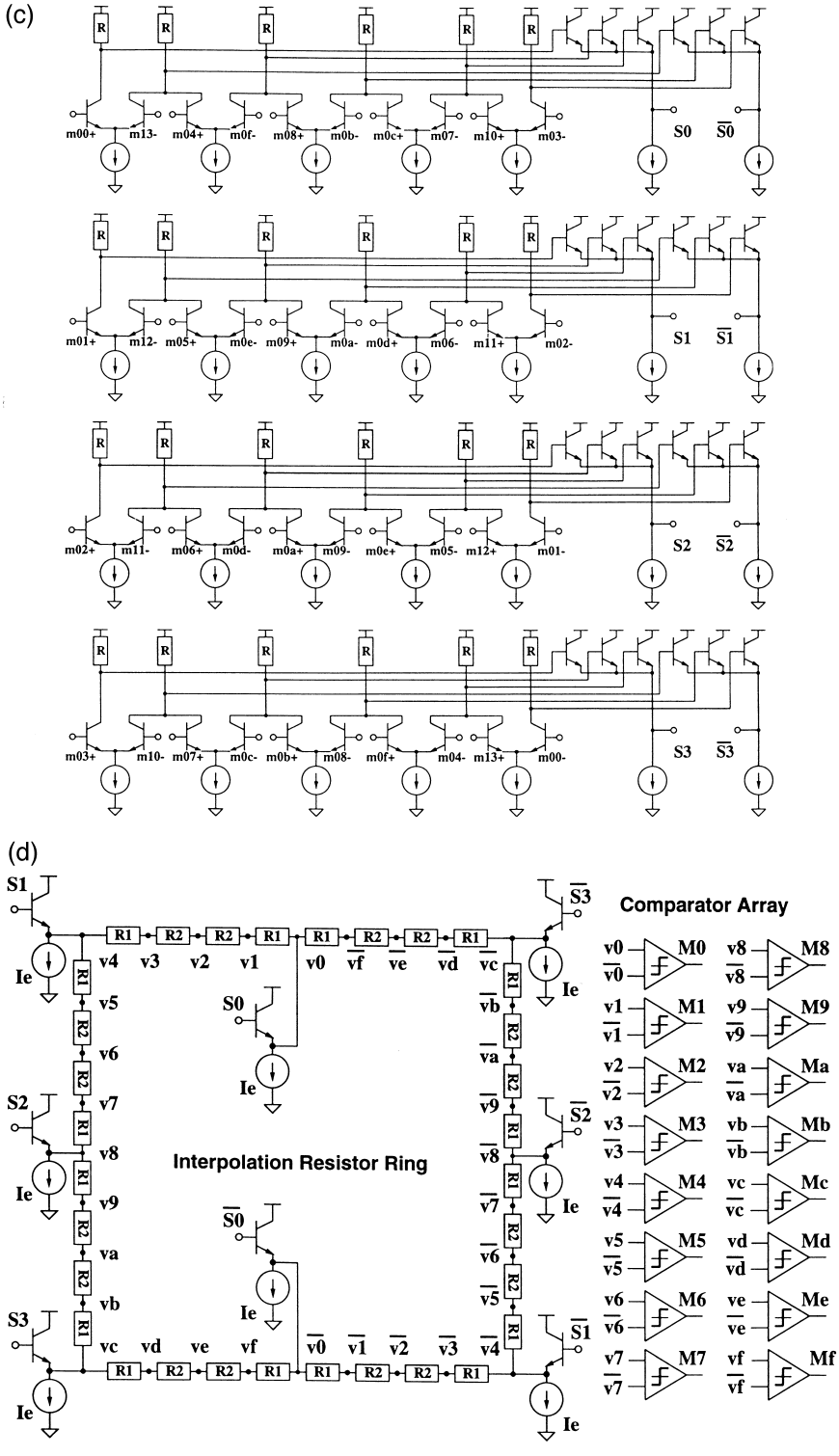
m02+
m12-
m12+
m02-


(c)
R
m00+ m13- m04+ m0f- m08+ m0b- m0c+ m07- m10+ m03-
S0 S̄0
m01+ m12- m05+ m0e- m09+ m0a- m0d+ m06- m11+ m02-
S1 S̄1
m02+ m11- m06+ m0d- m0a+ m09- m0e+ m05- m12+ m01-
S2 S̄2
m03+ m10- m07+ m0c- m0b+ m08- m0f+ m04- m13+ m00-
S3 S̄3
(d)
S1
S̄3
R1 R2 R2 R1 R1 R2 R2 R1
v4 v3 v2 v1 v0 v̄f v̄e v̄d v̄c
Ie
S0
v5 v6 v7 v8 v9 va vb
vc vd ve vf v̄0 v̄1 v̄2 v̄3 v̄4
v̄b v̄a v̄9 v̄8 v̄7 v̄6 v̄5
S2
S̄2
S3
S̄1
Interpolation Resistor Ring
Comparator Array
v0 v̄0 M0
v1 v̄1 M1
v2 v̄2 M2
v3 v̄3 M3
v4 v̄4 M4
v5 v̄5 M5
v6 v̄6 M6
v7 v̄7 M7
v8 v̄8 M8
v9 v̄9 M9
va v̄a Ma
vb v̄b Mb
vc v̄c Mc
vd v̄d Md
ve v̄e Me
vf v̄f Mf

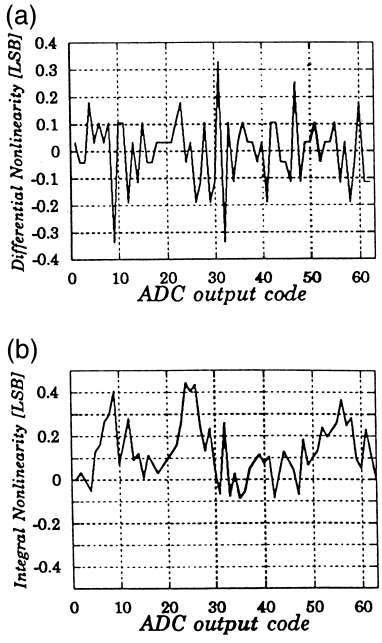


Fig. 4. Measured nonlinearities of the 6-bit ADC with SiGe HBT. (a) Differential nonlinearity. (b) Integral nonlinearity.

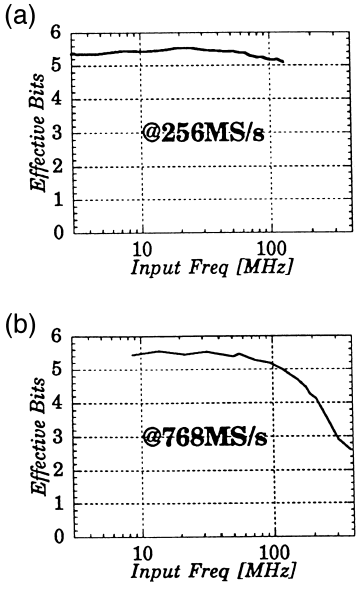


Fig. 5. Measured AC characteristics of the 6-bit ADC with SiGe HBT. (a) Input frequency vs. effective bits at 256 MS/s. (b) Input frequency vs. effective bits at 768 MS/s.

4.2. ADC architecture

The 6-bit ADC implemented with SiGe HBT [16] employs folding/interpolation architecture [23,28,34] to reduce hardware and power (about 1/3 of the flash ADC) while maintaining high-speed operation. A differential resistor string is used in the ADC input stage (Fig. 3a) to cancel the reference DC bowing effects [4,28]. The folding circuits (a cycle pointer) perform analog encoding and generate G5 (MSB) and G4 of Gray code and O/U (overflow/underflow) bit (Fig. 4b) [15]. Four sinusoidal wave generators (Fig. 3c) and a resistor interpolation circuit (Fig. 3d) produce 16 sinusoidal waves with different phases with respect to the input voltage. Following the interpolation circuit, XOR-tree type digital encoder circuits generate the lower 4 bits (G3, G2, G1, G0 (LSB)) of Gray code from $M_0, \ldots M_f$ in Fig. 3d. In other words, two higher bits are generated by analog encoding while the remaining four lower bits are generated by digital encoding.

All of the internal signals are differential, and all of the internal analog and digital circuits are basically composed of differential pairs and emitter followers, while the digital outputs are single-ended (open-collector).

4.3. Measured results

Fig. 4 shows the differential and integral nonlinearities measured for DC inputs with $1.6V_{pp}$ produced by programmable voltage generators and we see that they are within $\pm 1/2$ LSB. A sinusoidal input was applied to the ADC, and its number of

Fig. 3. 6-bit ADC circuits with SiGe HBTs. (a) Differential resistor string. (b) Folding circuits which generates $G5$, $G4$ and O/U. (c) Sinusoidal wave generators. Four-phase sinusoidal waves $S0$, $S1$, $S2$ and $S3$ with respect to the input voltage are generated. (d) Resistive interpolation circuit and the following comparators.

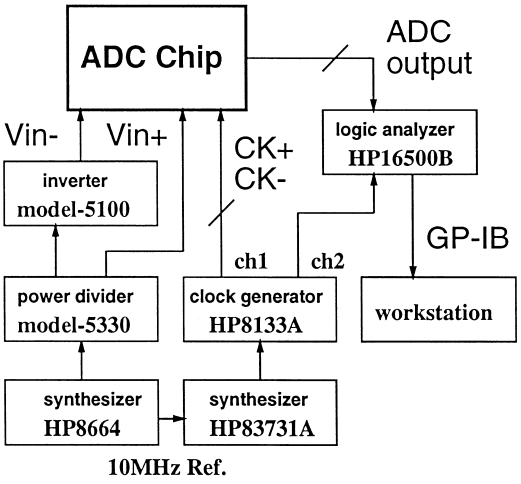


Fig. 6. AC measurement setup for the 6-bit ADC with SiGe HBT.

effective bits was calculated using 2 K-point FFT. Fig. 5a and b show the number of effective bits with respect to the input frequency at the sampling rates of 256 and 768 MHz, respectively. We see that the number of effective bits is more than 5.0 bits upto the input frequency of 128 MHz in both cases. At 896 MS/s, the number of effective bits drops to 4.4 bits even at an input frequency of 60 MHz. All measurements were performed by on-wafer probing, and Fig. 6 shows the AC measurement setup. Table 4 summarizes the ADC performance, and Fig. 7 shows the ADC chip photo (4.7×4.0 mm^2).

The main part limiting the AC performance of the ADC is the analog circuit; Fig. 8 shows the measured reconstructed ADC output for a high frequency sinusoidal input, and we notice some glitches. These are due to timing skew among folding circuits and sine wave generators. SPICE simulation showed that when digital error correction [15,18,23] is incorporated, the timing skew problem is alleviated (this will be described later) and the number of effective bits is

Table 4
Measured performance of the 6-bit ADC with SiGe HBT

Resolution	6 bits
Sampling frequency	768 MS/s
Effective bits	5.2 bits at 100 MHz
Analog input (differential)	1.6 $V_{p\text{-}p}$
Linearity	$< \pm 1/2$ LSB
Power (with output buffers)	3.5 W
Power supplies	0.5, −4.5, −5.0 V
HBT count	1740
Resistor count	731
Capacitor count	49
Chip size	4.7×4.0 mm^2

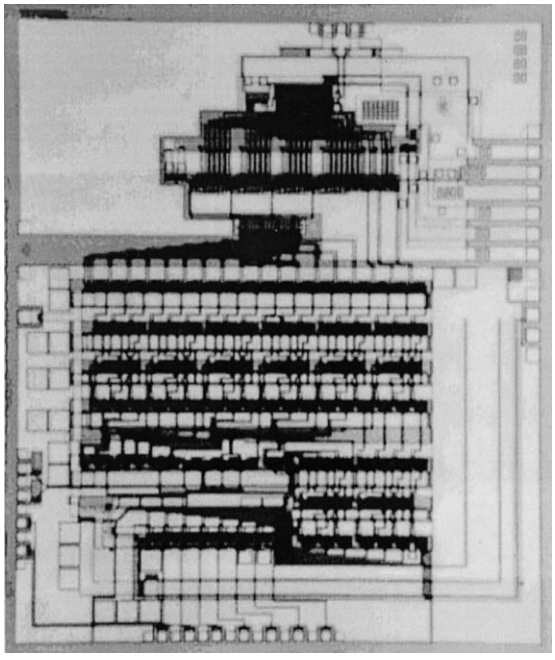


Fig. 7. Chip photo of the 6-bit ADC with SiGe HBT.

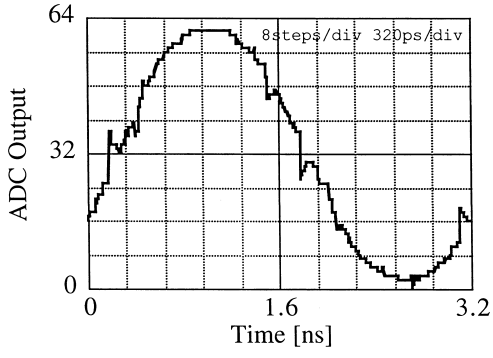


Fig. 8. Measured reconstructed ADC output waveform for a sinusoidal input of 312.4 MHz with 768 MS/s. We notice some glitches, which degrade the effective bits of the ADC at a high-frequency input.

more than 5.0 bits upto the input frequency of 400 MHz.

5. A 7-bit folding/interpolation ADC with SiGe HBT

Recently, folding/interpolation ADCs with cascaded analog encoding circuits [3,4,9,35] have been proposed/implemented for higher bit resolution. Based on this idea, we have designed a 7-bit folding/interpolation ADC with SiGe HBT; to obtain an extra 1-bit with minimum hardware, analog encoding circuits (Gilbert cells or analog multipliers, Fig. 9) are added after the resistive interpolation circuit [4]. We have fabricated this ADC with our SiGe HBT process, and Fig. 10 shows the ADC chip photo. Its chip area is 4.9×4.0 mm^2, which is just a little bit larger than that of the 6-bit ADC.

Our SPICE simulation showed that its number of effective bits is more than 6.5 bits upto 100 MHz input signal at 1 GS/s, however the measured results were 6.1 bits at 512 MS/s and 5.8 bits at 1 GS/s even for low frequency sinusoidal inputs (Table 5, Fig. 11). We have found that this is due to the large offset voltage ($\sigma = 6.5$ mV) of the input differential pairs; since our SiGe HBT process was not mature, its V_{be} variation was relatively large. It is expected that device mismatches will become smaller when the SiGe HBT process becomes more stable; this problem can be alleviated by circuit design approaches such as using an averaging resistor network among the input differential pairs [3,14]. We have also found by SPICE simulation that the distributed resistances and capacitances on the interconnection lines have to be taken care of, to improve the AC performance.

We are convinced through fabrication and testing of these designs that a 1 GS/s 7-bit ADC is feasible using our SiGe HBT process with reasonable chip area, though this has not been proven by an actual chip yet.

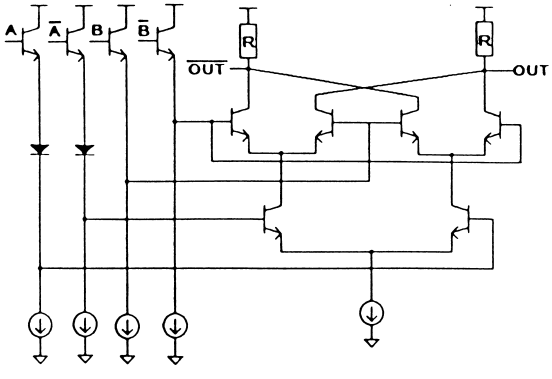


Fig. 9. Gilbert cell added after the resistive interpolation (Fig. 3d) to obtain an extra bit.

6. A 6-bit folding/interpolation ADC with GaAs HBT

This section describes a 6-bit 3 GS/s ADC implemented with GaAs HBTs [19].

6.1. Design philosophy

GaAs HBT can be considered as *a power-limited device*; its f_T increases monotonically within a reasonable range of I_c and thus its bias current is set as large as possible to obtain high performance. However, GaAs substrate thermal conductivity is one-third that of Si, and GaAs HBT electrical characteristics change with temperature, which limit the maximum reasonable power dissipation of a GaAs HBT chip. Also currently the large-scale integration of GaAs HBTs is difficult and monolithic integration of a 6-bit flash ADC is impractical. Hence, the reduction of power and circuit maintaining high-speed is a key point of the ADC architecture and circuit design.

6.2. ADC architecture

The 6-bit ADC with GaAs HBTs employs folding/interpolation architecture and MSB, MSB-1 and MSB-2 are generated by analog encoding while the other lower 3 bits are generated by digital encoding; this ADC uses more analog encoding than the 6-bit ADC with SiGe HBT described above. We use this configuration considering the balance between GaAs HBT yield problem and its higher speed (than SiGe HBT); qualitatively speaking, as the number of bits by analog encoding increases, the hardware and power of the ADC decrease while the analog encod-

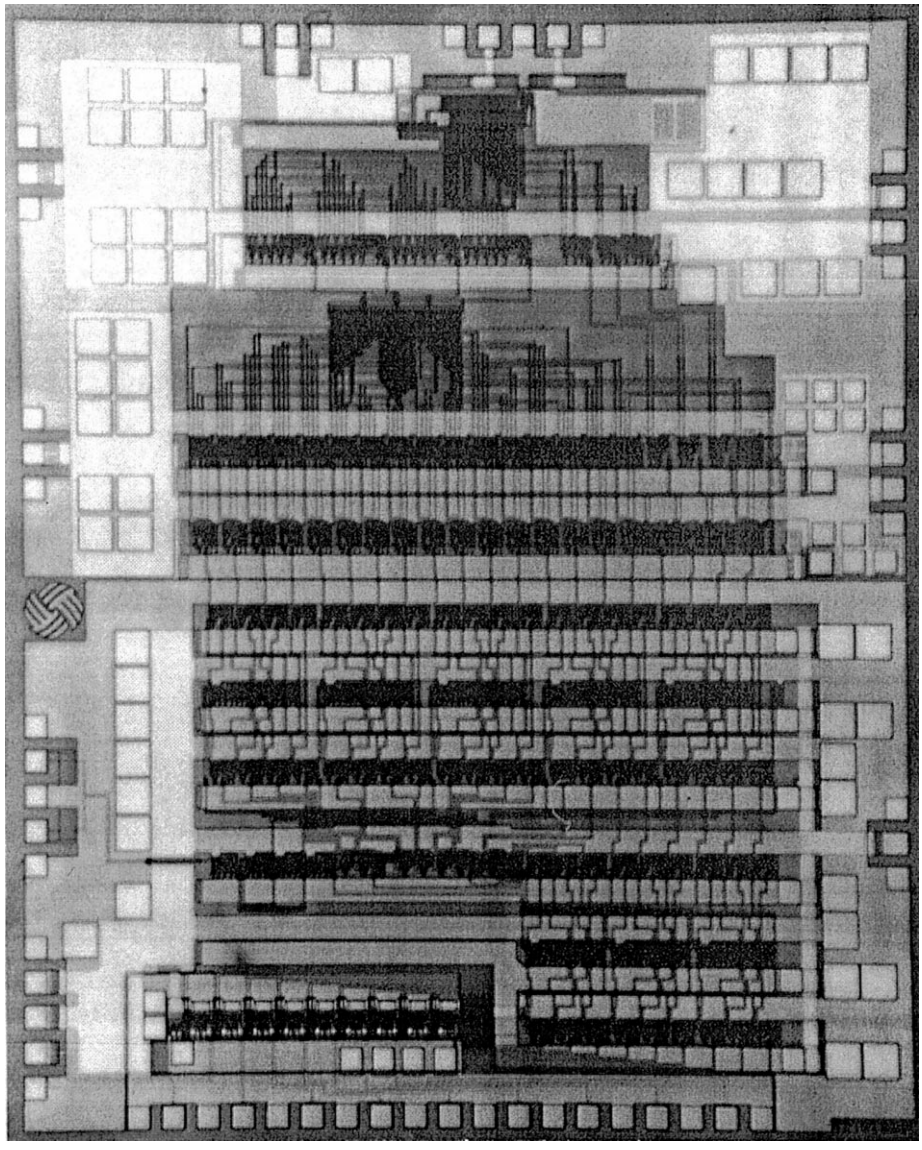


Fig. 10. Chip photo of the 7-bit ADC with SiGe HBT.

ing circuit generates higher frequency signals, which may degrade the AC performance of the folding ADC [23]. Fig. 12 shows the chip photo and Table 6 summarizes the ADC characteristics.

We remark that since our process technology is not mature, it is difficult to deduce the reasons for the performance difference among the three ADCs presented here; the performance difference is not be only due to architecture and circuit design but also due to process technology.

7. Digital error correction algorithm for folding / interpolation ADC

This section describes an error correction algorithm for the folding/interpolation ADC, and this

Table 5
Measured performance of the 7-bit ADC with SiGe HBT

Resolution	7 bits
Sampling frequency	1.0 GS/s
Effective bits	5.8 bits at 10 MHz, 1 GS/s
	6.1 bit at 4 MHz, 512 MS/s
Analog input (differential)	1.7 $V_{p\text{-}p}$
DNL	<1.2 LSB
INL	$<1.0\%$ of FSC
Power (with output buffers)	5.0 W
Power supplies	0.5, -3.6, -5.0 V
Input Capacitance	<3 pF
HBT count	2653
Resistor count	938
Capacitor count	90
Chip size	4.9×4.0 mm^2

algorithm is useful to improve the AC performance of the ADC especially when the ADC is not preceded by a T/H circuit [15,18,23].

7.1. Principle

Let us assume, without loss of generality, that in an 8-bit folding/interpolation ADC with Gray code output the higher 3 bits ($G7$, $G6$, $G5$) are generated by folding circuits (a cycle pointer), and the other lower 5 bits ($G4$, $G3$, $G2$, $G1$, $G0$) and a redundant bit $B4$ are generated by interpolation circuits. Their chart with respect to the input V_{in} is shown in Fig. 13. The error correction algorithm described here correct the values of the higher 3 bits ($G7$, $G6$, $G5$) according to the values of $G4$ and $B4$. In an ideal case (no timing skew or device mismatch), the transition points of $B4$ from 1 to 0 or from 0 to 1 can be equal to those of $G7$, $G6$ and $G5$ with respect to V_{in}. Also, assume that there are no analog skews among ($G7$, $G6$, $G5$) nor those among ($G4, \ldots, G0$, $B4$) while there is analog timing skew t between ($G7$, $G6$, $G5$) and ($G4, \ldots, G0$, $B4$). In the critical region X, $Y0$, $Y1$, $Z0$, $Z1$, $Z2$ and $Z3$ in Fig. 13, due to the skew δt, the cycle pointer samples $V_{in}(t)$ while the interpolation circuit samples $V_{in}(t+\delta t)$, and $V_{in}(t)$ and $V_{in}(t+\delta t)$ are in the different cycles; e.g., in Fig. 13, the cycle pointer samples A while the interpolation circuit samples B and then the total ADC output virtually samples C, which causes a large error. The digital error correction works as follows: when V_{in} is in the critical regions, digital error correction [15,18] corrects the values of $G7$, $G6$ and $G5$ to $G7'$, $G6'$ and $G5'$ based on $G7$, $G6$, $G5$, $G4$ and a redundant bit $B4$. Noting that critical regions of X, $Y0$, $Y1$, $Z0$, $Z1$, $Z2$ and $Z3$ can be

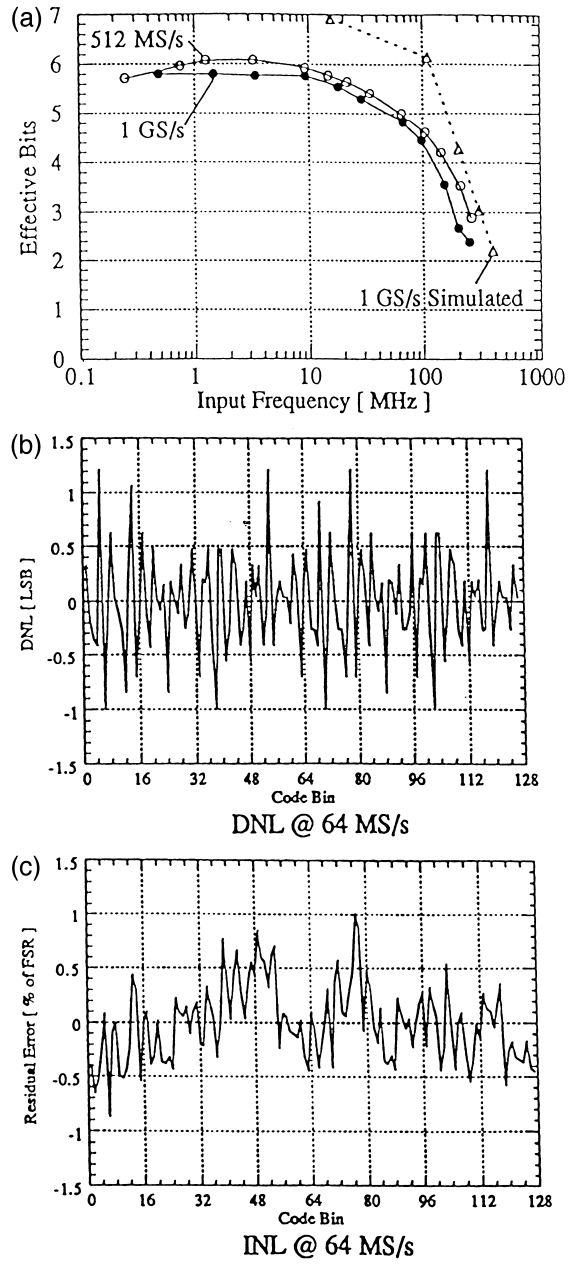


Fig. 11. Measured performance of the 7-bit ADC with SiGe HBT. (a) Input frequency vs. effective number of bits. (b) Differential nonlinearity for DC input with 1.7 $V_{p\text{-}p}$. (c) Integral nonlinearity for DC input with 1.7 $V_{p\text{-}p}$.

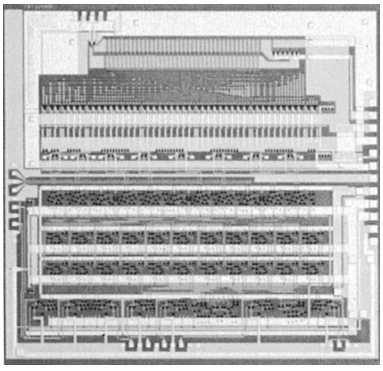


Fig. 12. Chip photo of the 6-bit ADC with GaAs HBT.

recognized correctly by the codes of $G7$, $G6$, $G5$, $G4$ and $B4$ according to Fig. 13 and Table 7, we obtain the following digital error correction algorithm:

$$G7' = \begin{cases} \overline{B4} & (\text{in case } V_{\text{in}} \text{ is in region } X) \\ G7 & (\text{otherwise}) \end{cases}$$

$$G6' = \begin{cases} \overline{B4} & (\text{in case } V_{\text{in}} \text{ is in region } Y0) \\ B4 & (\text{in case } V_{\text{in}} \text{ is in region } Y1) \\ G6 & (\text{otherwise}) \end{cases}$$

$$G5' = \begin{cases} \overline{B4} & (\text{in case } V_{\text{in}} \text{ is in region } Z0 \text{ or } Z2) \\ B4 & (\text{in case } V_{\text{in}} \text{ is in region } Z1 \text{ or } Z3) \\ G5 & (\text{otherwise}). \end{cases}$$

Then we obtain the following:

$$G7' = G6 \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{B4} + (\overline{G6} + G5 + G4) \cdot G7$$

$$G6' = (\overline{G7 \oplus B4}) \cdot G5 \cdot \overline{G4} + (\overline{G5} + G4) \cdot G6$$

$$G5' = (G7 \oplus G6 \oplus B4) \cdot G4 + \overline{G4} \cdot G5.$$

Note that the error-corrected ADC outputs are $G7'$, $G6'$, $G5'$, $G4$, $G3$, $G2$, $G1$ and $G0$.

Table 6
Measured performance of the 6-bit ADC with GaAs HBT

Resolution	6 bits
Sampling frequency	3.0 GS/s
Analog bandwidth	300 MHz
Analog input (differential)	1.5 $V_{\text{p-p}}$
Power (with output buffers)	4.0 W
Power supplies	0.5, −7.0 V
HBT count	845
SBD count	19
Resistor count	487
Capacitor count	20
Chip size	4.4×4.0 mm^2

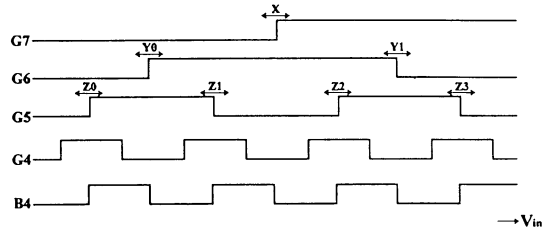


Fig. 13. The chart of $G7$, $G6$, $G5$ and $B4$ with respect to V_{in} and the critical regions of X, $Y0$, $Y1$, $Z0$, $Z1$, $Z2$ and $Z3$.

7.2. Simulation

Fig. 14 shows the SPICE simulation results of the 6-bit folding/interpolation ADC with SiGe HBT described above; a solid-line shows the effective bits vs. the input frequency *without* error correction and a dashed-line shows that *with* error correction. We see that with the error correction the effective bits are more than 5.0 bits upto the input frequency of 500 MHz. The fabricated ADC does not incorporate error correction and its measured results match fairly well with Fig. 5. Hence, it is expected that the actual chip would achieve comparable performance if it incorporates the error correction.

7.3. Limitation of digital error correction

We have shown [15,18] that the above-mentioned error correction works properly if and only if:

$$\frac{1}{2^n \pi} > \delta t \cdot f_{\text{in}}, \tag{1}$$

where n: the number of higher order bits generated by the cycle pointer (in the above example, $n = 4$),

Table 7
Critical regions and their corresponding higher bits
x: does not care.

Region	$G7$	$G6$	$G5$	$G4$
X	x	1	0	0
$Y0$	0	x	1	0
$Y1$	1	x	1	0
$Z0$	0	0	x	1
$Z1$	0	1	x	1
$Z2$	1	1	x	1
$Z3$	1	0	x	1

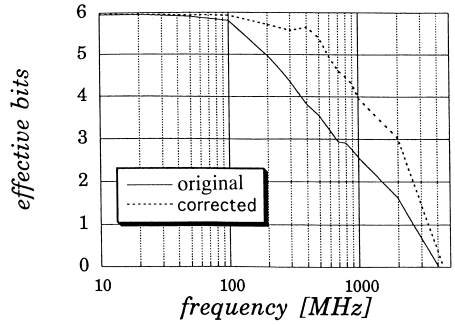


Fig. 14. SPICE simulation results of the 6-bit folding/interpolation ADC with SiGe HBT. The solid-line shows the number of effective bits vs. the input frequency *without* error correction, while the dashed-line shows the results *with* error correction.

δt: the analog timing skew between higher and lower order bits, f_{in}: the input signal frequency. The intuitive interpretation is as follows (Fig. 15): the error correction works properly if the difference, due to timing skew δt, between the cycle numbers, which the cycle pointer and the interpolation circuit indicate is within ± 1. On the other hand, when the difference is ≥ 2 or ≤ -2, the error correction does not work properly. According to Eq. (1), the timing skew δt needs to be minimized to improve the AC performance of the ADC even if error correction is employed, and this is also confirmed by SPICE simulation of the ADC at transistor level.

Remark that if device mismatches (e.g., DC offsets of analog encoding circuits) are sufficiently large, this may cause synchronization problems between folding circuits and interpolation circuits, but the above-mentioned error correction algorithm works also in this case as well as in the timing skew case. We note that the error correction algorithm can easily be extended to other configurations of folding/interpolation ADCs.

8. Track/hold circuit in high-speed ADC system

8.1. Role of track/hold circuit in high-speed ADC system

A T/H circuit is necessary *in practice* to improve the AC performance of the following ADC even if the ADC employs the folding/interpolation architecture, which *in principle* does not require a T/H circuit. When a T/H circuit precedes an ADC, the ADC input (i.e., the T/H output) is almost constant and the ADC performs the sampling operation in hold mode. Hence, during the hold mode, $V_{in}(t) \approx V_{in}(t + \delta t)$ if δt is sufficiently small compared to the hold duration so that the analog timing skew δt does not cause synchronization problems between folding circuits and interpolation circuits.

Three timing issues should be considered for the T/H circuit [18]:

1. Minimizing analog timing skew between folding circuit and interpolation circuit.
2. Optimum delay adjustment between T/H circuit clock and ADC sampling clock.
3. Duty cycle between track mode and hold mode duration.

Analog timing skew δt should be minimized for higher sampling rate; in our ADC [16], folding circuits are faster than sine generators and hence some circuitry, e.g., differential buffer amplifiers, should be inserted in folding circuits for extra delay. Since there is some delay in a T/H amplifier, the delay between T/H circuit clock and ADC sampling clock should be adjusted [25]. Also the duty cycle between track mode and hold mode duration should be considered; usually the duty cycle is 50% for a T/H circuit, however if the two T/H circuits are cascaded as a master–slave configuration [24], hold duration becomes longer, which will further improve the AC performance of the ADC.

We also remark that the folding circuits and sine wave generators produce higher frequency signals than the input frequency, which may degrade the AC performance of the ADC, and the T/H circuit in front of the ADC may alleviate this problem; the higher frequency signal generation does not matter if the T/H is incorporated and the output signals of the analog encoding circuits settle within the sampling period [4,24]. Also note that T/H circuits are also key components for a time-interleaved ADC system.

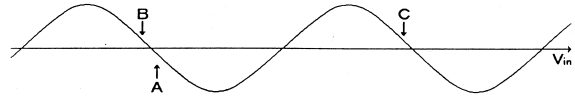


Fig. 15. The cycle pointer samples $V_{in}(t)$ $(= A)$ while the interpolation circuit samples $V_{in}(t + \delta t)$ $(= B)$, and $V_{in}(t)$ and $V_{in}(t + \delta t)$ can be in different cycles due to skew δt; the total ADC output virtually samples C, which causes a large error.

8.2. Track / hold circuit with GaAs HBT

Next, we will describe a 3GS/s 6-bit T/H circuit [19,33] implemented with GaAs HBT to improve the AC performance of the 3GS/s 6-bit ADC with GaAs HBT.

8.2.1. Architecture

The T/H circuit employs a differential open-loop architecture for high-speed operation, and its consists of diode bridge switches, hold capacitors (0.6 pF) and output buffers (Fig. 16). SBDs are used for the diode bridge switches as they can provide high-speed switching. The output buffer in Fig. 16b consists of differential Darlington emitter followers and an open-loop amplifier with gain of one. $Q1$ and $Q2$ are added to improve the linearity, and the current buffers $Q3$, $Q4$ enhance the AC performance.

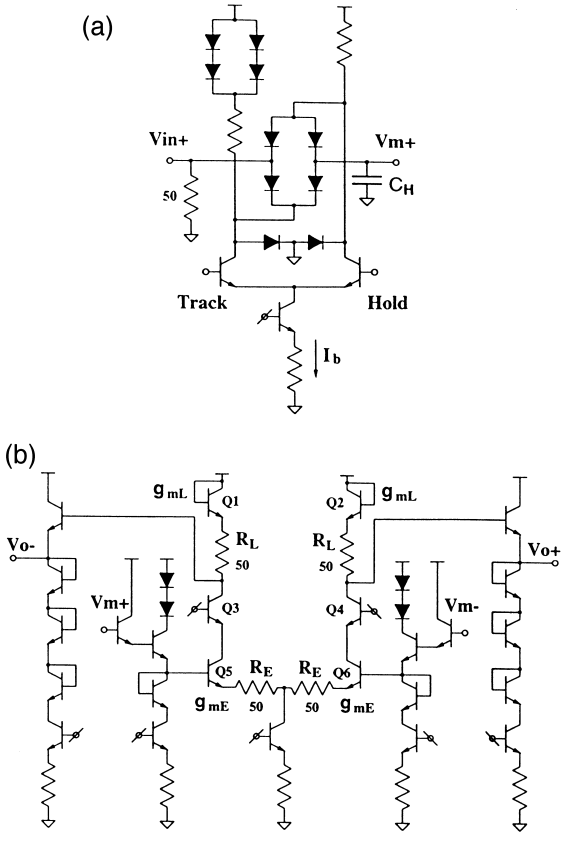


Fig. 16. T/H circuit schematics. (a) Core of T/H circuit. The actual circuit is differential but is shown single-ended for simplicity. (b) Output buffer.

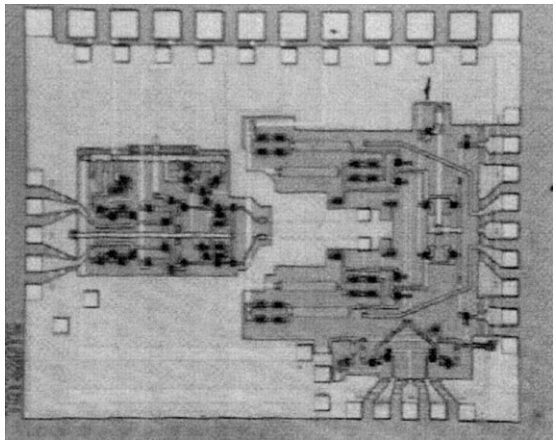


Fig. 17. Chip photo of the T/H circuit with GaAs HBT.

8.2.2. Implementation

The differential core part in Fig. 16a uses 16 HBTs and 20 SBDs dissipating 570 mW and the output buffer in Fig. 16b uses 27 HBTs and 4 SBDs with 420 mW. The whole T/H circuit occupies a chip area of 1.4×1.75 mm^2 (Figs. 16 and 17), and its layout is rather conservative to avoid thermal problems due to the GaAs substrate [27]. A summary of the measured results is shown in Table 8, and the reader can refer to Refs. [19,33] for details of the measurement.

9. Aperture jitter effects on high-speed ADC system

9.1. Problem formulation

In wideband high-precision sampling systems, the aperture jitter or phase noise [1,6,29] of the sampling clock is crucial. Consider a sinusoidal input $V_{in}(t) =$

Table 8
Measured performance of the T/H circuit with GaAs HBT

Sampling frequency	3.0 GS/s
Analog bandwidth	6.0 GHz
Analog input (differential)	1.0 $V_{p\text{-}p}$
Droop rate	2.1 mV/ns
Feedthrough	−46.0 dB at 500 MHz
Hold pedestal	$< \pm 10$ mV
Power consumption	990 mW
HBT count	43
SBD	24
Chip size	1.4×1.75 mm^2

$A\cos(2\pi f_{\text{in}}t)$, and a sampling system, which samples it at time $t = nT_s + \epsilon_n$ (Figs. 18 and 19), where T_s is the sampling period and ϵ_n is the aperture jitter; we assume that ϵ_n follows a Gaussian distribution of $N(0,\sigma_j^2)$. Then, we obtain the sampling system output of $V_{\text{out}}(nT_s) = V_{\text{in}}(nT_s + \epsilon_n)$, and the error between the input and output is given by:

$$V_{\text{out}}(nT_s) - V_{\text{in}}(nT_s) \approx \epsilon_n \frac{dV_{\text{in}}(t)}{dt}\Big|_{t=nT}. \quad (2)$$

where

$$2\pi f_{\text{in}}\sigma_j \ll 1 \quad (3)$$

is assumed. We see that the error is proportional to the signal slew-rate $(dV_{\text{in}}(t))/(dt)$ as well as the jitter ϵ_n. Therefore, note that as the input signal frequency f_{in} becomes higher, the aperture jitter effect becomes more serious because the signal slew-rate is proportional to f_{in}, and hence in wideband sampling systems, the aperture jitter effect is very problematic. Shinagawa et. al. showed in Shinagawa that with the assumption of Eq. (3) the noise power due to the jitter is given by:

$$P_j = 2\pi^2 f_{\text{in}}^2 A^2 \sigma_j^2. \quad (4)$$

However in wideband sampling systems such as wideband digitizing oscilloscopes, which incorporate an equivalent-time sampling function [5], the input signal frequency f_{in} is so high for a given σ_j that $2\pi f_{\text{in}}\sigma_j \ll 1$ does not hold. In this section, we show the exact formula of the noise power due to the aperture jitter for almost any input signal without assuming $2\pi f_{\text{in}}\sigma_j \ll 1$.

9.2. Aperture jitter effects for (almost) any input signal

Recently, Awad [2] derived the exact formula for the noise power due to the jitter for a sinusoidal input without the assumption of Eq. (3).

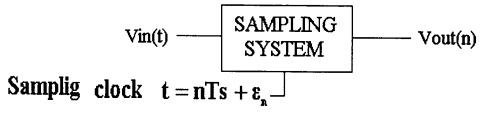


Fig. 18. A sampling system where $V_{\text{in}}(t)$ is an analog input and $V_{\text{out}}(n)$ is sampled output $(n = \ldots -2, -1, 0, 1, 2, \ldots)$. It is assumed that the sampling clock has a period of T_s with the aperture jitter ϵ.

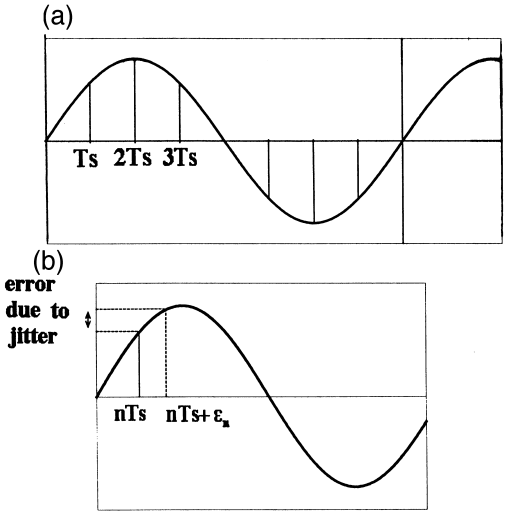


Fig. 19. (a) The sampling system in Fig. 18 samples a sinusoidal input with a sampling period of T_s. (b) Error of the sampled output due to the aperture jitter. When the sampling clock has the aperture jitter ϵ_n at nth clock period, the sampled output is $V_{\text{in}}(nT_s + \epsilon_n)$ while the ideal output is $V_{\text{in}}(nT_s)$; hence, the error due to the aperture jitter is given by $V_{\text{in}}(nT_s + \epsilon_n) - V_{\text{in}}(nT_s)$.

Fact (i). The exact noise power P_j due to the jitter for $V_{\text{in}}(t) = A\cos(2\pi f_{\text{in}}t)$ is given by:

$$P_j = \lim_{N\to\infty} \frac{1}{N} \sum_{n=0}^{N-1} \left[V_{\text{out}}(nT_s) - V_{\text{in}}(nT_s)\right]^2$$
$$= A^2\left[1 - \exp\left(-2\pi^2 f_{\text{in}}^2 \sigma_j^2\right)\right]. \quad (5)$$

Note that P_j does not depend on a sampling period of T_s.(ii) When $2\pi f_{\text{in}}\sigma_j \ll 1$,

$$P_j \approx A^2\left[1 - \left(1 - 2\pi^2 f_{\text{in}}^2 \sigma_j^2\right)\right] = 2\pi^2 f_{\text{in}}^2 \sigma_j^2 A^2,$$

which corresponds to the result in Ref. [30].

Next, we will describe the noise power and SNR due to the aperture jitter for (*almost*) *any input signal* [20].

Proposition. *(i) When the input $V_{in}(nT_s)$ is given by a Fourier series:*

$$V_{\text{in}}(nT_s) = \frac{a_0}{2} + \sum_{k=1}^{\infty} \left[a_k \cos(2\pi k f_0 nT_s) + b_k \sin(2\pi k f_0 nT_s)\right], \quad (6)$$

then the noise power P_j due to aperture jitter is given by

$$P_j = \sum_{k=1}^{\infty} \left(a_k^2 + b_k^2\right)\left[1 - \exp\left(-2\pi^2 (kf_0)^2 \sigma_j^2\right)\right]. \tag{7}$$

(iii) This idea can be extended to any stationary input signal (i.e., its Fourier transform exists, $\int_{-\infty}^{\infty} |V_{\text{in}}(t)| \mathrm{d}t < \infty$) using Fourier transform. Suppose that the Fourier transform of $V_{in}(t)$ is $F(j\omega)$, then the noise power P_j due to the jitter is given by:

$$P_j = \int_{-\infty}^{\infty} |F(j\omega)|^2 \left[1 - \exp\left(-\frac{\omega^2 \sigma_j^2}{2}\right)\right] \mathrm{d}\omega.$$

The reader can refer to Ref. [20] *for the numerical simulation results.*

10. Timing skew problem in time-interleaved ADC system

The time-interleaving method is very effective when implementing a high-sampling-rate ADC with relatively slow circuits (actually many of the ADCs for very wideband digitizing oscilloscopes use this method, where each channel ADC employs the folding/interpolation ADC implemented with Bipolar transistors [25,26], and this fact motivates the present theoretical study.) Fig. 20a shows its configuration where each of M channel ADCs (ADC_1, $\text{ADC}_2, \ldots,$ ADC_m) precedes a corresponding sample-hold circuit (SH_1, $\text{SH}_2, \ldots,$ SH_m) and each operates with one of M phase clocks (CK_1, $\text{CK}_2, \ldots,$ CK_m) respectively. The sampling rate of the ADC as a whole is M times the channel sampling rate. However, this interleaved ADC system suffers from clock skew effects (Fig. 20b) [13,21]. Suppose that the clocks $\text{CK}_1, \text{CK}_2, \ldots, \text{CK}_M$ have (fixed) timing skews $\mathrm{d}t_1$, $\mathrm{d}t_2, \ldots,$ $\mathrm{d}t_M$. These clock skews are considered as the jitter of the whole ADC sampling timing and we will calculate exactly the noise power due to these skews [20].

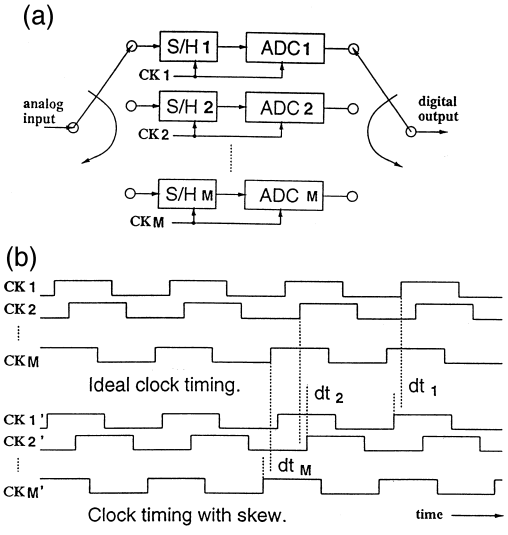


Fig. 20. (a) Time-interleaved ADC system. (b) Clock skew in the time-interleaved ADC system.

Proposition. *Consider a sinusoidal input $V_{in}(t) = A \cos(2\pi f_{in} t)$ for the interleaved ADC system, then the noise power P_s due to the timing skews is given by:*

$$P_s = \lim_{N\to\infty} \frac{1}{N} \sum_{n=0}^{N-1} \left(V_{\text{out}}(nT_s) - V_{\text{in}}(nT_s)\right)^2$$
$$= A^2 \left(1 - \frac{1}{M} \sum_{p=1}^{M} \cos(2\pi f_{\text{in}} \mathrm{d}t_p)\right). \tag{8}$$

Note that P_s in Eq. (8) *is different from P_j in* Eq. (5)*, and this difference can be important in wideband sampling systems.*

11. Discussion on high-speed ADC standardization for measuring instrument applications

This section addresses several issues relating to standardizing the specifications of high-speed ADCs for measuring instrument applications.

11.1. Sampling speed

Many scientists and engineers think that the sampling speed for the high-speed ADC should be clearly standardized in terms of the input signal [10,11]. In many cases, papers and/or data sheets claim like ''the sampling speed of this ADC is f_s,'' in spite of the fact that its number of effective bits drops rapidly

as the input frequency approaches $f_s/2$. In such a case, the speed of two ADCs cannot be compared with their claimed sampling speed. Also, one may say that an ideal ADC with resolution of N-bit and sampling speed of f_s should have the number of effective bits better than N-0.5 bits upto the input frequency of $f_s/2$. However, this is not always true in twofold. On the one hand, the input frequency can be much higher than $f_s/2$ for the ADC used in a wideband sampling oscilloscope, which incorporates equivalent time sampling. On the other hand, the input frequency is often upto $f_s/4$ (due to the design of the preceding analog anti-aliasing filter) for the ADC used in a real-time sampling oscilloscope, and for some measuring instrument applications, many sampling points are required for a transient input signal, and sometimes digital interpolation is performed between the adjacent sampling points.

11.2. Accuracy

For waveform measurement applications, the number of effective bits is often not enough to specify the accuracy of an ADC; the number of effective bits or SNR shows just its *averaged* performance, however for such applications the *worst case* performance is also important. Intuitively speaking, the effective bits are calculated from the following averaged error:

$$E_{\mathrm{avrg}} = \frac{1}{N}\sum_{n=0}^{N-1}\frac{\left(V_{\mathrm{in}}(nT_s) - V_{\mathrm{out}}(nT_s)\right)^2}{V_{\mathrm{in}}(nT_s)^2}.$$

On the other hand, worst case error (performance) may be defined as follows:

$$E_{\mathrm{wrst}} = \max_{0\le n\le N-1}|V_{\mathrm{in}}(nT_s) - V_{\mathrm{out}}(nT_s)|.$$

It degrades the waveform measurement seriously if the output $V_{\mathrm{out}}(nT_s)$ shows some glitches even though there are no glitches in the input signal $V_{\mathrm{in}}(nT_s)$, and the worst case error (which may be caused by the comparator metastability, sparkles, etc.) will specify this performance, and this concept should be standardized even though the word error rate (or bit error rate) is similar to this [10,11].

11.3. Time-interleaved ADC

A time-interleaved ADC is extensively used for the high-speed waveform measurement instruments; however, mismatches among its channel ADCs cause errors. In the time-interleaved ADC, there are some errors, which are serious for waveform measurements and which can not be specified by the number of effective bits. For example, the output of the time-interleaved ADC may show a limit-cycle for some DC inputs even though the offset mismatches among its channel ADCs is calibrated to better than 1/2 LSB and the other characteristics are perfectly matched. The output of the ADC should be constant for a DC output, however, the output of the interleave ADC may show a limit-cycle (called ''1 LSB noise''), which is highly undesirable for waveform measurement applications. Some instruments cancel this ''1 LSB noise'' by digital filtering following the ADC. In our opinion, the method of specifying inherent errors in the time-interleaved ADC should be standardized.

12. Conclusions

We have described three high-speed ADCs and a T/H circuit for measuring instrument applications: a 6-bit 800 MS/s ADC with SiGe HBTs, a 7-bit 1 GS/s ADC with SiGe HBTs, a 6-bit 3 GS/s ADC with GaAs HBTs and a 6-bit 3 GS/s T/H circuit with GaAs HBTs. We have shown that SiGe HBTs and GaAs HBTs have technological potential for ultra-high-speed ADC systems. Motivated by the need to implement high-speed and wideband ADC systems, we have derived three theoretical results: (i) an error correction algorithm for the folding/interpolation ADC and its limitation for high-frequency inputs, (ii) aperture jitter effects in wideband ADCs and (iii) timing skew effects in a time-interleaved ADC system. Based on these, we have addressed several issues relating to standardizing the specifications of high-speed ADC for measuring instrument applications.

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References

[1] A.A. Abidi, ''How Phase Noise Appears in Oscillators,'' Workshop on Advances in Analog Circuit Design, Italy,1997, April.

[2] S.S. Awad, Analysis of accumulated timing-jitter in the time domain, IEEE Trans. Instrum. Meas. l47 (1) (1998) 69–74, (Feb.).

[3] K. Bult, A. Buchwald, An embedded 240 mW 10 b 50 MS/s CMOS ADC in 1 mm^2, IEEE J. Solid-State Circuits 32 (12) (1997) 1887–1895, (Dec.).

[4] W.T. Colleran, A.A. Abidi, A 10 bit 75 MS/s two-stage pipelined bipolar A/D converter, IEEE J. Solid-State Circuits 28 (12) (1993) 1187–1199, (Dec.).

[5] W.L. Gans, The measurement and deconvolution of time jitter in equivalent-time waveform samplers, IEEE Trans. Instrum. Meas. 32 (1) (1983) 126–133, (March).

[6] A. Hajimiri, T. Lee, A general theory of phase noise in electrical oscillators, IEEE J. Solid-State Circuits 33 (2) (1998) 179–193, (Feb.).

[7] D.L. Harame, J.H. Comfort, J.D. Cressler, E.F. Crabe, J.Y.-C. Sun, B.S. Meyerson, T. Tice, Si/SiGe epitaxial-base transistors: Part I. Materials, physics and circuits, IEEE Trans. Electron Devices 42 (3) (1995) 435–468, March.

[8] D.L. Harame, J.H. Comfort, J.D. Cressler, E.F. Crabe, J.Y.-C. Sun, B.S. Meyerson, T. Tice, Si/SiGe epitaxial-base transistors: Part II. Process integration and analog applications, IEEE Trans. Electron Devices 42 (3) (1995) 469–482, (March).

[9] G. Hoogzaad, R. Roovers, A 65 mW 10 b 40 MS/s BiCMOS nyquist ADC in 0.8 mm^2, in: Tech. Digest of International Solid-State Circuits Conference, San Francisco,1999, pp. 320–321, (Feb.).

[10] IEEE Standard for Digitizing Waveform Recorders, IEEE Std 1057 (994).

[11] IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters, IEEE Std 1241 (1998).

[12] in: B. Jalali, S.J. Pearton (Eds.), InP HBTs: Growth, Processing and Applications,1995, Artech House.

[13] Y.-C. Jeng, Digital spectra of nonuniformly sampled signals: fundamentals and high-speed waveform digitizers, IEEE Trans. Instrum. Meas. 37 (2) (1988) 245–251, (June).

[14] K. Kattmann, J. Barrow, A technique for reducing differential nonlinearity errors in flash A/D converters, in: Tech. Digest of International Solid-State Circuits Conference, San Francisco,1991, pp. 170–171, (Feb.).

[15] H. Kobayashi, H. Sakayori, T. Tobari, H. Matsuura, Error correction algorithm for folding/interpolation ADC, in: Proc. of International Symposium on Circuits and Systems, Seattle vol. 11995, pp. 700–703, (May).

[16] H. Kobayashi, T. Mizuta, K. Uchida, H. Matsuura, A. Miura, T. Yakihara, S. Oka, D. Murata, A high-speed 6-bit ADC with SiGe HBT, IEICE Trans. Fundam. Electron. E81-A (3) (1998) 389–397, (March).

[17] H. Kobayashi, T. Mizuta, K. Uchida, H. Matsuura, A. Miura, T. Yakihara, S. Oka, D. Murata, Design consideration for folding/interpolation ADC with SiGe HBT, in: Proc. of IEEE Instrumentation and Measurement Technology Conference, Ottawa,1997, pp. 1142–1147, (May).

[18] H. Kobayashi, T. Mizuta, K. Uchida, H. Matsuura, K. Kobayashi, AC performance improvement of folding/interpolation ADC with SiGe HBT, in: Proc. of IEEE Instrumentation and Measurement Technology Conference, St. Paul, MN,1998, pp. 1385–1390, (May).

[19] H. Kobayashi, T. Tobari, H. Matsuura, A. Miura, M. Yamanaka, T. Yakihara, S. Kobayashi, S. Oka, T. Fujita, D. Murata, System architecture and key components of a multi-Giga-Hertz A/D converter with HBT, in: Proc. of IEEE Instrumentation and Measurement Technology Conference,1996, pp. 1160–1166, (June).

[20] H. Kobayashi, M. Morimura, K. Kobayashi, Y. Onaya, Aperture jitter effects on wideband sampling systems, in: Proc. of IEEE Instrumentation and Measurement Technology Conference, Venice, Italy,1999, pp. 880–885, (May).

[21] A. Montijo, K. Rush, Accuracy in interleaved ADC system, Hewlett-Packard Journal (1993) 38–46, (Oct.).

[22] K.R. Nary, R. Nubling, S. Beccue, W.T. Colleran, J. Penney, K.-C. Wang, An 8-bit 2 Giga sample per second analog to digital converter, in: GaAs IC Symposium Tech. Digest,1995, pp. 303–306, (Oct.).

[23] R.V. Plassche, Integrated Analog-to-Digital and Digital-to-Analog Converters, Kluwer Academic Publishing, 1994.

[24] K. Poulton, K.L. Knudsen, J.J. Corcoran, K.-C. Wang, R.B. Nubling, R.L. Pierson, M.-C.F. Chang, P.M. Asbeck, R.T. Huang, A 6-b 4 GSa/s GaAs HBT ADC, IEEE J. Solid-State Circuits 30 (10) (1995) 1109–1117, (Oct.).

[25] K. Poulton, K.L. Knudsen, J. Kerley, J. Kang, J. Tani, E. Cornish, M. VanGrouw, An 8 GS/s 8 bit ADC system, in: Symposium on VLSI Circuits Digest of Technical Paper, Kyoto,1997, pp. 24–24, (June).

[26] K. Poulton, J. Concoran, T. Honak, A 1 GHz 6 b ADC system, IEEE J. Solid-State Circuits 22 (6) (1987) 962–970, (Dec.).

[27] K. Poulton, K.L. Knudsen, J.J. Corcoran, K.-C. Wang, R.L. Pierson, R.B. Nubling, M.-C.F. Chang, Thermal design and simulation of biploar integrated circuits, IEEE J. Solid-State Circuits 25 (10) (1992) 1379–1387, (Oct.).

[28] B. Razavi, Principles of Data Conversion System Design, IEEE Press, 1995.

[29] B. Razavi, A study of phase noise in CMOS oscillators, IEEE J. Solid-State Circuits 31 (3) (1996) 331–343, (Mar.).

[30] M. Shinagawa, Y. Akazawa, T. Wakimoto, Jitter analysis of high-speed sampling systems, IEEE J. Solid-State Circuits 25 (1) (1990) 220–224, (Feb.).

[31] S. Subbanna, D. Ahlgren, D. Harame, B. Meyerson, How SiGe evolved into a manufacturable semiconductor production process, in: Tech. Digest of International Solid-State Circuits Conference, San Francisco,1999, pp. 66–67, (Feb.).

[32] Y. Tamba, K. Yamakido, A CMOS 6 b 500 MS/s ADC for

a hard disk drive read channel, in: Tech. Digest of International Solid-State Circuits Conference, San Francisco,1999, pp. 324–325, (Feb.).
[33] T. Tobari, H. Kobayashi, K. Uchida, H. Matsuura, M. Yamanaka, S. Kobayashi, T. Fujita, A. Miura, Track/hold circuit in GaAs HBT process, IEICE Trans. Fundam. E80-A (3) (1997) 454–460, (March).
[34] J. Valburg, R.J. Plassche, An 8 b 650 MHz folding ADC, IEEE J. Solid-States Circuits 27 (12) (1992) 1662–1666, (Dec.).
[35] P. Vorenkamp, R. Roovers, A 12 b 60 MS/s cascaded folding/interpolating ADC, IEEE J. Solid-State Circuits 32 (12) (1997) 1876–1886, (Dec.).
[36] T. Wakimoto, Y. Akazawa, S. Konaka, Si Bipolar 2 GHz 6 bit flash AD conversion LSI, IEEE J. Solid-States Circuits 23 (6) (1988) 1345–1350, (Dec.).
[37] K. Yoon, S. Park, W. Kim, A 6 b 500 MS/s CMOS flash ADC with a background interpolated auto-zeroing technique, in: Tech. Digest of International Solid-State Circuits Conference, San Francisco,1999, pp. 326–327, (Feb.).
[38] P. Xiao, K. Jenkins, M. Soyuer, H. Ainspan, J. Burghartz, H. Shin, M. Dolan, D. Harame, A 4 b 8 GS/s A/D converter in SiGe bipolar technology, in: Tech. Digest of International Solid-State Circuits Conference, San Francisco,1997, pp. 124–125, (Feb.).

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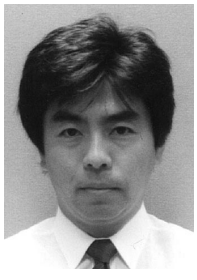
His current research interests are in the development of Si compound semiconductor (SiGe, etc.) devices for high-frequency systems.



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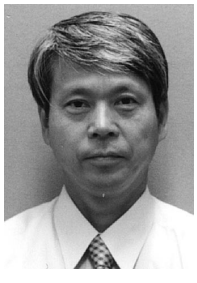

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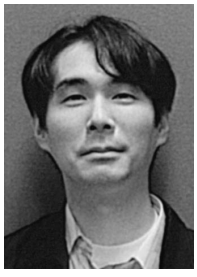

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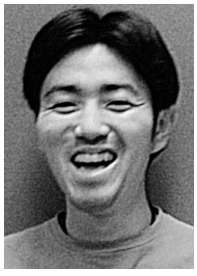
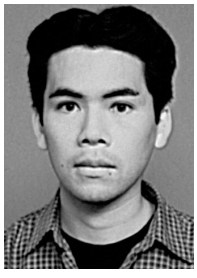


Atsushi Nakajima graduated from Chyukyo High School in 1991. He joined Yokogawa Electric in 1991 and joined Teratec in 1996. He has been engaged in the process engineering.



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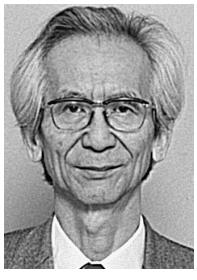

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