IEICE TRANS. FUNDAMENTALS, VOL.E89–A, NO.4 APRIL 2006

PAPER Special Section on Selected Papers from the 18th Workshop on Circuits and Systems in Karuizawa

Complex Bandpass ΔΣAD Modulator Architecture without I, Q-Path Crossing Layout

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SUMMARY This paper proposes a new architecture for multibit complex bandpass ΔΣAD modulators with built-in Switched-Capacitor (SC) circuits for application to Low-IF receivers such as used for Bluetooth and WLAN. In the realization of complex bandpass ΔΣAD modulators, we face the following problems: (i) SNR of AD converter is deteriorated by mismatches between internal analog I and Q paths. (ii) Layout design becomes complicated because of signal lines crossing by complex filter and feedback from DAC for I and Q paths in the complex modulator, and this increases required chip area. We propose a new structure for a complex bandpass ΔΣAD modulator which can be completely divided into two paths without layout crossing, and solves the problems mentioned above. The two parts of signal paths and circuits in the modulator are changed for I and Q while CLK is changed for High/Low by adding multiplexers. Symmetric circuits are used for I and Q paths at a certain timing, and they are switched by multiplexers to those used for Q and I paths at another timing. Therefore the influence from mismatches between I and Q paths is reduced by dynamic matching. As a result, the modulator is divided into two separate parts without crossing signal lines between I and Q paths and its layout design can be greatly simplified compared with conventional modulators. We have conducted MATLAB simulations to confirm the effectiveness of the proposed structure.

key words: *complex bandpass ΔΣAD modulator, I, Q path mismatches, dynamic matching, multiplexer*

1. Introduction

In the RF receiver of communication systems such as cellular phones and wireless LANs, low-IF receiver architecture is frequently used. In conventional low-IF receiver architectures, two real (one input and one output) ΔΣAD modulators are used for In-phase (I) and Quadrature (Q) paths. Its disadvantage is that not only input signals but also image signals are converted by ADCs. On the other hand, complex bandpass ΔΣAD modulators can provide superior performance to a pair of real bandpass ΔΣAD modulators of the same order. They process just input I and Q signals and not image signals, and AD conversion can be realized with low power dissipation, so they are desirable for such low-IF receiver applications [1]–[4]. The performance of the complex bandpass ΔΣAD modulator is degraded by mismatches between I and Q paths which cause both signal and quantization noise in the mirror image band and alias into the design signal band, thus decrease the SNDR of the complex modulator.

This paper presents a new Switched-Capacitor topology architecture which is suitable for complex bandpass ΔΣAD modulators and compensates for mismatches between I and Q paths. The new architecture reduces the amount of mirror image band quantization noise aliased into the signal band. It also simplifies the modulator structure into a symmetrical configuration with no crossing of signal lines between the two circuit parts, and thus required chip area becomes smaller and its layout design can be simplified. Moreover, this technique can be extended to multi-bit modulators suitable for complex bandpass DWA algorithm [5]–[7].

2. New Structure of Complex Bandpass Filter

Figure 1(a) shows a conventional complex bandpass filter and the inputs and outputs are written as follows:

$$I_{out}(n) = I_{in}(n-1) - Q_{out}(n-1) \quad (1)$$

$$Q_{out}(n) = Q_{in}(n-1) + I_{out}(n-1) \quad (2)$$

Figure 1(b) shows the proposed structure of a complex bandpass filter, where four multiplexers (MUX) are added to the conventional structure. The select signal (SEL) for the MUXs is generated by half of CLK in Z^{-1} block and they are synchronized. Compared to the conventional structure, we see that the proposed complex filter can be divided into two separate parts without any crossing of signal lines,

The proposed complex filter operates with two states; in state 1 (in Fig. 1(c)), the upper part of circuit is used for I path, while the lower path is for Q path. In state 2 (in Fig. 1(d)), the upper part of circuit is used for Q path, while the lower path is for I path. In our proposed configuration, the input I and Q signals alternate between the

Manuscript received June 27, 2005.
Final manuscript received October 3, 2005.

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DOI: 10.1093/ietfec/e89–a.4.908

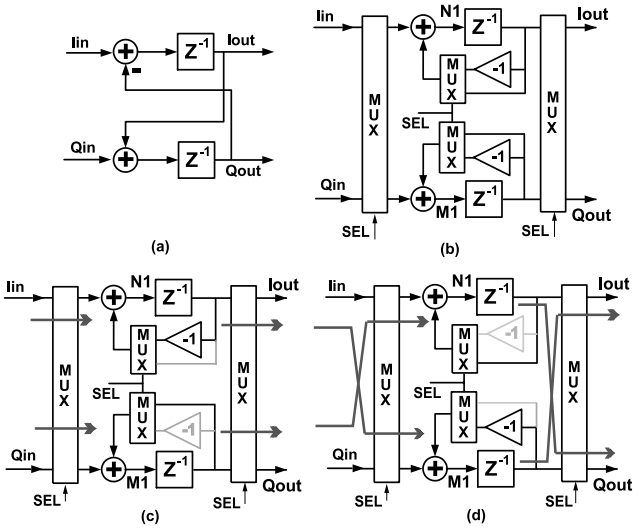

Fig. 1 (a) Conventional complex bandpass filter. (b) Proposed structure of a complex bandpass filter. (c) Operation of the proposed complex bandpass filter (state 1). (d) Operation of the proposed complex bandpass filter (state 2).

above two parts of the complex filter by SEL signal defined above. Thus the inputs and outputs are written as the same as Eqs. (1) and (2).

3. Conventional Complex Bandpass ΔΣAD Modulator

Figure 2 shows a conventional configuration of a discrete-time second-order complex bandpass ΔΣAD modulator [8], which is composed of a second-order complex bandpass filter, two 3-bit ADCs and four 3-bit DACs. Multi-bit ADCs/DACs are used inside the modulator to obtain high SNR with a low-order loop filter and relax the required performance for OP-Amps. MUXs and data-weighted averaging (DWA) logic circuits [5]–[7] are added to reduce the effect of nonlinearities of multi-bit DACs inside the modulator.

The input and output of the complex bandpass ΔΣAD modulator shown in Fig. 2 are given by

$$I_{out} + jQ_{out} = z^{-2}\left[\frac{1}{2}(I_{in} + jQ_{in}) + (z-j)^2(E_I + jE_Q)\right].$$

Internal signals in Fig. 2 can be written as follows:

$$I_1(n+1) = a_1 \cdot I_{in}(n+1) + b_1 \cdot DAC1(n+1) - Q_1(n) \quad (3)$$

$$Q_1(n+1) = a_1 \cdot Q_{in}(n+1) + b_1 \cdot DAC2(n+1) + I_1(n) \quad (4)$$

$$I_2(n+1) = a_2 \cdot I_1(n) + b_2 \cdot DAC3(n+1) - Q2(n) \quad (5)$$

$$Q_2(n+1) = a_2 \cdot Q_2(n) + b_2 \cdot DAC4(n+1) + I_2(n). \quad (6)$$

Here, the inputs of DAC1 and DAC4 are fedback from the output of ADCI, while the inputs of DAC2 and DAC3 are fedback from the output of ADCQ.

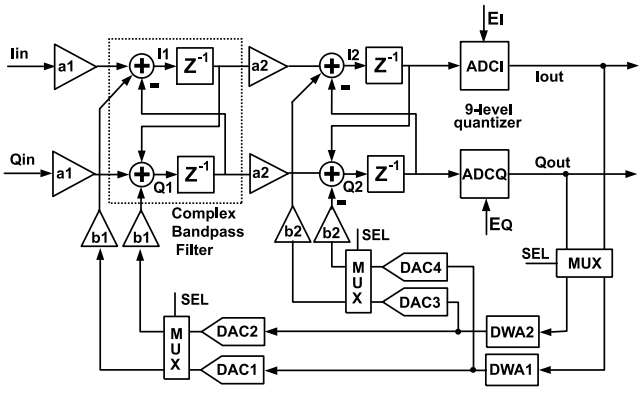

Fig. 2 Conventional discrete-time second-order complex bandpass ΔΣAD modulator. (Here a_1 =1/3, b_1 = −2/3, a_2 = 3/2, b_2 = 2)

The following two problems arise when implementing the conventional configuration in Fig. 2.

1. **Complexity of chip layout design:**
   There are many I and Q signal crossing lines in the complex bandpass ΔΣAD modulator as shown in Fig. 2. There are not only signal crossings between the I and Q paths of the complex filter in the forward paths, but also signal crossings between the feedback paths from ADCs through four DACs in I and Q paths. As their result, the signal lines become long, which leads to large chip area, and crosstalk may occur, and also large power dissipation may be needed to drive large parasitic capacitances.
2. **Mismatches between I and Q paths:**
   Mismatches between forward I and Q paths cause an image signal in Fig. 2, and the quantization noise of the mirror image band aliases into the design signal band, which degrades the modulator SNR (see Appendix). Some ideas [10]–[13] have been proposed to reduce their influence, but they are not very suitable for our modulator structure.

Therefore, we propose a new architecture of a complex bandpass ΔΣAD modulator to solve the above two problems, and we have conducted MATLAB simulations to verify its effectiveness.

Remark The effect of mismatches among DACs in feedback paths can be reduced by our already proposed DWA algorithm [5], [6] because it alternates the DACs for I and Q paths every sample cycle, and hence it is not a problem here.

4. Proposed Structure of Complex Bandpass ΔΣAD Modulator

Figure 3 shows the structure of our proposed complex bandpass ΔΣAD modulator. First, we will show that the proposed structure is equivalent to the conventional one shown in Fig. 2 when their circuits are ideal (no mismatches).

At time $n = 2k - 1$ (Fig. 4):

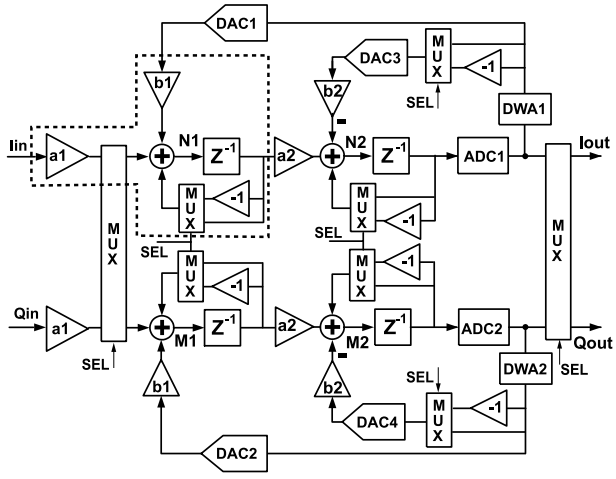

Fig. 3 Proposed structure of a complex bandpass ΔΣAD modulator.

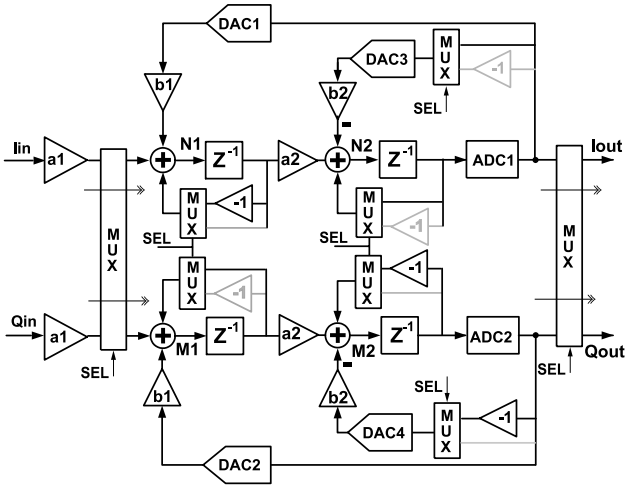

Fig. 4 Operation of proposed modulator (at time $n = 2k - 1$).

The input analog signal for the *upper* part circuits is I_{in} while the one for the *lower* part circuits is Q_{in}. Also the output digital signal from the *upper* part ADC1 is I_{out}, while the one from the *lower* part ADC2 is Q_{out}. Then the internal signals relationship is given as follows:

$$N_1(2k) = a_1 \cdot I_{in}(2k) + b_1 \cdot DAC1(2k) - N_1(2k-1) \quad (7)$$

$$M_1(2k) = a_1 \cdot Q_{in}(2k) + b_1 \cdot DAC2(2k) + M_1(2k-1) \quad (8)$$

$$N_2(2k) = a_2 \cdot N_1(2k-1) + b_2 \cdot DAC2(2k) + N_2(2k-1) \quad (9)$$

$$M_2(2k) = a_2 \cdot M_1(2k-1) + b_2 \cdot DAC4(2k) - M_2(2k-1). \quad (10)$$

Here

$$k = \ldots -2, -1, 0, 1, 2, 3, \ldots$$

Let

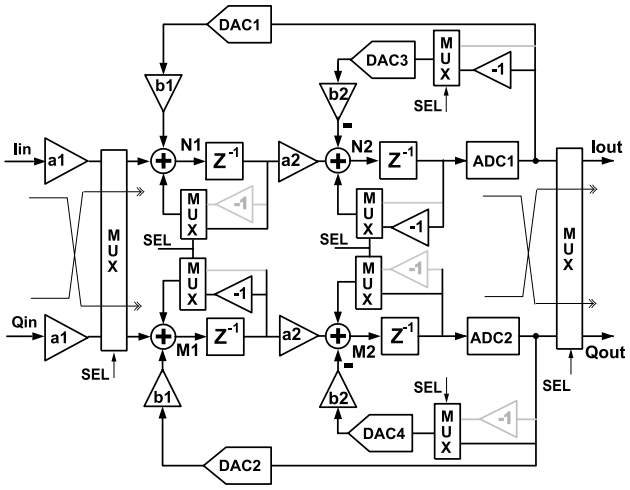

Fig. 5 Operation of proposed modulator (at time $n = 2k$).

$$N_1(2k-1) = Q_1(2k-1)$$
$$M_1(2k-1) = I_1(2k-1)$$
$$N_2(2k-1) = I_2(2k-1)$$
$$M_2(2k-1) = Q_2(2k-1).$$

Then we see from Fig. 4 that ADC1 output (I signal) is fedback to DAC1 and DAC3, and ADC2 output (Q signal) is to DAC2 and DAC3. Thus Eqs. (7) and (3), Eqs. (8) and (4), Eqs. (10) and (5), Eqs. (9) and (6) have the same forms respectively.

At time $n = 2k$ (Fig. 5):

The input analog signal for the *lower* part circuits is I_{in} while the one for the *upper* part circuits is Q_{in}. Also the output digital signal from the *lower* part ADC2 is I_{out}, while the one from the *upper* part ADC1 is Q_{out}. Then we have the followings:

$$N1(2k+1) = a_1 \cdot Q_{in}(2k+1) + b_1 \cdot DAC1(2k+1) - N_1(2k) \quad (11)$$

$$M_1(2k+1) = a_1 \cdot I_{in}(2k+1) + b_1 \cdot DAC2(2k+1) + M_1(2k) \quad (12)$$

$$N_2(2k+1) = a_2 \cdot N_1(n) + b_2 \cdot DAC3(2k+1) + N2(2k) \quad (13)$$

$$M_2(2k+1) = a_2 \cdot M_1(2k) + b_2 \cdot DAC4(2k+1) - M_2(2k). \quad (14)$$

Let

$$N_1(2k) = I_1(2k)$$
$$M_1(2k) = Q_1(2k)$$
$$N_2(2k) = Q_2(2k)$$
$$M_2(2k) = I_2(2k).$$

Similarly we see from Fig. 5) that ADC1 output (Q signal) is fedback to DAC1 and DAC3 and ADC2 output (I signal) is fedback to DAC2 and DAC3. Hence Eqs. (12) and (3), Eqs. (11) and (4), Eqs. (13) and (5), Eqs. (14) and (6) have

the same forms respectively.

From the above statements, we see that the proposed structure (Fig. 3) is equivalent to the conventional one (Fig. 2) when their circuits are ideal.

Also we see from Fig. 3 that the proposed structure has no crossing signal lines for either the forward paths of Z^{-1} block or the feedback paths from DACs, which is different from the conventional modulator in Fig. 2. Hence the proposed modulator can be completely divided into two separate parts and its layout design can be greatly simplified compared with the conventional one. Then its internal signal lines can be shorter, which leads to smaller chip area.

For the proposed architecture, we note that MUXs can be realized by MOS switches easily. Moreover we add MUXs which alternate the polarity of the fedback signals between +1 and −1 at every sampling time to the feedback paths of filters and DACs. This is to keep the polarity of internal complex signals so that they are processed as a complex signal form [14]. In fact we can realize this simply by chopping the two differential outputs at every sampling time.

5. Reduction of SNR Deterioration by I and Q Path Mismatches

We explain why our proposed structure can reduce the influence of mismatches between I and Q paths. Note that for the circuit surrounded by a dotted line in Fig. 3, we have the followings:

$$N_1(2k-1) = Q_1(2k-1) \text{ while } n = 2k-1,$$
$$N_1(2k) = I_1(2k) \quad \text{while } n = 2k.$$

We see that ADC1 output is for I_{out} at time $n = 2k-1$, and it is for Q_{out} at time $n = 2k$. DACs are used alternately for I and Q paths when CLK toggles. Thus the SNR degradation by mismatches between the upper and lower paths can be reduced by this dynamic matching.

Furthermore, we propose another dynamic matching technique for SC circuits to reduce the influence of mismatches between capacitors in the complex filter. Figure 6 shows the SC implementation of a complex bandpass filter which uses Z^{-1} blocks [9] in Fig. 3.

For an ideal complex modulator shown in Fig. 6 (without any mismatches), the values of the capacitors in the complex filter in Fig. 3 should have the following relationships:

$$\frac{C_{inI}}{C_{outI}} = \frac{C_{inQ}}{C_{outQ}} \left(= a_1\right),$$
$$\frac{\sum_{n=0}^{7} C_{DIn}}{C_{outI}} = \frac{\sum_{n=0}^{7} C_{DQn}}{C_{outQ}} \left(= b_1\right),$$
$$C_{CPI} = C_{CPQ} = C_{outI} = C_{outQ}.$$

However, in real chips the ratios of the capacitances do not satisfy the above equations due to process variations, which cause the mismatches between I and Q paths and the modulator SNR degrades. According to this consideration, we propose to add another dynamic matching technique for the SC filter in the first stage of the modulator (Fig. 3) to reduce the influence of capacitor mismatches. The SC filter circuit operates as follows (Fig. 7):

1. C_{inI} and C_{inQ} are fixed for I and Q paths in the front of the input MUX. Input signals I_{in} and Q_{in} charge to C_{inI} and C_{inQ} at first, and then they transfer the charges to upper and lower paths alternately by the input MUX. This idea is based on our simulation result that the influence of mismatches in C_{inI} and C_{inQ} is small.
2. We exchange capacitors for C_{OUTI} and C_{CPI}, C_{OUTQ} and C_{CPQ} very sampling time by MUXs, in order to reduce the influence of mismatches between C_{OUTI} and C_{CPI}, C_{OUTQ} and C_{CPQ}.

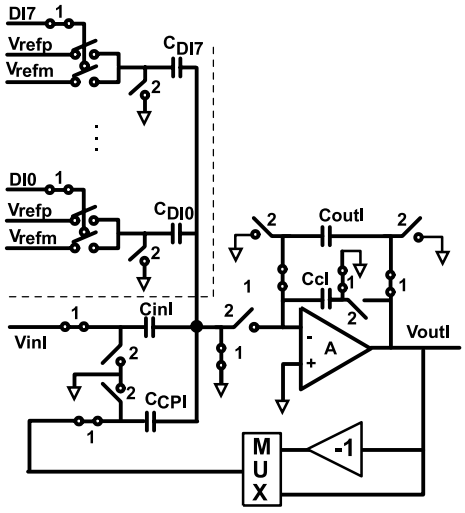

Fig. 6 SC implementation of proposed complex bandpass filter (which is the surrounded part by a dotted line in Fig. 3).

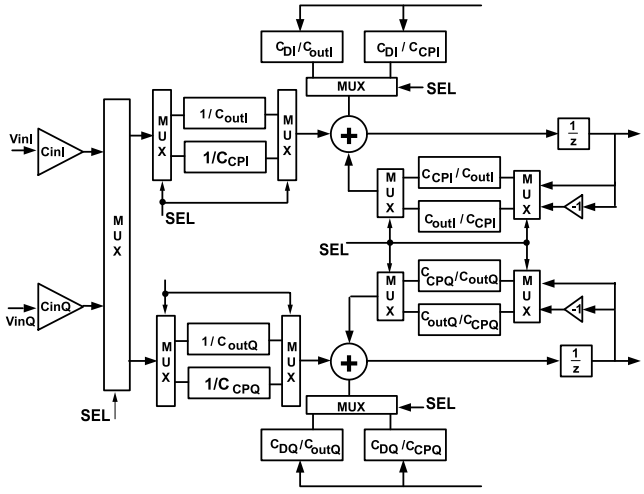

Fig. 7 Equivalent circuit of the proposed first-stage filter in the modulator which can reduce the influence of capacitor mismatches by dynamic matching.

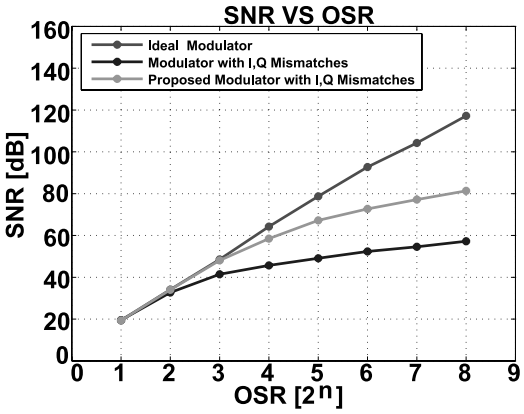

Fig. 8 Comparison for SNR of modulators in three cases. (parameter as Table 1).

With the above configuration and operation, we can reduce influence of mismatches in the modulator further. Since the influence of mismatches in the second-stage filter is smaller, we form the above operation for the first-stage only.

6. Simulation of Proposed Architecture

We have conducted MATLAB simulations to confirm the effectiveness of the proposed architecture with dynamic matching. A second-order complex bandpass modulator with internal ADCs/DACs of 9-level resolution (in Fig. 2 or Fig. 3) was used for the simulation with the following three cases:

1. An ideal modulator (in Figs. 2, 3) without any mismatches and nonlinearities between I and Q paths is used.
2. A modulator in Fig. 2 with I and Q paths mismatches, and internal DACs with nonlinearities is used.
3. A modulator which employs the proposed architecture (in Fig. 3) and whose mismatches and nonlinearities are the same as case 2 is used.

Figure 8 shows the simulation result comparison for SNR of the modulators in three cases. We see that in case 1, SNR of the ADC increases as OSR increases. However in case 2 (where mismatch parameters between I and Q paths are shown in Table 1), SNR saturates as OSR increases. On the other hand, in case 3, the mismatch effects are out of signal band by dynamic matching and their influence on the modulator accuracy is reduced which leads to SNR improvement. Also Fig. 9 shows the simulation result comparison for SNR of the modulators with ideal DACs, where mismatch parameters are shown in Table 2.

7. Conclusion

We have proposed a new architecture of a multibit complex bandpass ΔΣAD modulator which is built by switched-capacitor circuits targeted for low-IF receivers applications in Bluetooth and WLAN. The influence of mismatches between I and Q paths to SNR is reduced by adding some multiplexers to the modulator circuitry, which are relatively easy to implement. As another result, the modulator is divided into two separate parts without crossing of signal lines between I and Q paths and its layout design can be greatly simplified compared with conventional circuits. The validity of the proposed architecture and circuit technique has been confirmed by MATLAB simulation. As the next step, we are designing and laying out the transistor level circuits of the multi-bit complex bandpass ΔΣAD modulator with the proposed architecture and dynamic matching technique.

Table 1 Parameter 1 for capacitor mismatches between I and Q paths.

	I	Q
C_{in}	(1−0.023)*1	(1−0.023)*1
C_{out}	(1+0.014)*3	(1−0.028)*3
C_{CP}	(1−0.035)*3	(1+0.028)*3
C_{D0}	(1−0.0004)*2	(1−0.018)*2
C_{D1}	(1−0.0014)*2	(1+0.014)*2
C_{D2}	(1+0.0018)*2	(1+0.008)*2
C_{D3}	(1−0.0006)*2	(1+0.014)*2
C_{D4}	(1+0.0012)*2	(1+0.012)*2
C_{D5}	(1+0.0012)*2	(1−0.006)*2
C_{D6}	(1−0.018)*2	(1−0.024)*2
C_{D7}	(1−0.000)*2	(1+0.000)*2

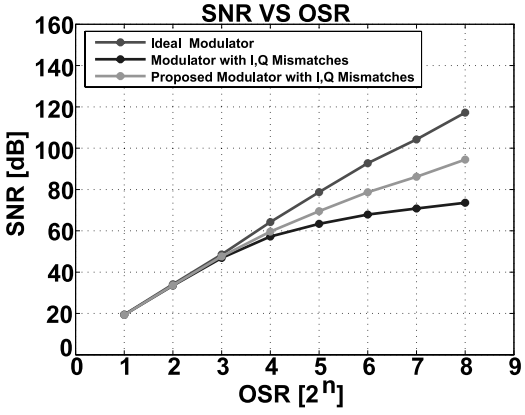

Fig. 9 Comparison for SNR of modulators with ideal DACs in three cases. (parameter as Table 2).

Table 2 Parameter 2 for capacitor mismatches between I and Q paths.

	I	Q
C_{in}	(1−0.03)*1	(1+0.03)*1
C_{out}	(1+0.014)*3	(1−0.03)*3
C_{CP}	(1−0.03)*3	(1+0.02)*3

Acknowledgement

We would like to thank STARC which supports this research. Thanks are also due to T. Kozawa, E. Imaizumi, H. Sugihara, T. Komuro, I. Sakurazawa and K. Wilkinson for valuable discussions. A part of this work was performed at Gunma University Satellite Venture Business Laboratory.

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Appendix: Resolution Deterioration by I and Q Mismatches in a Complex Bandpass ΔΣAD Modulator

According to the thinking of complex signal processing [14], we consider the reason to resolution (SNR) deteriorates by I and Q mismatches. We can get the relationship of complex inputs and outputs as following while the complex modulator shown in Fig. A· 1 without any mismatches($\alpha = 0$):

$$I_{out} + jQ_{out} = \frac{H}{1+H}(I_{in} + jQ_{in}) + \frac{1}{1+H}(E_i + jE_q).$$

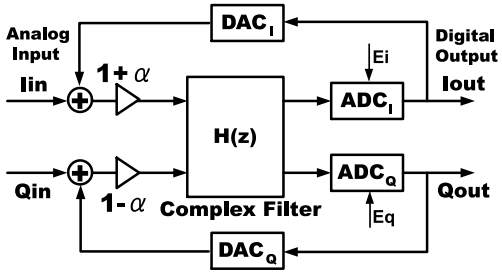

Fig. A· 1 A complex AD modulator with I and Q paths mismatches as α.

However,while the modulator with I and Q mismatches ($\alpha \neq 0$), the equation will be written as follows:

$$\begin{aligned} I_{out} + jQ_{out} &= \frac{H + (1-\alpha^2)H^2}{1 + 2H + (1-\alpha^2)H^2}(I_{in} + jQ_{in}) \\ &+ \frac{\alpha H}{1 + 2H + (1-\alpha^2)H^2}(I_{in} - jQ_{in}) \\ &+ \frac{1+H}{1 + 2H + (1-\alpha^2)H^2}(E_i + jE_q) \\ &+ \frac{\alpha H}{1 + 2H + (1-\alpha^2)H^2}(E_i - jE_q). \end{aligned}$$

Here, the quantization noise of image signal $(E_i - jE_q)$ will alias into the signal band, thus damage the SNR of the modulator, and the image noise transfer function can be written as follows:

$$\frac{\alpha H}{1 + 2H + (1-\alpha^2)H^2}.$$

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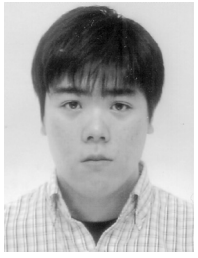

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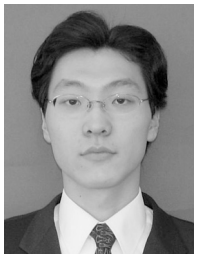

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