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High-Voltage MOS Device Modeling with BSIM3v3 SPICE Model

Takao MYONO[†a)], ***Member***, **Eiji NISHIBE**[†], **Shuichi KIKUCHI**[†], **Katsuhiko IWATSU**[†], **Takuya SUZUKI**[†], ***Nonmembers***, **Yoshisato SASAKI**[††], ***Member***, **Kazuo ITOH**[††], ***Nonmember***, ***and*** **Haruo KOBAYASHI**[††], ***Member***

SUMMARY This paper presents a new technique for modeling High-Voltage lightly-doped-drain MOS (HV MOS) devices accurately with the BSIM3v3 SPICE model. Standard SPICE models do not model the voltage dependency of R_s and R_d in HV MOS devices; this causes large discrepancies between the simulated and measured I-V characteristics of HV MOS devices. We propose to assign physical meanings and values different from the original BSIM3v3 model to three of its parameters to represent the voltage dependency of R_s and R_d. With this method, we have succeeded in highly accurate parameter extraction, and the simulated I-V characteristics of HV MOS devices using the extracted parameters match the measured results well. The relationship between the proposed modeling technique and the physical mechanism of HV MOS devices is also discussed based on measurement and device simulation results. Since our method does not change any model equations of BSIM3v3, it can be applied to any SPICE simulator on which the BSIM3v3 model runs, so we can use SPICE simulation for accurate circuit design of complex circuits using HV MOS devices.

key words: *high-voltage MOS, BSIM3, SPICE model*

1. Introduction

High-Voltage lightly-doped-drain MOS (HV MOS) devices are widely used, such as in LCD driver circuits, and recently complex analog circuitry using operational amplifiers has been implemented with HV MOS devices; hence the circuit design using HV MOS devices is very important [1]. However, at present, no standard SPICE model can model HV MOS devices precisely. For example, the BSIM3 version 3 (BSIM3v3) SPICE model [2]–[7] is widely accepted as one of the best models for submicron MOS devices. As shown in Fig. 1, the BSIM3v3 SPICE model simplifies the source resistance (R_s) and the drain resistance (R_d) to reduce the calculation load; it is assumed that R_s and R_d are constant or linear functions of the gate-source voltage (V_{gs}), and R_s and R_d are equal at all operating voltages; they are combined into R_{ds}. This is a simple-yet-accurate model for ordinary MOS devices for which the above assumptions are valid. However, for HV MOS devices, these assumptions are not valid and this method can not model HV MOS devices accurately; to increase the breakdown voltage, their R_s and R_d are made quite large and they are highly voltage dependent. Also in general their R_s and R_d are not equal. This is due to the fact that R_s and R_d are implemented with p^-region in source and drain of a p-channel HV MOS device, and especially p^-region in drain not only works as a drain resistance R_d but also causes *separation* between the channel and p^-region at a lower drain voltage V_{ds} than the velocity saturation voltage. (This channel separation is caused by the growth of the depletion region in the p^-region with increasing V_{ds}, which will be explained later.) This effect is very similar to pinch off of long channel MOS devices, but in HV MOS devices the channel separation causes drain current saturation even in triode region. This causes large discrepancies between the simulated and measured I-V characteristics of HV MOS devices. (The same argument is valid also for an n-channel HV MOS device.)

This paper proposes a novel technique to model HV MOS devices accurately with the BSIM3v3 SPICE model without any modification to its model equations; we assign physical meanings and values different from the original model to three of its parameters to represent the voltage dependency of R_s and R_d and the separation between the channel and p^-region. The parameter extraction method is described, and the measured and simulated I-V characteristics of HV MOS devices match well, which confirms the effectiveness of this method. The relationship between the proposed modeling technique and the physical mechanism of HV MOS devices is also discussed based on measurement

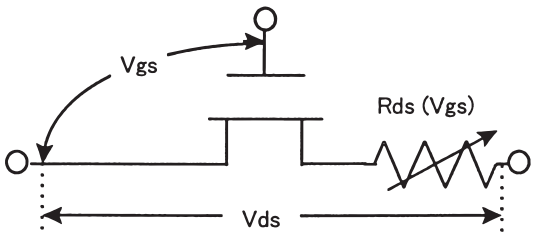

Fig. 1 Source and drain resistance model of original BSIM3v3. Source and drain resistances are combined into R_{ds} which is constant or a linear function of V_{gs}.

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[†]The authors are with MOS-LSI Division, SANYO Electric Co. Ltd., Gunma-ken, 370-0596 Japan.
[††]The authors are with Department of Electronic Engineering, Faculty of Engineering, Gunma University, Kiryushi, 376-8515 Japan.
a) E-mail: myon003877@swan.sanyo.co.jp

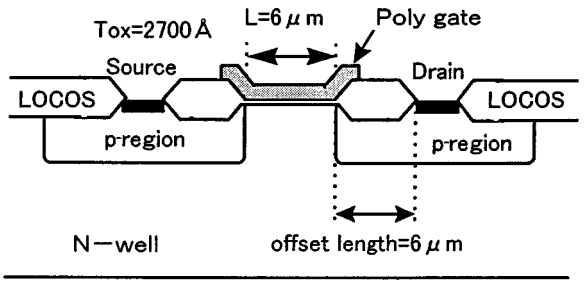

Fig. 2 Schematic structure of a p-channel HV MOS device. P^-region is provided in source and drain to increase the breakdown voltage. In some HV MOS devices, p^-region is provided only in drain.

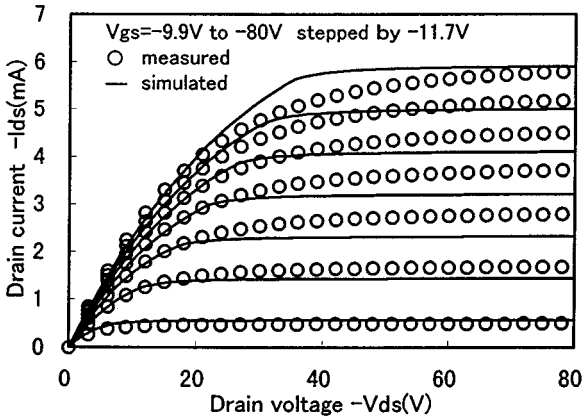

Fig. 3 Comparison between the measured and simulated I-V characteristics of a p-channel HV MOS device (original BSIM3v3). Large discrepancies are observed at high V_{ds} and V_{gs}.

and device simulation results. We note that our method does not change any model equations of BSIM3v3 and thus it can be applied to any SPICE simulator on which the BSIM3v3 model runs.

We close this section by remarking that recently some HV MOS device models are commercially available from CAD vendors, however, they require special parameter extraction tools and circuit simulators of the CAD vendors and the technical details of their HV MOS device models are not disclosed.

2. HV MOS Device Technology

Figure 2 shows the structure of the 80-V p-channel HV MOS device that we have developed, with gate-oxide film thickness (T_{ox}) of 2700 Å, channel length (L) of 6 μm and offset length of 6 μm. The explanation how this device structure realizes a high breakdown voltage is given as follows: large R_s and R_d are implemented with p^-region of low doping concentration in source and drain, respectively. In addition, when a high drain voltage V_{ds} is applied to the device, the depletion region grows in the p^-region, and hence the resistance value of the p^-region (i.e., the values of R_s and R_d) gets larger. Thus, the effective voltage across the channel does not increase significantly, and this is why the device structure in Fig. 2 realizes a high breakdown voltage and R_s and R_d are highly operating voltage dependent.

Figure 3 shows its I-V characteristics, and we see that the drain current in the saturation region (I_{dsat}) and the drain saturation voltage (V_{dsat}) increase at a decreasing rate as the gate voltage (V_{gs}) increases; the increase in I_{dsat} may be expressed as follows:

$$I_{dsat} \propto (V_{gs} - V_{th})^a, a < 1 \text{ for HV MOS devices,} \tag{1}$$

where V_{th} is the threshold voltage. (Note that $a = 2$ for ordinary long channel MOS devices and $a = 1$ for ordinary short channel MOS devices.) This is due to the increase in its source resistance (R_s) and drain resistance (R_d) (but mainly due to the increase in R_d). We see that the voltage dependency of R_s and R_d affects the I-V characteristics significantly.

3. HV MOS Device Modeling Accuracy with Original BSIM3v3

This section discusses the HV MOS device modeling accuracy using the original BSIM3v3 [2]–[7]. The BSIM3v3 represents R_s and R_d as a linear resistor R_{ds} as shown in Fig. 1 to reduce the calculation load while maintaining modeling accuracy. (On the other hand, in BSIM1 [8] and BSIM2 [9], which are earlier versions of submicron MOS SPICE models, R_s and R_d are not modeled explicitly but their effects are included implicitly in carrier mobility.) The BSIM3v3 gives the drain current equation in strong inversion region as follows:

$$I_{ds} = \frac{G_{ds0} V_{dseff}}{1 + G_{ds0} R_{ds}}, \tag{2}$$

where

$$G_{ds0} = \mu_{eff} \frac{\epsilon_{ox}}{T_{ox}} \frac{W}{L} \frac{V_{gs} - V_{th} - A_{bulk}(V_{dseff}/2)}{1 + V_{dseff}/(E_{sat} \cdot L)}, \tag{3}$$

$$E_{sat} = \frac{2 \cdot VSAT}{\mu_{eff}}, \tag{4}$$

μ_{eff} is the mobility, ϵ_{ox} is the permitivity of the silicon-oxide film, V_{th} is the threshold voltage, $VSAT$ is the saturation velocity, T_{ox} is the gate-oxide film thickness, W is the channel width, L is the channel length, V_{dseff} is the effective drain voltage parameter and A_{bulk} is the bulk charge parameter. For ordinary MOS devices, it can be assumed that the drain saturation effect is due to velocity saturation, and in case of the velocity saturation we obtain the following at the end of the drain:

$$I_{dsat} = W \cdot VSAT \frac{\epsilon_{ox}}{T_{ox}}(V_{gs} - V_{th} - A_{bulk} \cdot V_{dsat}), \quad (5)$$

where voltage drops across the source and drain resistances are neglected, I_{dsat} is the drain saturation current and V_{dsat} is the drain saturation voltage. Letting $I_{ds} = I_{dsat}$ and $V_{dseff} = V_{dsat}$ and also letting Eq. (2) = Eq. (5), we obtain the drain saturation voltage V_{dsat} as follows:

$$V_{dsat} \approx \frac{E_{sat}L(V_{gs} - V_{th})}{A_{bulk}E_{sat}L + (V_{gs} - V_{th})}, \quad (6)$$

where the effect of R_{ds} in our proposed model described later is neglected because we confirmed experimentally that the effect of R_{ds} on V_{dsat} is very small. Empirically a value of $\approx 1.0 \times 10^5$ (m/sec) $\pm 20\%$ is obtained for parameter $VSAT$ [10] when the parameter extraction is performed for ordinary MOS devices with the BSIM3v3 model. When $VSAT$ has such a value (i.e. the drain current saturation is caused by the velocity saturation), the increase rate of the saturation current I_{dsat} keeps almost constant even if V_{gs} increases. Furthermore, the equation of the source and drain resistance R_{ds} without back-gate-bias-voltage in BSIM3v3 (Fig. 1) is given by

$$R_{ds} = \frac{RDSW(1 + PRWG \cdot V_{gs})}{W}, \quad (7)$$

where $RDSW$ is source and drain resistance per unit channel width. Note that R_{ds} has a gate-voltage (V_{gs}) coefficient $PRWG$. BSIM3v3, which has this source and drain resistance model, works as an accurate model for ordinary submicron MOS devices where $R_s = R_d$, and the extracted parameter value of R_{ds} yields to approximately $R_s + R_d$; thus its measured and simulated I-V characteristics match well.

On the other hand, Fig. 3 shows a comparison of the measured and simulated I-V characteristics of a p-channel HV MOS device; we have extracted its parameters by the standard method (using an UT-MOST parameter extraction tool [11]) with the original BSIM3v3. It is observed that both match fairly well for *low* V_{gs} and V_{ds} operating voltages while there are large discrepancies between them for *high* V_{gs} and V_{ds} operating voltages. This is because the simulation does not express the inherent phenomenon of the HV MOS device that the increase rate of I_{dsat} decreases as the gate voltage (V_{gs}) increases.

Note that the features of the extracted BSIM3v3 parameter values of the HV MOS device are as follows:

1. The velocity saturation parameter $VSAT$ value is 1.94×10^4 (m/sec). This is due to the fact that the parameter extraction tool optimizes the value of $VSAT$ according to the inherent phenomenon of the HV MOS device that the increase rate of I_{dsat} decreases with the nonlinear voltage drops across R_d and R_s.
2. The parameter $RDSW$ value of source and drain resistance per unit channel width is 1.75×10^5 (Ω-μm). When we decreased the operation voltage ranges of V_{gs} and V_{ds} to a smaller voltage (10 V) and reextracted the value of $RDSW$, we obtained the same value. This means that $RDSW$ represents the source and drain resistance component which is almost independent of V_{gs} and V_{ds}.
3. The value of the parameter $PRWG$, the gate-voltage coefficient for R_{ds}, is 1×10^{-5} (V^{-1}); this is sufficiently small and R_{ds} can be considered as an almost constant resistance.

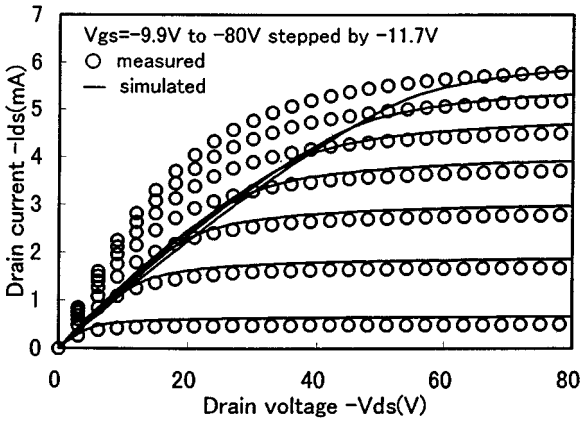

Fig. 4 Comparison between the measured and simulated I-V characteristics of a p-channel HV MOS device with an optimized parameter $PRWG$ value of 1.6E-2 in the original BSIM3v3.

We have investigated the effectiveness of the gate-voltage dependent model of R_{ds} in Eq. (7) for HV MOS devices; the parameter extraction system optimized only the value of $PRWG$ by setting $VSAT = 1 \times 10^5$ and with the other parameter values the same as the previously extracted ones. We obtained a parameter $PRWG$ value of 1.6×10^{-2} and performed the SPICE simulation with this value; Fig. 4 shows the measured and simulated I-V characteristics, and large discrepancies are observed in triode region. We see that the gate-voltage dependent model of R_{ds} given by Eq. (7) can not express precisely the inherent phenomenon of the HV MOS device that the increase rates of V_{dsat} and I_{dsat} decrease with the nonlinear voltage drops across R_d and R_s.

Since BSIM3v3 is a *physical* SPICE model (whose equations and parameters have physical meanings), its parameter extraction system sets the initial values and ranges of the parameters according to the physical phenomena of the MOS device to be measured. The system performs the extraction for each parameter automatically according to its initial-setting value and within the operating voltage range where the corresponding physical phenomenon occurs; e.g., since the drain current saturation is due to the velocity saturation in ordinary MOS devices, the parameter extraction tool optimizes the value of $VSAT$ to express this phenomenon,

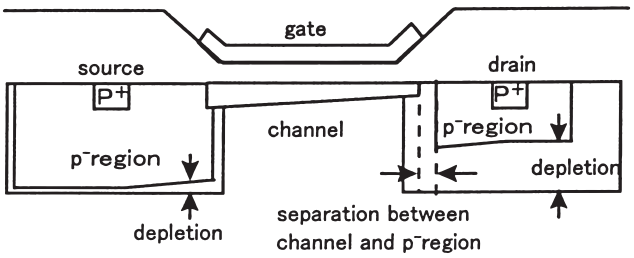

Fig. 5 Cross-section of a p-channel HV MOS device which explains its physical phenomena (the depletion region growth and the channel separation in drain).

and does not use other parameters for numerical fitting. Hence clarifying the physical mechanism in p^-region is very important in order to model the HV MOS device accurately with BSIM3v3.

4. HV MOS Device Mechanism Analysis with Device Simulations

This section discusses the physical mechanism of the HV MOS device focusing on p^-region and based on device simulations. We have conducted device simulations for the HV MOS devices and obtained the following results:

1. As the drain voltage (V_{ds}) increases, the depletion region in p^-region grows as shown in Fig. 5 and the separation between the channel of the drain-side and p^-region appears after V_{ds} reaches a certain value. (Hereafter we will call this effect "channel separation.")
2. As the gate voltage (V_{gs}) increases, the growth of the depletion region in p^-region slows.

According to the above device simulation results and the measured I-V characteristics in Fig. 3, we conjecture as follows:

1. The drain voltage (V_{ds}) which causes channel separation is smaller than the saturation voltage (V_{dsat}) in Eq. (6).
2. When the channel separation appears, the drain-side channel voltage level does not change even if V_{ds} increases.

These effects are very similar to *pinch off* of long channel MOSFET model in a sense that in HV MOS devices the effective drain-source voltage across the channel is clamped at the voltage at which the channel separation appears and which becomes larger as the gate-voltage V_{gs} increases. However note that in HV MOS devices the channel separation appears even in triode region, which differs from the pinch-off effect, and hence as V_{gs} increases, the increase rate of V_{dsat} decreases. We see that expressing these phenomena in BSIM3v3 equations would lead to an accurate modeling of HV MOS devices.

5. Proposed HV MOS Device Modeling Technique

Based on the above-mentioned HV MOS device mechanism analysis, this section proposes a novel HV MOS device modeling technique by changing the physical interpretations of BSIM3v3 model but without changing its equations.

In the original BSIM3v3, the V_{dseff} function follows V_{ds} in triode region while it approaches to V_{dsat} in saturation region (i.e., it is clamped to V_{dsat} there) [6] and then V_{dseff} improves the continuities of the I-V characteristics between triode and saturation regions. Equation (6) shows that V_{dsat} is determined by $VSAT$ and V_{gs} for a fixed channel length L and is almost independent of A_{bulk}. Also recall that $VSAT$ can not express the channel separation effect as shown in Fig. 3. In addition to these facts, we would like to consider the following:

1. Since the drain voltage V_{ds} at which the channel separation appears is much smaller than the velocity saturation voltage, the velocity saturation effect can be ignored in the HV MOS device model.
2. The extracted parameter value of A_{bulk} is always nearly equal to 1.0 and hence the bulk charge effect is small enough to be ignored compared to the other physical effects. Thus the parameter A_{bulk} can be used to represent another physical phenomenon.
3. The drain voltage V_{ds} at which the channel separation appears can be controlled within a wide range if it is expressed by V_{dsat} in Eq. (6) and controlled mathematically by A_{bulk}.

Our first idea is to express the effective drain voltage clamped by the channel separation using V_{dseff} and to control the clamp voltage V_{dsat} of V_{dseff} by A_{bulk}. Note that A_{bulk} of Eq. (8) has the gate-voltage-coefficient AGS, and then the clamp voltage V_{dsat} can appropriately vary with V_{gs} by optimizing AGS. If the velocity saturation is ignored, the gate-voltage-dependency of V_{dsat} can be further effectively expressed. Focusing on AGS and V_{gs} and considering other parameters as constants α and β, A_{bulk} is given by

$$A_{bulk} = 1 + \frac{K_1}{2\sqrt{\phi_s - V_{bs}}} \frac{A_0 L}{L + 2\sqrt{X_j X_{dep}}}$$

$$\times \left[1 - AGS \cdot (V_{gs} - V_{th}) \cdot \left(\frac{L}{L + 2\sqrt{L + X_j X_{dep}}} \right)^2 \right]$$

$$= 1 + \alpha [1 - AGS \cdot (V_{gs} - V_{th}) \beta]$$

$$\equiv f_1(AGS, V_{gs}), \tag{8}$$

where ϕ_s is the surface potential, X_j is the junction

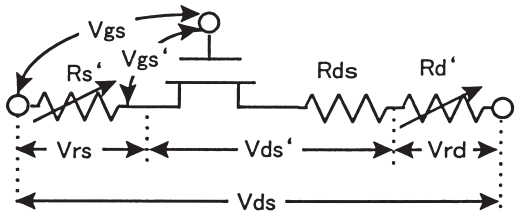

Fig. 6 Source and drain resistance model of modified BSIM3v3. R_{ds} is an operating-voltage-*independent* component while R'_s and R'_d are operating-voltage-*dependent* components.

depth, X_{dep} is the depletion width in the substrate, K_1 is the first-order body effect coefficient, A_0 is the bulk charge effect coefficient for channel length and V_{bs} is the substrate bias voltage. Then the velocity saturation voltage V_{dsat} is only a function of AGS and V_{gs} if the velocity saturation effect is ignored:

$$V_{dsat} \approx \frac{V_{gs} - V_{th}}{A_{bulk}} \equiv f_2(AGS, V_{gs}). \tag{9}$$

Then V_{dseff}, which is a function of $VSAT$, $DELTA$, V_{gs} and V_{ds} in the original BSIM3v3, yields to a function of AGS, $DELTA$, V_{gs} and V_{ds}, and hence it is a V_{gs}-dependent function controlled by AGS within a wide range:

$$\begin{aligned} V_{dseff} &= V_{dsat} - \frac{1}{2}(V_{dsat} - V_{ds} - DELTA \\ &+ \sqrt{(V_{dsat} - V_{ds} - DELTA)^2 + 4 \cdot DELTA \cdot V_{dsat}}) \\ &\equiv f_3(AGS, DELTA, V_{ds}, V_{gs}), \end{aligned} \tag{10}$$

where $DELTA$ is a tendency coefficient of V_{dseff}. In our new interpretation, A_{bulk} is not a bulk charge parameter any more but a channel separation effect parameter, and AGS is its gate-voltage coefficient.

Next, we will try to model the source and drain resistances of HV MOS devices, which are implemented as p^- region, and we propose an HV MOS device model as shown in Fig. 6. We consider that R_s and R_d are given as follows:

$$R_s = R_{s0} + R'_s, \qquad R_d = R_{d0} + R'_d,$$

where R'_s and R'_d depend on V_{gs} and V_{ds} while R_{s0} and R_{d0} are constant terms which are combined into R_{ds}. The physical meanings of R_{s0}, R'_s, R_{d0} and R'_d are given as follows: R_{s0} and R_{d0} are the source and drain resistances in the p^- regions respectively when no drain current flows and hence the depletion regions do not grow, and R_{s0} and R_{d0} are combined into R_{ds}. On the other hand, when the drain current flows due to V_{gs} and V_{ds}, it causes voltage drops across p^-regions in source and drain in Fig. 5. Due to these voltage drops and the substrate bias voltage, the depletion regions grow in the p^- regions, which effectively reduces the volumes of the p^- regions. Hence the resistances of the p^- regions in source and drain increase, and let their increased resistance values in source and drain be R'_s and R'_d respectively. In other words, the values of R'_s and R'_d depend on V_{gs} and V_{ds}.

Now let us consider how to express this model with BSIM3v3. When V'_{gs} and V'_{ds} are the effective gate-source and drain-source voltages across the pure MOSFET component plus R_{ds} (which can be modeled by the original BSIM3v3, see Fig. 1), respectively, and V_{rs} and V_{rd} are voltage drops due to R'_s and R'_d respectively, we obtain the following:

$$V'_{gs} = V_{gs} - V_{rs}, \tag{11}$$

$$V'_{ds} = V_{ds} - (V_{rs} + V_{rd}). \tag{12}$$

Now let us consider how to express the HV MOS device model in Fig. 6 by assigning different meanings from the original BSIM3v3 to the parameters of V_{dseff} and A_{bulk} and ignoring the velocity saturation effect. First we define V'_{ds} using the parameter V_{dseff}:

$$V'_{ds} = V_{dseff}, \tag{13}$$

so that the parameter V_{dseff} expresses the channel separation effect as well as the effect of R'_s and R'_d. Next we express the physical phenomena of p^-region in source using A_{bulk} and V_{dseff}, and when the velocity saturation effect is ignored, G_{ds0} is given by

$$\begin{aligned} G_{ds0} &= \mu_{eff} \frac{\epsilon_{ox}}{T_{ox}} \frac{W}{L} \\ &\times \left[V_{gs} - V_{th} - \frac{V_{dseff}}{2} - (A_{bulk} - 1)\frac{V_{dseff}}{2} \right]. \end{aligned}$$

Then we define V_{rs} as follows:

$$V_{rs} = (A_{bulk} - 1)\frac{V_{dseff}}{2}. \tag{14}$$

It follows from Eqs. (11) and (14) that

$$V'_{gs} = V_{gs} - (A_{bulk} - 1)\frac{V_{dseff}}{2}. \tag{15}$$

Thus we obtain the drain current equation from Eqs. (11) – (15) as follows:

$$I_{ds} = \frac{G_{ds0} V'_{ds}}{1 + R_{ds} G_{ds0}},$$

where

$$G_{ds0} = \mu_{eff} \frac{\epsilon_{ox}}{T_{ox}} \frac{W}{L} \left(V'_{gs} - V_{th} - \frac{V'_{ds}}{2} \right).$$

In the above-proposed equations, V_{rs} is controlled by A_{bulk}, and hence A_{bulk} represents the channel separation and source resistance, and AGS is its gate-voltage coefficient. Furthermore, $V_{rs} + V_{rd}$ is controlled by $DELTA$, which is a coefficient of V_{dseff} and thus A_{bulk} and $DELTA$ are optimized not independently but they are optimized to well-balanced values.

Table 1 Extracted parameters of original and modified BSIM3v3 models.

Extracted parameters	VSAT	AGS	DELTA
Original BSIM3v3	1.94×10^4	1×10^{-5}	0.01
Modified BSIM3v3	1×10^9	-0.0984	0.991

6. Parameter Extraction Technique

This section describes how to extract parameter values from HV MOS devices with the above-mentioned proposed BSIM3v3 model. The proposed method uses parameters A_{bulk} and V_{dseff} to represent V_{rs} and V_{rd} respectively and also ignores the velocity saturation effect, and hence the parameter values of A_{bulk} and V_{dseff} have to be extracted to optimize V_{rs} and V_{rd} respectively and the value of $VSAT$ has to be sufficiently large. We have found that the standard parameter extraction method (e.g., with an UTMOST parameter extraction tool [11]) can be directly applied just with the following initial-parameter-value-settings and operating-voltage-ranges so that the parameter values of AGS and $DELTA$ based on Eqs. (14), (15) and (13) can be extracted and the velocity saturation effect can be ignored:

1. Set $VSAT$ to a large value (e.g., 1×10^9) to ignore the velocity saturation effect.
2. Set the initial value of AGS to -0.1 to optimize the parameter value of AGS in saturation region as well as in triode region close to saturation region. This means optimizing the clamp voltage V_{dsat} of V_{dseff} in Eq. (10) and V'_{gs} in Eq. (11).
3. Set the initial value of $DELTA$ to 1.0 to optimize the parameter value of $DELTA$ around the drain saturation voltage. This means optimizing the $V_{rs}+V_{rd}$ component of V_{dseff} in Eqs. (12) and (13).

Here AGS is the gate bias coefficient for A_{bulk} and $DELTA$ is the coefficient for V_{dseff} in BSIM3v3. Note that the value of AGS is usually extracted as a positive value with the original BSIM3v3 by setting its initial-value to zero, while it is negative in our proposed method because its physical interpretation is different. According to the above procedure, we have obtained the parameter values of $VSAT$, AGS and $DELTA$ for a p-channel MOS device as shown in the column "modified BSIM3v3" of Table 1, and the other parameter values are the same as those extracted using the original BSIM3v3. SPICE simulation of the HV MOS device was performed using these parameters, and Fig. 7 shows a comparison of the simulated and measured I-V characteristics of a p-channel HV MOS device while Fig. 8 shows those of an n-channel HV MOS device. We see that the simulated and measured I-V characteristics match well at almost all operating voltages in both p-channel and n-channel HV MOS devices, which confirms the effectiveness of our technique.

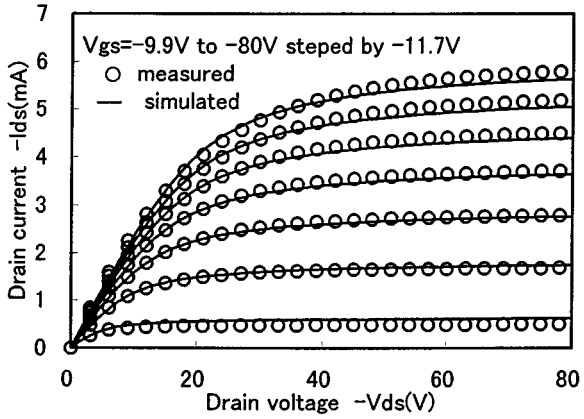

Fig. 7 Comparison between the measured and simulated I-V characteristics of a *p-channel* HV MOS device (modified BSIM3v3).

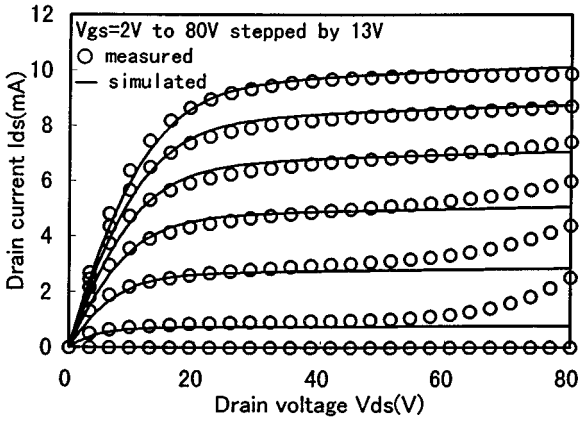

Fig. 8 Comparison between the measured and simulated I-V characteristics of an *n-channel* HV MOS device (modified BSIM3v3).

Remark: Figure 8 shows some discrepancies between the measured and simulated I-V characteristics of an n-channel HV MOS device in high V_{ds} and low V_{gs} operating region, which is due to the substrate current induced body effect (SCBE) [12], [13]. It is well-known that SCBE has a peak as a function of V_{gs}, and it is estimated that the SCBE of the measured device in Fig. 8 has relatively strong dependency on V_{gs} and has a peak at $V_{gs} \approx 15$ V. However the BSIM3v3 SPICE model does not incorporate the V_{gs}-dependency for SCBE [5], and this is the reason for the discrepancies in Fig. 8.

7. Verification of Relationship between Modified BSIM3v3 and Physical Mechanism for HV MOS Device

In this section we will try to verify our interpretation on the physical mechanism of a p-channel HV MOS de-

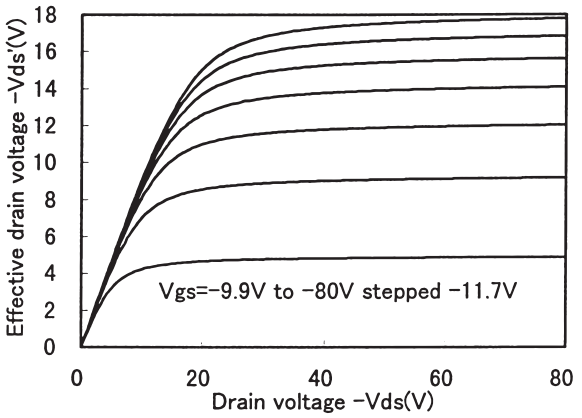

Fig. 9 Drain-source voltage V_{ds} across a p-channel HV MOS device vs. its effective drain-source voltage V'_{ds} across the channel. V'_{ds} is calculated based on the source and drain resistance model in Fig. 5.

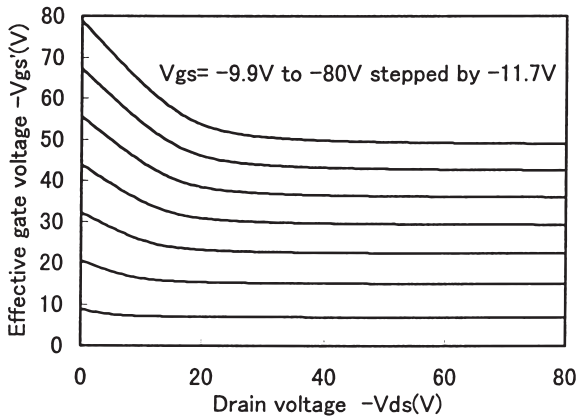

Fig. 10 Drain-source voltage V_{ds} across a p-channel HV MOS device vs. its effective gate-source voltage V'_{gs}. V'_{gs} is calculated based on the source and drain resistance model in Fig. 5.

vice using three parameters in BSIM3v3 because our interpretation on the modified BSIM3v3 is based on the physical mechanism of HV MOS devices. Figure 9 shows V_{ds} (the drain-source voltage across the HV MOS device) versus V'_{ds} (the effective drain-source voltage across the pure channel), calculated from the optimized parameter values of AGS and $DELTA$, and we see that V'_{ds} is clamped to a substantially smaller voltage than V_{ds}; this is the reason that the HV MOS device has a high breakdown voltage. Furthermore, Fig. 10 shows V_{ds} versus V'_{gs} (the effective gate-source voltage across the pure MOS component). The value of V'_{gs} is determined by the voltage drop V_{rs} due to the drain current across R_s. Recall that V'_{ds} and V'_{gs} are optimized by A_{bulk} (whose value varies from 1.4 to 4.2 due to the gate-voltage), and as the value of A_{bulk} increases, V_{dsat} (equivalent to the channel separation voltage) becomes smaller while R'_s becomes larger; the optimized value of A_{bulk} is a trade-off between V_{dsat} and R'_s. We see that our modified BSIM3v3 model can explain the physical mechanism of HV MOS devices very well.

8. Conclusion

We have described a new technique to model HV MOS devices accurately with the BSIM3v3 SPICE model. None of the standard SPICE models can model the voltage dependency of R_s and R_d of HV MOS devices, but we have assigned physical meanings and values different from the original BSIM3v3 model to three of its parameters to represent the voltage dependency of R_s and R_d. We have succeeded in highly accurate parameter extraction, and the simulated I-V characteristics of HV MOS devices using the extracted parameters matched well to the measured results. The relationship between the proposed modeling technique and the physical mechanism of HV MOS devices has been also discussed based on measured and device simulation results. Since our method does not change any model equations of BSIM3v3, it can be applied to any SPICE simulator on which the BSIM3v3 model runs. Our results here will enable accurate design for complex circuits, such as operational amplifiers, with HV MOS devices based on SPICE simulation.

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Takao Myono graduated from Kumagaya technical high school in 1964. In 1964 he joined Sanyo Electric Corporation, Semiconductor Division, Gunma, Japan. From 1965 to 1967 he studied at Ibaraki University. From 1967 to 1976 he was engaged in the design of PMOS and CMOS logic LSIs, and from 1976 to 1995 he was involved in the development of CAD systems. He is currently a Department Manager in memory LSIs. His current interests are analog circuits and device modeling.

Eiji Nishibe received the B.S. and M.S. degrees in material engineering from Science University of Tokyo in 1993 and 1995,respectively. In 1995, he joined Sanyo Electric Corporation, Semiconductor Division, Gunma, Japan. He has been working on the development of high voltage devices for LCD drivers.

Shuichi Kikuchi received B.S. degree in applied material science from Muroran Institute of Technology, Muroran, Japan in 1983. In 1983, he joined Sanyo Corporation, Semiconductor Division, Gunma, Japan. From 1983 to 1988 he worked on the design and product engineering of micro-controllers. Since 1988, he has been working on the development of HV MOS device technology.

Katsuhiko Iwatsu received the M.S. degree in physical chemistry from Tokyo Institute of Technology in 1996. In 1996 he joined Sanyo Electric Corporation, Semiconductor Division, Gunma, Japan. He has been working on the development of product engineering for logic LSIs.

Takuya Suzuki received the B.S. and M.S. degrees in Electrical Engineering from Gunma University, Gunma, Japan in 1979 and 1981,respectively. In 1981, he joined Sanyo Electric Corporation, Semiconductor Division, Gunma, Japan. He is currently a Department Manager in device technology.

Yoshisato Sasaki received the B.E., M.E., and D.E. degrees in electrical communication from Tohoku University, Sendai, Japan, in 1962, 1964 and 1968, respectively. He is currently a Professor of the Department of Electronic Engineering at Gunma University. His general research interests include physics and technology of silicon processing. He is a member of the Japan Society of Applied Physics, the Physical Society of Japan.

Kazuo Itoh received the B.E. and M.E. degrees in Electronic Engineering from Gunma University in 1974 and 1976, respectively, and the Dr. Sci. degree from the University of Tokyo in 1989. He joined the Faculty of Technology, Gunma University in 1976 as a Research Associate and is currently an Associate Professor (1991–) in the Department of Electronic Engineering. His research interests include semiconductor nano fabrication and its quantum transport.

Haruo Kobayashi received the B.S. and M.S. degrees in information physics and mathematical engineering from University of Tokyo in 1980 and 1982 respectively, the M.S. degree in electrical engineering from UCLA in 1989, and the Dr.Eng. degree in electrical engineering from Waseda University in 1995. He joined Yokogawa Electric Corp. Tokyo, Japan in 1982, where he was engaged in the research and development related to measuring instruments and mini-supercomputers. In 1997 he joined Gunma University and presently is an Associate Professor there. He was also an adjunct lecturer at Waseda University from 1994 to 1997. His research interests include analog & digital integrated circuits design and signal processing algorithms. He is a recipient of the 1994 Best Paper Award from the Japanese Neural Network Society.