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Modeling and Parameter Extraction Technique for Uni-Directional HV MOS Devices

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SUMMARY This paper presents a new technique for accurately modeling uni-directional High-Voltage lightly-doped-drain MOS (HV MOS) devices by extending the bi-directional HV MOS model and adopting a new parameter extraction method. We have already reported on a SPICE model for bi-directional HV MOS devices based on BSIM3v3. However, if we apply this bi-directional HV MOS model and its parameter extraction technique directly to uni-directional HV MOS devices, there are large discrepancies between the measured and simulated *I*-*V* characteristics of the uni-directional devices. This paper extends the bi-directional HV MOS model, and adopts a new parameter extraction technique. Using parameters extracted with the new method, the simulated *I*-*V* characteristics of the uni-directional *n*-channel HV MOS device match the measured results well. Since our method does not change any model equations of BSIM3v3, it can be applied to any SPICE simulator on which the BSIM3v3 model runs.
key words: *high-voltage MOS, BSIM3, SPICE model*

1. Introduction

We have developed several kinds of HV MOS devices whose device structures and doping levels in the offset regions differ depending on the specifications of the devices. We have developed representative 80 V and 45 V HV MOS devices. The 80 V HV MOS device is bi-directional (e.g., it can be used as a bi-directional MOS switch) with both drain and source offset regions, and we previously described its SPICE model [4]–[6] based on BSIM3v3 [1]–[3]. On the other hand, the 45 V HV MOS device is uni-directional, and has only a drain offset region. That is, it does not have a source offset region with corresponding source resistance. However, our previously-proposed bi-directional HV MOS model inherently includes source offset region resistance, and we cannot eliminate it from the model equations. Hence, if we apply the bi-directional HV MOS model and its parameter extraction technique directly to the uni-directional HV MOS device, we have to compensate for part of the drain current caused by the source resistor model. However, this compensation makes it difficult to represent the transconductance reduction (g_m-reduction) in saturation region with increasing gate-source voltage (V_{gs}) which is inherent to bi-directional and uni-directional HV MOS devices [4], [5]; as a result, with this model there are large discrepancies between the measured and simulated I_{ds}-V_{ds} characteristics of uni-directional HV MOS devices.

In this paper, we have used the same technique to model uni-directional HV MOS devices as previously reported for bi-directional HV MOS devices [4]–[6] while adopting a new parameter extraction technique. To compensate for part of the drain current caused by the source resistor model, we utilize the dependence of bulk charge parameter (A_{bulk}) on V_{gs}; and to model the g_m-reduction, we utilize the dependence of the source and drain resistor parameters (R_{ds}) on V_{gs}. As a result, voltage dependencies of both the parameters are derived as large values, and we use these two values in a manner different from their primary purposes in BSIM3v3. With the new uni-directional HV MOS modeling technique, the simulated *I*-*V* characteristics of the uni-directional *n*-channel HV MOS device match the measured characteristics well, which confirms its effectiveness.

2. Uni-Directional HV MOS Device Technology

Figure 1 shows the structure of our 45 V *n*-channel HV MOS device, with a gate-oxide film thickness (T_{ox}) of 1350Å, channel length (L) of 3.2 μm and offset of 3.2 μm. An n^-offset region of low doping concentration is used in the drain region, in order to realize high uni-directional drain-source breakdown voltage. Based on our device simulations, we consider that the basic operation of the bi-directional HV MOS device is as explained below [5], and this is also valid for the uni-directional HV MOS device. When drain-source voltage (V_{ds}) is applied to the HV MOS device, a depletion region grows in the n^-offset region and separates the channel from the n^-offset region. The effect of the electric field from the gate electrode on the depletion region causes the drain-side channel terminal voltage to saturate at a low voltage. This reduces the voltage across the channel, and hence increases the breakdown voltage between the drain and source. Moreover, as the drain-

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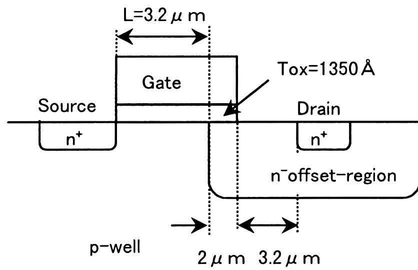

Fig. 1 Schematic structure of the uni-directional n-channel HV MOS device.

side channel terminal voltage saturates in the triode region, g_m is reduced.

For the sub-micron devices, g_m-reduction in triode region is caused by source resistance R_s rather than drain resistance R_d. On the other hand for HV MOS devices, g_m-reduction is mainly due to drain resistance: HV MOS devices have an offset region in drain (and also in source for bi-directional HV MOS devices), and the depletion region inside the offset region grows due to the voltage drop in the offset region and the potential difference between the offset region and the substrate (Fig. 3 in [5]). Note that growth of the depletion region increases resistance of the offset region, and since the drain side has larger potential difference between the offset region and the substrate, the depletion region in the offset region of the drain side spreads more widely. Hence when V_{ds} is applied to the bi-directional HV MOS, R_d becomes much larger than R_s, and g_m-reduction of HV MOS is mostly caused by the offset region of the drain, so that bi-directional and uni-directional HV MOS devices have almost the same level of g_m-reduction.

3. Application of Bi-Directional HV MOS Model to Uni-Directional HV MOS Device

In this section, we directly apply the bi-directional HV MOS model and its parameter extraction technique to the uni-directional HV MOS device, and investigate the results. The bi-directional HV MOS model parameter extraction technique is outlined below [4]–[6]:

1) First, extract all BSIM3v3 parameters by the standard method.
2) Then set the value of $VSAT$ to a large value (e.g., 1×10^9 m/sec) assuming a long-channel device.
3) Optimize AGS and $DELTA$ at the same time. This is to optimize the saturation voltage of the drain-side channel terminal V_{dsat} and the source resistance due to the offset region.
4) Our recent studies show that the modeling accuracy of drain conductances (g_{ds}) can be improved by optimizing $PDIBLC1$ (first output resistance $DIBL$ (Drain-Induced Barrier Lowering) effect correction parameter) and $PDIBUC2$ (second output resistance $DIBL$ effect correction parameter).

Table 1 Extracted BSIM3v3 parameter values for each step.

	AGS	U0	UA	RDSW	PRWG
Step I	0.084	616	0.7×10^{-8}	3.8×10^{3}	0.0
Step II	-0.036	616	0.7×10^{-8}	3.8×10^{3}	0.0
Step III	-0.049	520	0.4×10^{-8}	3.8×10^{3}	0.0
Step IV	-0.076	463	0.0	1.9×10^{3}	0.092
Step V	-0.077	588	0.0	5.5×10^{3}	0.018

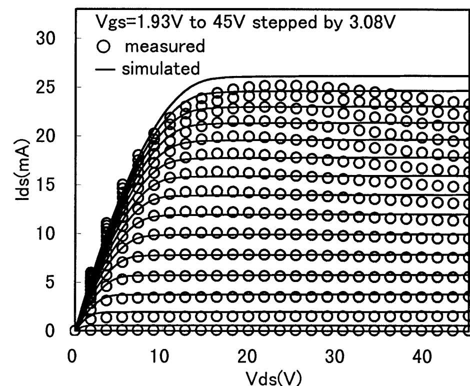

Fig. 2 Comparison between measured and simulated (with the bi-directional HV MOS model) I-V characteristics of the 45 V HV MOS device.

Using the above procedure for the bi-directional HV MOS device, the parameter AGS optimizes V_{dsat} and source resistance in a well-balanced manner, and the measured and simulated I-V characteristics match well. Furthermore, this method can precisely reproduce the g_m-reduction phenomenon, which is inherent to HV MOS devices.

On the other hand, step II in Table 1 shows the parameters obtained by directly applying the bi-directional HV MOS device model and parameter extraction technique to the uni-directional HV MOS device, and Fig. 2 shows a comparison of the measured and simulated I-V characteristics. Figure 3 shows a comparison of the measured and simulated results for g_m. In Fig. 2 large discrepancies are observed between the measured and simulated I-V characteristics, and Fig. 3 shows that AGS cannot represent the g_m reduction.

4. Negative Drain Conductance

Some HV MOS devices (such as the 45 V HV MOS device) have the operating region where their drain conductances (g_{ds}) are negative as shown in Fig. 4. The negative g_{ds} does not appear (or very small if it appears) for HV MOS devices where the gate terminal is provided on the LOCOS to reduce the electric field from the gate to the offset region (Fig. 2 in [5]). On the other hand an apparently negative g_{ds} is observed for a type of HV MOS device with a flat gate terminal (Fig. 1).

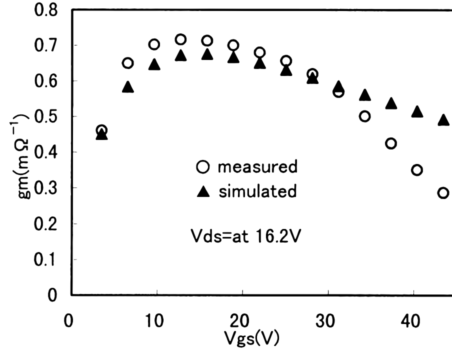

Fig. 3 Comparison between measured and simulated (with the bi-directional HV MOS model) g_m characteristics of the 45 V HV MOS device.

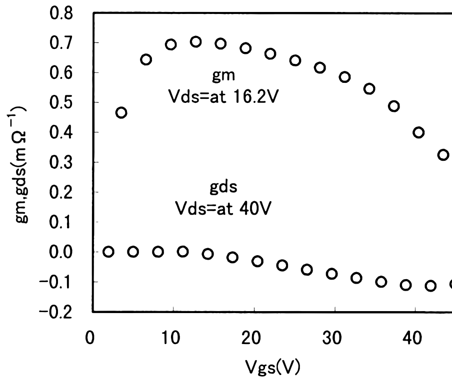

Fig. 4 Measured g_m and g_{ds} characteristics of the 45 V HV MOS device.

We consider that this phenomenon of negative g_{ds} depends upon the doping density in the offset region and the device structure. We have found, by Figs. 3 and 4, that the V_{gs} region where g_{ds} is negative corresponds to that when g_m reduces with increasing V_{gs}. As described in [5], when g_m reduces with increasing V_{gs}, the channel is in triode region, and I_{ds} changes by fairly amount even with a small change of V_{ds}. On the other hand, when g_m increases with increasing V_{gs}, I_{ds} is almost constant for a small change of V_{ds}. Thus we deduce that the negative g_{ds} is caused by the channel terminal voltage on the drain side, which is as the same as in the case of g_m reduction: the channel terminal voltage on the drain side slightly decreases after the saturation as increasing V_{ds}. The detailed analysis of its physical mechanism is left for a future work.

5. Limitation of Applying Bi-Directional HV MOS Model to Uni-Directional HV MOS Device

In order to examine limitations of applying the bi-directional HV MOS modeling technique to the uni-directional HV MOS device, we optimize AGS, mobility $U0$ and first-order mobility degradation coefficient UA at the same time. Step III in Table 1 shows the parameters obtained according to the above optimization. The simulated I-V characteristics using these parameters are hardly improved compared to the simulation result of Step II. It is clear that effective mobility μ_{eff} cannot represent the g_m-reduction and cannot supplement the function of AGS.

6. Proposed Uni-Directional HV MOS Device Modeling Technique

In this section we propose a uni-directional HV MOS modeling technique: we use the bi-directional HV MOS model in [4]–[6] as a basis, and the main equations are as follows:

$$G_{ds0}=\mu_{eff}\frac{\varepsilon_{ox}}{T_{ox}}\frac{W}{L}\left(V_{gs}-V_{rs}-V_{th}-\frac{V'_{ds}}{2}\right), \qquad (1)$$

$$V_{rs}=(A_{bulk}-1)\frac{V'_{ds}}{2}, \qquad (2)$$

$$I_{ds}=\frac{G_{ds0}V'_{ds}}{1+G_{ds0}R_{ds}}, \qquad (3)$$

$$A_{bulk}\equiv f_1(AGS,V_{gs}), \qquad (4)$$

$$V_{dsat}\approx\frac{V_{gs}-V_{th}}{A_{bulk}}\equiv f_2(AGS,V_{gs}), \qquad (5)$$

$$V'_{ds}=V_{dseff}\equiv f_3(AGS,DELTA,V_{ds},V_{gs}). \qquad (6)$$

Here, W is the channel width, μ_{eff} is the effective mobility, ε_{ox} is the permitivity of the silicon-oxide film, V_{th} is the threshold voltage, AGS is the gate bias coefficient of the A_{bulk}, V_{dsat} is the saturation value of the drain-side channel terminal, V_{dseff} is the effective drain-source voltage and $DELTA$ is the effective drain voltage smoothing parameter of V_{dseff}. Where, V'_{ds} is the drain-side channel terminal voltage, which is equivalent to the V_{dseff} of BSIM3v3.

V_{rs} is voltage drop across the source resistance in the offset region. It cannot be eliminated from Eq. (1) as V_{rs} is inherent for the bi-directional HV MOS model with BSIM3v3. Hence, it is necessary to compensate for part of the drain current component by V_{rs} in Eq. (1) for the uni-directional HV MOS model. Here, we define the drain current I_{dsr0} in which the voltage V_{rs} in Eq. (1) is eliminated as shown below. I_{dsr0} is a model equation for the uni-directional HV MOS device model.

$$G_{dsr0}=\mu_{eff}\frac{\varepsilon_{ox}}{T_{ox}}\frac{W}{L}\left(V_{gs}-V_{th}-\frac{V'_{ds}}{2}\right), \qquad (7)$$

$$I_{dsr0}=\frac{G_{dsr0}V'_{ds}}{1+G_{dsr0}R_{ds}}. \qquad (8)$$

Further, by defining I_{vrs} as the variable component of

drain current due to V_{rs}, we obtain the following expression:

$$I_{ds} = I_{dsr0} - I_{vrs}. \tag{9}$$

The above expression indicates that the way to compensate for I_{vrs} in the uni-directional HV MOS model is to optimize I_{dsr0} by making it larger than I_{ds} by the value of I_{vrs}. Here it can be assumed that the value of I_{ds} is equivalent to the measured data. Suppose the parameter AGS is set to a large negative value, the value of A_{bulk} in Eq. (4) increases, which in turn decreases the value of V_{dsat} in Eq. (5) and results in decreasing the value of I_{dsr0}. At the same time, A_{bulk} increases the value of I_{vrs} larger. So, AGS cannot optimize V_{dsat} correctly, and I_{ds} cannot represent the g_m-reduction (refer to Sect. 7). In addition, the value of I_{vrs} cannot be obtained directly by calculation; instead use the following equation:

$$I_{vrs} = I_{dsr0} - I_{ds}. \tag{10}$$

Here, we define G'_{ds0} in which μ_{eff} is eliminated from G_{ds0} in Eq. (1), as follows:

$$G'_{ds0} = \frac{\varepsilon_{ox}}{T_{ox}} \frac{W}{L} \left(V_{gs} - V_{th} - A_{bulk} \frac{V'_{ds}}{2} \right). \tag{11}$$

We can represent the drain current in Eq. (3) as follows:

$$I_{ds} = \frac{G'_{ds0} V'_{ds}}{1/\mu_{eff} + G'_{ds0} R_{ds}}. \tag{12}$$

The equation shows that μ_{eff} can attenuate the drain current but cannot cause g_m-reduction. We can understand this clearly by the I-V characteristics simulation of ordinary MOS devices with changing the value of the BSIM3v3 parameter UA (first-order mobility degradation coefficient).

We propose the following model which can express the g_m-reduction.

1) BSIM3v3 SPICE model combines the source and drain resistance with R_{ds} (whose value depends on V_{gs}) as follows:

$$R_{ds} = \frac{RDSW(1 + PRWG \cdot V_{gs})}{W}, \tag{13}$$

where $RDSW$ is the source and drain resistance per unit channel width and $PRWG$ is a V_{gs} coefficient. R_{ds} is incorporated in the drain current expression of the simplified model as an explicit function of G_{ds0} shown in Eq. (3), and R_{ds} hardly affects the saturation voltage (V_{dsat}) of BSIM3v3. Note that G_{ds0} has R_{ds} in its denominator, and by making R_{ds} a function of V_{gs}, it is possible to accurately express the g_m-reduction for I_{dsr0} and I_{ds} mathematically.

2) R_{ds} provides the g_m-reduction for I_{dsr0} and I_{ds}, but they are not the same. I_{dsr0} with a larger absolute value has larger g_m-reduction, so that it can give most appropriate g_m-reduction in order to compensate the value of I_{vrs}, which is $I_{dsr0} - I_{ds}$.

3) R_{ds} has little influence on V_{dsat}, and it can be utilized independently of AGS.

4) AGS can be used to optimize the absolute value of I_{ds}, through V_{dsat}.

5) For HV MOS devices, both V_{gs}-caused mobility degradation effect and g_m-reduction occur at the same time and influence of the latter is more predominant. So in the HV MOS model, it is possible to ignore the mobility degradation effect. By defining μ_{eff} as a constant regarding to V_{gs}, we can obtain about five times faster optimization of the parameters for the parameter extraction tool.

7. Characteristics of R_{ds} in BSIM3v3

In order to introduce R_s and R_d precisely to the MOS model, we define V'_{gs} and V'_{ds} as follows:

$$V'_{gs} = V_{gs} - R_s \cdot I_{ds}, \tag{14}$$

$$V'_{ds} = V_{ds} - (R_s + R_d) \cdot I_{ds}. \tag{15}$$

Here, V'_{gs} is the effective gate-source voltage and V'_{ds} is the effective drain-source voltage. If R_s and R_d are defined another devices from MOSFET in the model (such as LEVEL2 and LEVEL3 models), we can obtain accurate solution of V'_{gs} and V'_{ds}: however this technique makes the simulation matrix bigger and increases calculation time necessary for the Newton method. Hence, after BSIM1 model was proposed, a simplified model of R_s and R_d has been incorporated in the MOSFET model, in order to cope with simulation of large scale circuits, assuming that R_s and R_d have small values in the sub-micron devices.

In BSIM3v3 model, R_{ds} is simply added to the channel resistance R_{ch} to obtain the total MOSFET resistance R_{tot}:

$$R_{tot} = R_{ch} + R_{ds}. \tag{16}$$

The second technique for simplification is to assume that the value of R_{ch} does not depend on the voltage drop of R_{ds} even though this is not strictly accurate according to physical meanings of R_s and R_d. By these two simplification techniques, R_{ds} in BSIM3v3 just works in a manner to make the drain current smaller, and we can understand this clearly by comparing simulation results of the I-V characteristics of MOSFET ($R_{ds} = 0$) with resistance devices (with the value of R_{ds} /2) added to source and drain sides and that of MOSFET where R_{ds} is given as a parameter. Furthermore, calculation of R_{ds} versus V_{dsat} shows that the value of V_{dsat} is almost constant against changes in R_{ds}, and it agrees with the value of V_{dsat} obtained assuming $R_{ds} = 0$: in other words, R_{ds} of BSIM3v3 does not affects the value of V_{dsat}. In our proposed model, we express g_m-reduction in I-V characteristics by making this R_{ds} dependent on V_{gs}.

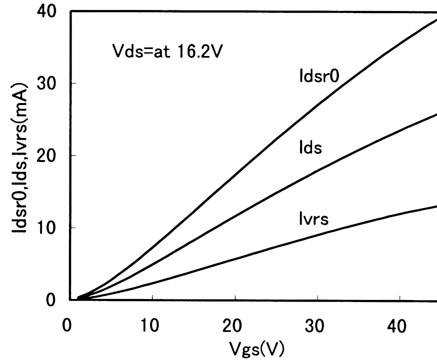

Fig. 5 Simulated I_{dsr0}, I_{ds} and I_{vrs} with the bi-directional HV MOS model.

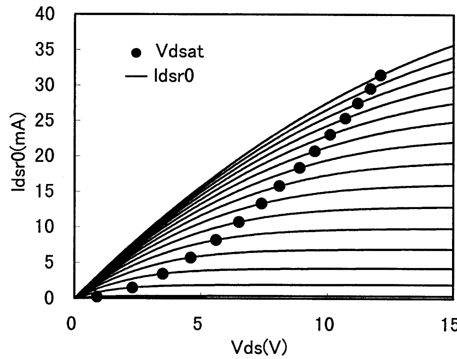

Fig. 6 Simulated I_{ds}-V_{ds} characteristics with $VSAT = 1\times10^9$, $V_{rs} = 0$ and V_{dsat} optimized by AGS.

8. Verification of Bi-Directional HV MOS Device Parameter Extraction Technique with Uni-Directional HV MOS Model

In this section we examine that the bi-directional HV MOS modeling technique does not represent uni-directional HV MOS devices well, and on the basis of the result we will try to establish a uni-directional HV MOS model parameter extraction technique. Figure 5 shows the simulated results of I_{dsr0}, I_{ds} and I_{vrs} in the saturation region ($V_{ds} = 16.2$ V) of the Step II parameters. Figure 6 shows the simulated I-V characteristics, ignoring velocity saturation effect ($VSAT = 1 \times 10^9$) and the value of V_{rs} is zero ($AGS = 0$), and also with the inserted values of V_{dsat} (●) optimized by AGS. The graph indicates the following:

1) I_{dsr0} is a value where I-V characteristics saturates at the V_{dsat} point shown by (●).

2) Based on Fig. 5 and Fig. 6, the value of V_{dsat} is larger to the extent that I_{dsr0} compensates the value of I_{vrs}.

3) I_{ds} cannot express g_m-reduction accurately at large V_{dsat} in high V_{gs} region. For the HV MOS model, g_m-reduction starts appearing as the V_{dsat} becomes smaller. Suppose I_{vrs} is zero and the value of V_{dsat} is such as to optimize I_{ds}, Fig. 6 shows that it is

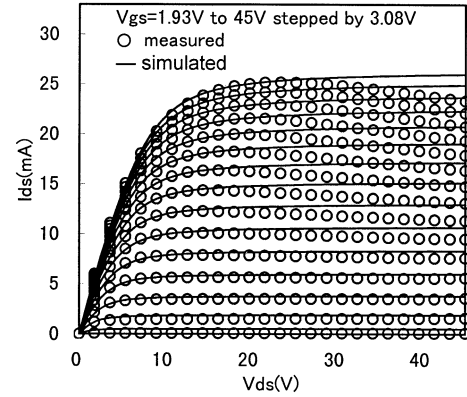

Fig. 7 Comparison between the measured and simulated (with the uni-directional model) I-V characteristics of the 45 V n-channel HV MOS device.

possible to express the g_m-reduction more accurately. Further, Fig. 4 shows that measured drain conductance (g_{ds}) is negative in high V_{gs} region. The BSIM3v3 SPICE model employs Early voltage to express the I-V characteristics in the saturated region so that the value of g_{ds} does not fall negative. In the circuit simulation, negative g_{ds} model causes divergence. Specifically, in the modeling technique, it is not allowed to express negative values of g_{ds}. Further for the circuit design with HV MOS devices, usually we can ignore g_{ds} reduction in the region with larger V_{gs} and V_{ds}, so that we exclude this region when optimizing the model parameters.

9. Proposed Parameter Extraction Technique for Uni-Directional HV MOS Device Modeling

In this section we describe the proposed parameter extraction technique for the uni-directional HV MOS model which can be implemented by using a SPICE model parameter extraction system, such as UTMOST [7].

1) First, extract all BSIM3v3 parameters by the standard method (step I in Table 1).

2) Then set the value of $VSAT$ to a large value (e.g., 1×10^9) assuming the long channel model.

3) Optimize the parameters of $U0$, $RDSW$, $PRWG$, AGS, and $DELTA$ together in all the triode region (up to close to the saturation region) i.e., from ($V_{ds} = 0$ V, $V_{gs} = 1.93$ V) to ($V_{ds} = 20$ V, $V_{gs} = 45$ V). $RDSW$ and $PRWG$ have to be optimized such that R_{ds} expresses g_m-reduction of I_{dsr0} while AGS has to be optimized such that A_{bulk} and V_{dsat} compensate for I_{vrs}.

4) Optimize $PDIBLC1$ and $PDIBLC2$

Since optimization of the absolute value of I_{ds} and g_m interact with each other, it is necessary to optimize them simultaneously. Step IV in Table 1 shows extracted parameter values based on the above procedure, and Fig. 7 shows a comparison between the

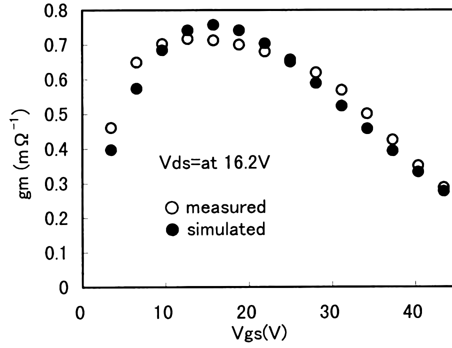

Fig. 8 Comparison between the measured and simulated (with the uni-directional HV MOS model) g_m characteristics.

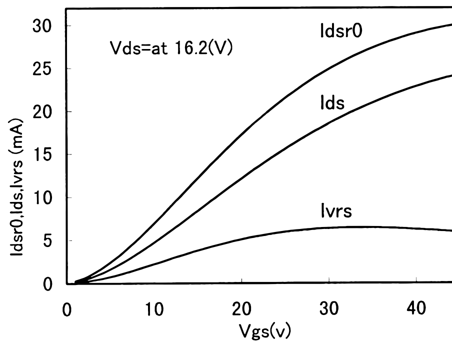

Fig. 9 Simulated I_{dsr0}, I_{ds} and I_{vrs} with the uni-directional HV MOS model.

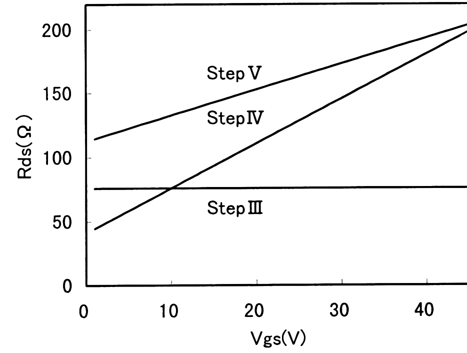

Fig. 10 Calculated R_{ds} as a function of V_{gs}.

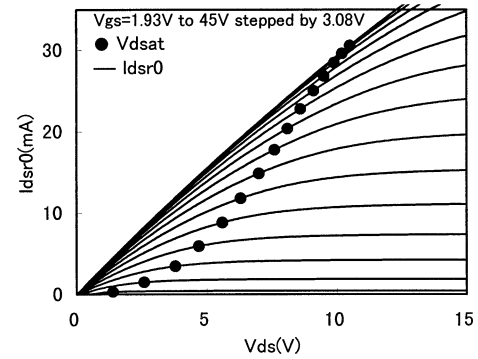

Fig. 11 Simulated *I-V* characteristics with $VSAT = 1 \times 10^9$, $AGS = 0$, $PRWG = 0.092$ and V_{dsat} optimized by AGS.

measured and simulated *I-V* characteristics. Figure 8 shows a comparison between the measured and simulated results for g_m. In Fig. 7, we see that good agreement is obtained between the measured and simulated results (except for the region where negative g_{ds} appears). Also we see that Fig. 8 shows g_m-reduction. Figure 9 shows the simulation results of I_{dsr0}, I_{ds} and I_{vrs} using the parameters obtained based on the uni-directional HV MOS model and the new parameter extraction technique. Step IV in Fig. 10 shows the calculated R_{ds} as a function of V_{gs}. Figure 11 shows the simulated *I-V* characteristics with $VSAT = 1 \times 10^9$, $AGS = 0$ and g_m-reduction caused by R_{ds} (Step IV $PRWG = 0.092$), and inserted V_{dsat} (●) optimized by AGS.

In this paragraph we will try to verify the parameter extraction technique for uni-directional HV MOS model.

1) Figure 8 proves that the uni-directional HV MOS model and the parameter extraction technique well-express the g_m-reduction in the saturation region of I_{ds}. I_{vrs} in Fig. 5 is a linear function of V_{gs}. However, in Fig. 9, I_{vrs} has changed to a non-linear function against V_{gs}, which results in optimizing the g_m-reduction of I_{ds}.

2) Step IV in Fig. 10 indicates that R_{ds} has a large dependence on the value of V_{gs}. The value of R_{ds} of ordinary devices does not depend on the value of V_{gs}.

3) Figure 11 shows that because of the V_{gs} dependence on R_{ds}, I_{dsr0} provides g_m-reduction.

4) In Fig. 7, accuracy of simulation decreases in the linear region with higher value of V_{gs}. This is because R_{ds} provides the g_m-reduction in all the region. However, g_m-reduction due to the drain-side offset region appears only in the saturation region. To compensate for the worsening accuracy, it is effective to implement Step IV again by setting the channel length modulation parameter $PCLM = 0$. The 0 value of $PCLM$ amplifies the g_m-reduction in the saturation region, so that V_{gs} dependence of R_{ds} is optimized smaller (Step V in Table 1). As a result of this, g_m-reduction caused by R_{ds} in the linear region gets smaller. Step V in Table 1 shows the parameters with $PCLM = 0$ and Fig. 12 shows the comparison between the measured and simulated *I-V* characteristics in the triode region. Figure 13 shows I_{ds}-V_{gs} characteristics in triode region. Note that I_{ds} monotonically increases under the condition of $V_{gs} \leq 40\,\text{V}$, however, I_{ds} slightly decreases when $V_{gs} \geq 40\,\text{V}$, and this phenomenon is more predominant when $V_{ds} = 1\,\text{V}$ than $V_{ds} = 2\,\text{V}$. This is due to the decrease of the channel voltage of the drain terminal by the influence of the gate electric field.

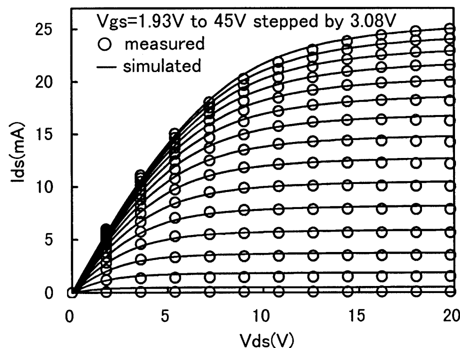

Fig. 12 Comparison between the measured and simulated (with the uni-directional HV MOS model and $PCLM = 0$) *I*-*V* characteristics in the triode region.

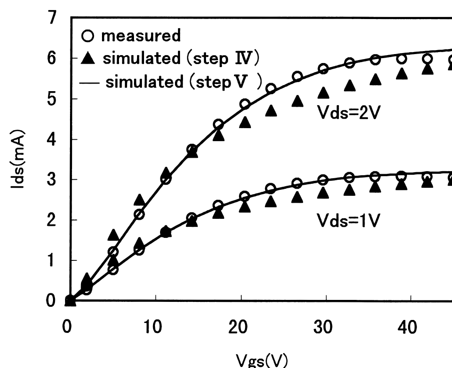

Fig. 13 Comparison between the measured and simulated (with the uni-directional HV MOS model) I_{ds}-V_{gs} characteristics in triode region.

10. Accuracy to Cope with Channel Length and Width

In order to utilize R_{ds} of the uni-directional HV MOS device, the value of RSH (source drain sheet resistance in ohm per square) must be set to zero, and by making R_{ds} dependent on W, g_m-reduction for HV MOS devices with different W can be expressed in our model. For different channel length of bi-directional and uni-directional HV-MOS devices, use the following equations of BSIM3v3 model:

$$dL = LINT + \frac{LL}{L^{LLN}}, \tag{17}$$

$$L_{eff} = L_{drawn} - 2dL, \tag{18}$$

where $LINT$ is a length offset fitting parameter from *I*-*V* without bias, LL is a coefficient of length dependence for length offset, LLN is a power of length dependence for length offset, L_{drawn} is a CAD drawn channel length, and L_{eff} is an effective channel length. We applied the above model to the 45 V HV MOS device and was able to extract highly accurate parameters with the standard channel length of 3.2 μm and $L = 4\,\mu$m respectively though an error of 5% was observed for $L = 4.8\,\mu$m. Our experience shows that *I*-*V* characteristics change against the channel of the HV MOS device depends mainly on the density and length of the offset region but L dependency of Eqs. (17),(18) is effective only in a limited region. For HV MOS device, impedance control of a device by channel length is not effective and mostly it is controlled by offset region. For the 45 V HV MOS device, drain current difference between $L = 3.2\,\mu$m and $L = 4.8\,\mu$m at $V_{gs} = 45$ V was small (about 7%), and hence in our actual LSI design with 45 V n-channel HV MOS device, we use only the standard channel length of $L = 3.2\,\mu$m.

11. Circuit Simulation Accuracy

As described before, our model can express the *I*-*V* characteristics (static characteristics) of the HV MOS device, and in this section we examine our modeling accuracy for the dynamic characteristics (i.e., capacitance model). The HV MOS device physically operates in triode region for almost all the voltage range for circuit design, but for the our model,we assume that it operates in the saturation region (when $V_{ds} > V_{dsat}$), and hence we need some care for the capacitance model. The BSIMv3 intrinsic capacitance model consists of 9 kinds of capacitances between each terminal (with directional features) and these are voltage dependent in triode region whereas they are constant in the saturation region, and the total of each capacitance between terminals is fairly constant in both regions. The voltage dependent intrinsic capacitance can be obtained by differentiating channel charges with respect to the corresponding voltage between terminals, and hence BSIM3v3 parameters obtained by *I*-*V* characteristics are also intrinsic capacitance model parameters. According to the above-mentioned physical meaning difference, our proposed model shows some discrepancy to the intrinsic capacitance model. Furthermore it is difficult to model the diffusion capacitance in the offset region accurately (as shown in Fig. 5 in [5]) due to the complicated depletion region effect in the offset region. Difference between the simulation ($CAPMOD = 1$, $XPART = 0$) and measurement of the circuit delay time of a level shift circuit incorporated in the actual LSI was 15% (simulated value was smaller). Currently, the HV MOS devices are not used for high speed system, and the discrepancy between the simulation and measurement is not a problem: however, care must be taken when applying this model to the circuit design of high speed operation.

12. Conclusion

We propose a new modeling technique for uni-directional HV MOS devices by extending the bi-directional HV MOS model and adopting a new pa-

rameter extraction technique. Uni-directional HV MOS devices do not have source resistance due to the offset region, however, the bi-directional HV MOS model we previously proposed inherently includes source resistance. Hence, if we apply the bi-directional HV MOS model and its parameter extraction technique directly to uni-directional HV MOS devices, we have to compensate the source resistance model component. However this compensation makes it difficult to represent the g_m-reduction phenomenon which is inherent to HV MOS devices, and causes large discrepancies between the measured and simulated I-V characteristics of the uni-directional HV MOS device. We propose to assign physical meanings and values which are different from the original BSIM3v3 equations to two of its main parameters. Further, we propose to adopt a new parameter extraction technique. With this method we have succeeded in compensating the source resistance component while accurately expressing the g_m-reduction. Also the measured results confirmed the effectiveness of our proposed technique: the simulated I-V characteristics of n-channel uni-directional 45 V HV MOS devices using extracted parameters matched the measured results well. Since our method does not change any model equations of BSIM3vs, it can be applied to any SPICE simulator on which the BSIM3v3 model runs.

References

[1] Y. Cheng, M.-C. Jeng, Z. Liu, J. Hubg, M. Chen, P.K. Ko, and C. Hu, “A physical and scalable I-V model in BSIM3v3 for analog/digital circuit simulation,” IEEE Electron Devices, vol.44, no.2, pp.277–284, Feb. 1997.

[2] J.H. Huang, Z.H. Liu, M.C. Jeng, K. Hui, M. Chan, P.K. Ko, and C. Hu, BSIM3 Manual (version 2.0), University of California, Berkeley, 1994.

[3] BSIM3v3 Manual (final version), University of California, Berkeley, 1995.

[4] T. Myono, S. Kikuchi, K. Iwatsu, E. Nishibe, T. Suzuki, Y. Sasaki, K. Itoh, and H. Kobayashi, “Modeling technique for high-voltage MOS devices with BSIM3v3 SPICE,” Electronics Letters, vol.34, no.18, pp.1790–1791, Sept. 1998.

[5] T. Myono, S. Kikuchi, K. Iwatsu, E. Nishibe, T. Suzuki, Y. Sasaki, K. Itoh, and H. Kobayashi, “High-voltage MOS device modeling with BSIM3v3 SPICE model,” IEICE Trans. Electron., vol.E82-C, no.4, pp.630–637, April 1999.

[6] T. Myono, E. Nishibe, S. Kikuchi, K. Iwatsu, T. Suzuki, Y. Sasaki, K. Itoh, and H. Kobayashi, “Modeling and parameter extraction technique for high-voltage MOS device,” Proc. International Symposium on Circuits and Systems, pp.230–233, Orlando, Florida, June 1999.

[7] UTMOST III Extraction manual, vol.1, ver. 12.03, SILVACO International, Santa Clara, CA.

Appendix

Since our HV MOS model copes with only in strong inversion region, V_{gseff} is given by $V_{gseff} = V_{gs} - V_{th}$ and equations of (4)–(6) can be rewritten as follows:
Equation (4): Bulk charge parameter

$$A_{bulk} = \left(1+\frac{K1}{2\sqrt{\phi_s - V_{bs}}}\left\{\frac{A0\cdot L}{L+2\sqrt{XJ\cdot X_{dep}}}\cdot\left[1-AGS\cdot(V_{gs}-V_{th})\left(\frac{L}{L+\sqrt{XJ\cdot X_{dep}}}\right)^2\right]+\frac{B0}{W+B1}\right\}\right)\frac{1}{1+KETA\cdot V_{bs}},$$

where ϕ_s is the surface potential, X_j is the junction depth, X_{dep} is the depletion width in the substrate, $K1$ is the first-order body effect coefficient, $A0$ is the bulk charge effect coefficient for channel length and V_{bs} is the substrate bias voltage.
Equation (5): Saturation voltage
Intrinsic case ($R_{ds} = 0$)

$$V_{dsat} = \frac{E_{sat}L(V_{gs}-V_{th})}{A_{bulk}E_{sat}L + V_{gs} - V_{th}},$$

where, E_{sat} is Critical electrical field and is given by

$$E_{sat} = \frac{2\cdot VSAT}{\mu_{eff}}. \tag{A$\cdot$1}$$

If $VSAT$ is very large we can get the following equation.

$$V_{dsat} \approx \frac{V_{gs}-V_{th}}{A_{bulk}}. \tag{A$\cdot$2}$$

Equation (6): Effective drain voltage

$$V_{dseff} = V_{dsat} - \frac{1}{2}\Big[V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat}-V_{ds}-\delta)^2 + 4\delta V_{dsat}}\Big]. \tag{A$\cdot$3}$$

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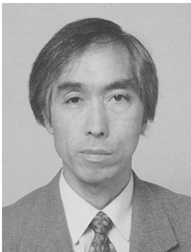

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