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LETTER

Dynamic Power Dissipation of Track/Hold Circuit

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SUMMARY This paper describes the formula for dynamic power dissipation of a track/hold circuit as a function of the input frequency, the input amplitude, the sampling frequency, the track/hold duty cycle, the power supply voltage and the hold capacitance for a sinusoidal input.

key words: *track/hold circuit, sampling, dynamic power dissipation, low power circuit design*

1. Introduction

A Track/Hold (T/H) circuit is an essential component for data acquisition systems, and let us consider the T/H circuit shown in Fig. 1. When its power consumption is discussed, usually only the static power consumed in the input and output buffers is considered [1], [2]. However the hold capacitor C_H is charged from power supply V_{dd} or discharged to GND through the input buffer according to the input signal; this leads to some power consumption which we call "the dynamic power dissipation of the T/H circuit." In most cases this dynamic power dissipation is not accounted for, but – as the input frequency increases and low power circuit design is demanded – this power becomes not negligible. Hence, in this paper, we will consider the formula for the dynamic power dissipation of the T/H circuit as a function of several parameters.

2. Formula for Dynamic Power Dissipation

Proposition: Consider a T/H circuit in Fig. 1 where we assume that the input buffer and sampling switch are ideal and the input signal and the sampling clock are not synchronized. In other words, the incoherent sampling is performed [3]. Then its dynamic power dissipation, $P_{T/H}$, of the T/H circuit for a sinusoidal input ($V_{in}(t) = A\sin(2\pi f_{in}t) + V_{dd}/2$) is given as follows:

$$P_{T/H} = 2AC_H V_{dd} f_{in}\left[r + (1-r)\left|\mathrm{sinc}\left((1-r)\pi\frac{f_{in}}{f_s}\right)\right|\right] \tag{1}$$

where $\mathrm{sinc}(x) := \sin(x)/x$, f_{in} is the input frequency, A is the input amplitude, f_s is the sampling frequency, r is the track/hold duty cycle (in other words, r/f_s is the duration in track mode while $(1-r)/f_s$ is the duration in hold mode, and $0 \le r \le 1$), V_{dd} is the power supply voltage and C_H is the hold capacitor.

Before we give the general proof of Eq. (1), we will consider some special cases.

A. Power Dissipation in Track Mode ($r = 1$): Let us consider the special case where the sampling switch is always ON and hence r=1 . Then during $0 \le t < 1/(2f_{in})$, charge of $2AC_H$ is provided to the hold capacitor C_H from V_{dd} through the input buffer while during $1/(2f_{in}) \le t < 1/f_{in}$, the hold capacitor is discharged to GND through the input buffer (Fig. 2); hence in this case the dynamic power dissipation $P_{r=1}$ is given by

$$P_{r=1} = 2AC_H V_{dd} f_{in}. \tag{2}$$

We see that $P_{r=1}$ is equal to $P_{T/H}$ in Eq. (1) with $r = 1$, and note that this formula (Eq. (2)) is similar to the following well-known dynamic power dissipation formula for digital CMOS logic where $2A = V_{dd}$ [4]:

$$P_{logic} = C_H V_{dd}^2 f_{toggle}.$$

Here f_{toggle} is the number of the logic gate output toggles per unit time.

B. Power Dissipation in Impulse Sampling ($r = +0$): Next let us consider the case where the duration in

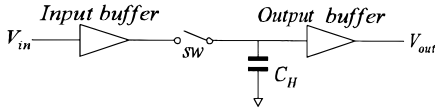

Fig. 1 A T/H circuit which consists of an input buffer, a sampling switch SW, a hold capacitor C_H and an output buffer.

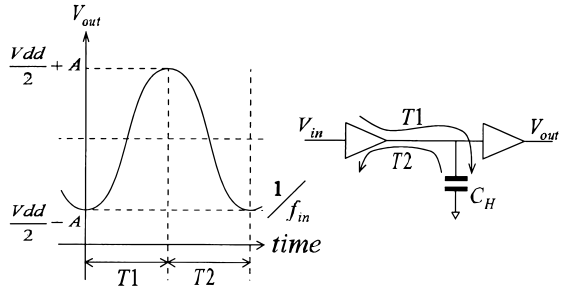

Fig. 2 The output waveform of the T/H circuit for a sinusiodal input when $r = 1$. During $T1$ the hold capacitor is charged from the power supply V_{dd} through the input buffer while during $T2$ it is discharged to GND.

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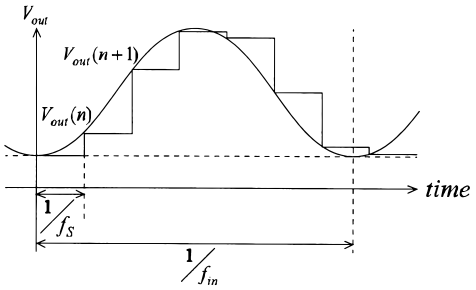

Fig. 3 The input and output waveforms of the T/H circuit when the duration in track mode approaches zero (i.e., $r = +0$).

track mode approaches zero and the one in hold mode approaches $1/f_s$ (i.e., $r \to +0$); this case happens such as in impulse sampling. Then the output waveform of the T/H circuit is given in Fig. 3 and the hold capacitor C_H is charged/discharged by the amount of $Q_{n,n+1}$ from time n to $n+1$, where

$$\begin{aligned} &Q_{n,n+1} \\ &= AC_H \left[\sin\left(2\pi\frac{f_{in}}{f_s}(n+1)\right) - \sin\left(2\pi\frac{f_{in}}{f_s}n\right)\right] \\ &= 2AC_H \sin\left(\pi\frac{f_{in}}{f_s}\right)\cos\left(2\pi\frac{f_{in}}{f_s}\left(n+\frac{1}{2}\right)\right). \end{aligned} \tag{3}$$

Here if $Q_{n,n+1} \geq 0$, C_H is charged from V_{dd}, while if $Q_{n,n+1} < 0$, C_H is discharged to GND by an amount of $|Q_{n,n+1}|$. Hence the dynamic power dissipation $P_{r=0}$ is given by

$$P_{r=0} = \frac{1}{2}V_{dd}f_s\overline{|Q|}. \tag{4}$$

Here $\overline{|Q|}$ is defined by

$$\overline{|Q|} := \lim_{N\to\infty}\frac{1}{N}\sum_{n=0}^{N-1}|Q_{n,n+1}|. \tag{5}$$

The coefficient of "1/2" in Eq. (4) is due to the fact that when the charge Q is charged to C_H from V_{dd} during $1/f_s$ and discharged to GND during next $1/f_s$, then the power of $V_{dd}Q(f_s/2)$ is dissipated. Since we assume that the input signal and the sampling clock are *not* synchronized, f_{in}/f_s is not a rational number (e.g., not like $f_{in}/f_s = 0.5$) [3], we obtain the following (see also Appendix):

$$\begin{aligned} &\lim_{N\to\infty}\frac{1}{N}\sum_{n=0}^{N-1}\left|\cos\left(2\pi\frac{f_{in}}{f_s}\left(n+\frac{1}{2}\right)\right)\right| \\ &\quad = \frac{1}{2\pi}\int_0^{2\pi}|\cos(x)|dx = \frac{2}{\pi}. \end{aligned} \tag{6}$$

Hence it follows from Eqs. (3), (5) and (6) that $\overline{|Q|}$ is given by

$$\begin{aligned} \overline{|Q|} &:= \lim_{N\to\infty}\frac{1}{N}\sum_{n=0}^{N-1}|Q_{n,n+1}| \\ &= 2AC_H\left|\sin\left(\pi\frac{f_{in}}{f_s}\right)\right| \\ &\quad \times \lim_{N\to\infty}\frac{1}{N}\sum_{n=0}^{N-1}\left|\cos\left(2\pi\frac{f_{in}}{f_s}\left(n+\frac{1}{2}\right)\right)\right| \\ &= \frac{4}{\pi}AC_H\left|\sin\left(\pi\frac{f_{in}}{f_s}\right)\right|. \end{aligned} \tag{7}$$

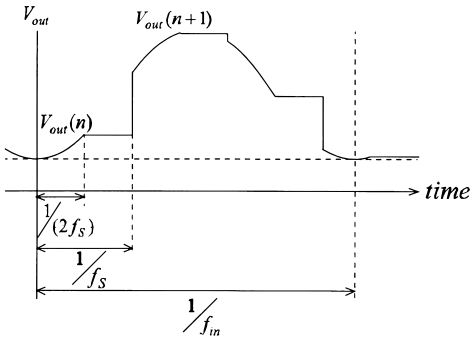

Fig. 4 The output waveform of the T/H circuit for a sinusiodal input when durations of track and hold modes are equal (i.e., $r = 0.5$).

Then it follows from Eqs. (4) and (7) that

$$\begin{aligned} P_{r=0} &= \frac{2}{\pi}AC_HV_{dd}f_s\left|\sin\left(\pi\frac{f_{in}}{f_s}\right)\right| \\ &= 2AC_HV_{dd}f_{in}\left|\frac{\sin(\pi f_{in}/f_s)}{\pi f_{in}/f_s}\right| \\ &= 2AC_HV_{dd}f_{in}\left|\mathrm{sinc}\left(\pi\frac{f_{in}}{f_s}\right)\right|. \end{aligned} \tag{8}$$

We see that $P_{r=0}$ in Eq. (8) is equal to $P_{T/H}$ in Eq. (1) with $r = 0$.

C. Power Dissipation in General Case: Consider the general case where the ratio of durations of track and hold modes is $r:(1-r)$. Figure 4 shows the output waveform of the T/H circuit for a sinusiodal input when $r = 0.5$. Since the ratio of the track mode per a sampling period is r, the dynamic power, P_{Track}, consumed in track mode is given by

$$\begin{aligned} P_{Track} &= rP_{r=1} \\ &= 2rAC_HV_{dd}f_{in}. \end{aligned} \tag{9}$$

During the transition from n-th hold time to $(n+1)$-th track time, the hold capacitor C_H is charged/discharged by an amount of $Q_{n+r,n+1}$, where

$$\begin{aligned} &Q_{n+r,n+1} \\ &= AC_H\left[\sin\left(2\pi\frac{f_{in}}{f_s}(n+1)\right) - \sin\left(2\pi\frac{f_{in}}{f_s}(n+r)\right)\right] \\ &= 2AC_H\sin\left((1-r)\pi\frac{f_{in}}{f_s}\right)\cos\left(2\pi\frac{f_{in}}{f_s}\left(n+\frac{1+r}{2}\right)\right). \end{aligned}$$

Here if $Q_{n+r,n+1} \geq 0$, C_H is charged from V_{dd}, while if $Q_{n+r,n+1} < 0$, C_H is discharged to GND by an amount

of $|Q_{n+r,n+1}|$. Hence the dynamic power, P_{Hold}, consumed during the transition from hold to track modes is given by

$$P_{Hold} = \frac{1}{2} V_{dd} f_s \overline{|Q_r|}, \tag{10}$$

where $\overline{|Q_r|}$ is defined by

$$\overline{|Q_r|} := \lim_{N\to\infty} \frac{1}{N} \sum_{n=0}^{N-1} |Q_{n+r,n+1}|. \tag{11}$$

Assuming that f_{in}/f_s is an irrational number, we obtain the following equation similar to Eq. (6):

$$\begin{aligned} &\lim_{N\to\infty} \frac{1}{N} \sum_{n=0}^{N-1} \left| \cos\left(2\pi \frac{f_{in}}{f_s}\left(n + \frac{1+r}{2}\right)\right)\right| \\ &\quad = \frac{1}{2\pi} \int_0^{2\pi} |\cos(x)| dx = \frac{2}{\pi}. \end{aligned} \tag{12}$$

Then it follows from Eqs. (11) and (12) that $\overline{|Q_r|}$ is given by

$$\begin{aligned} \overline{|Q_r|} &:= \lim_{N\to\infty} \frac{1}{N} \sum_{n=0}^{N-1} |Q_{n+r,n+1}| \\ &= 2AC_H \left|\sin\left((1-r)\pi \frac{f_{in}}{f_s}\right)\right| \\ &\quad \times \lim_{N\to\infty} \frac{1}{N} \sum_{n=0}^{N-1} \left| \cos\left(2\pi \frac{f_{in}}{f_s}\left(n + \frac{1+r}{2}\right)\right)\right| \\ &= \frac{4}{\pi} AC_H \left|\sin\left((1-r)\pi \frac{f_{in}}{f_s}\right)\right|. \end{aligned} \tag{13}$$

Hence it follows from Eqs. (10) and (13) that

$$\begin{aligned} &P_{Hold} \\ &= \frac{2}{\pi} AC_H V_{dd} f_s \left|\sin\left((1-r)\pi \frac{f_{in}}{f_s}\right)\right| \\ &= 2(1-r)AC_H V_{dd} f_{in} \left|\frac{\sin((1-r)\pi f_{in}/f_s)}{(1-r)\pi f_{in}/f_s}\right| \\ &= 2(1-r)AC_H V_{dd} f_{in} \left|\mathrm{sinc}\left((1-r)\pi \frac{f_{in}}{f_s}\right)\right|. \end{aligned} \tag{14}$$

Then it follows from Eqs. (9) and (14) that the total dynamic power $P_{T/H}$ is given by

$$P_{T/H} = P_{Track} + P_{Hold}$$

which yields to Eq. (1), and thus the proposition has been proved.

3. Numerical Calculation

Figure 5 shows the numerical calculation results of Eq. (1) in cases of $r = 0$, $r = 0.5$ and $r = 1.0$. Here the range of $f_{in} : f_s$ is greater than 1: 2 because some applications (such as wideband digitizing oscilloscopes incorporating equivalent-time sampling function) require such range. We see that in case of $r = 1.0$ the dynamic power dissipation is proportional to f_{in} while in case of $r = 0$ it takes the maximum value of $2AC_H V_{dd} f_{in}$ at $f_{in}/f_s = n + 1/2$ and the minimum value of 0 at $f_{in}/f_s = n$, where $n = 0, 1, 2, 3, ...$

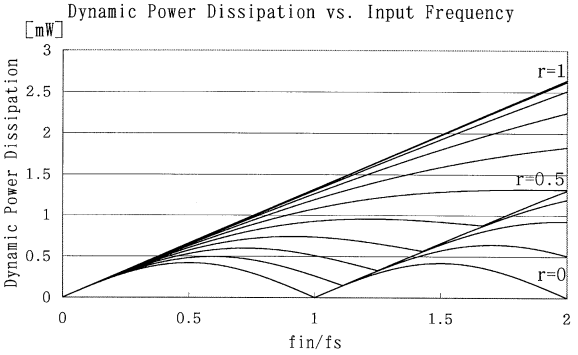

Fig. 5 The numerical calculation results of Eq. (1), where A=1 V, C_H=2 pF, V_{dd}=3.3 V, f_s=100 MHz and f_{in}=0 $\sim$ 200 MHz.

4. Conclusion

We have derived the formula for dynamic power dissipation—which will be important for high frequency input signal and sampling clock—of a track/hold circuit as a function of the input frequency, the input amplitude, the sampling frequency, the track/hold duty cycle, the power supply voltage and the hold capacitance for a sinusoidal input. This result may be also useful for some switched-capacitor circuits.

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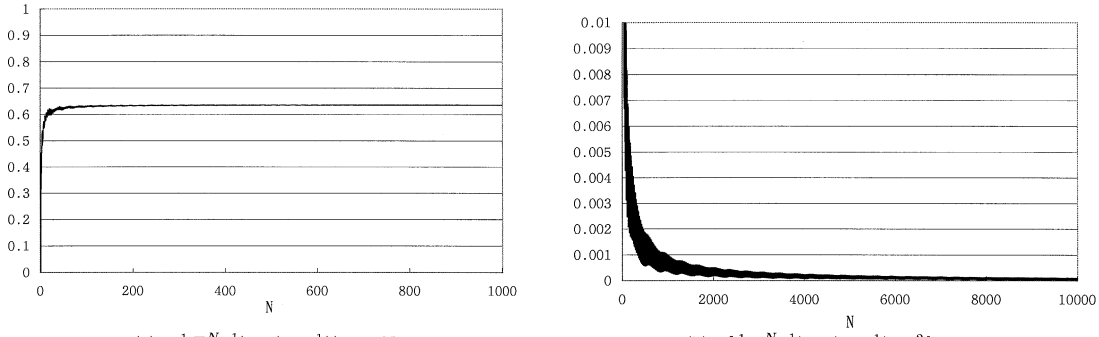
Appendix

This appendix discusses the validity of Eqs. (6) and



(a) $\frac{1}{N}\Sigma_{n=0}^{N-1}|\cos(n+\frac{1}{2})|$ vs. N

(a)

(b) $[\frac{1}{N}\Sigma_{n=0}^{N-1}|\cos(n+\frac{1}{2})-\frac{2}{\pi}]$ vs. N

(b)

Fig. A· 1 The numerical calculation result of $\frac{1}{N}\sum_{n=0}^{N-1}|\cos(2\pi\frac{f_{in}}{f_s}(n+\frac{1}{2}))|$ when f_{in}/f_s is equal to $1/(2\pi)$, an irrational number. In other words, the numerical calculation result of $\frac{1}{N}\sum_{n=0}^{N-1}|\cos(n+\frac{1}{2})|$ with respect to N, and we see that it converges to a value of $2/\pi$. (a) $\frac{1}{N}\sum_{n=0}^{N-1}|\cos(n+\frac{1}{2})|$ vs. N. (b) $[\frac{1}{N}\sum_{n=0}^{N-1}|\cos(n+\frac{1}{2})|-\frac{\pi}{2}]$ vs. N.

(12). Note that if input signal and the sampling are synchronized (i.e., the coherent sampling is performed) and hence f_{in}/f_s is a rational number [3], we do not have necessarily the results of Eqs. (6) and (12). Consider the case of Eq. (6) and, for example, if $f_{in}/f_s = 0.5$, then

$$\cos\left(2\pi\frac{f_{in}}{f_s}\left(n+\frac{1}{2}\right)\right)=\cos\left(\pi\left(n+\frac{1}{2}\right)\right)=0$$

for all of an integer n and hence

$$\lim_{N\to\infty}\frac{1}{N}\sum_{n=0}^{N-1}\left|\cos\left(2\pi\frac{f_{in}}{f_s}\left(n+\frac{1}{2}\right)\right)\right|=0.$$

In other words, if f_{in}/f_s is a rational number,

$$\theta(n):=mod_{2\pi}\left(2\pi\frac{f_{in}}{f_s}\left(n+\frac{1}{2}\right)\right) \qquad (\mathrm{A}\cdot 1)$$

may take only specific values and may not cover all range from 0 to 2π; in that case Eq. (6) does not necessarily hold.

On the other hand, if input signal and the sampling are not synchronized and hence f_{in}/f_s is an irrational number [3], the following lemma is valid:

Lemma: When f_{in}/f_s is an irrational number, for a given $\delta(0\le\delta<2\pi)$ and an arbitrary $\epsilon>0$, there exists an integer n which satisfies $|\theta(n)-\delta|<\epsilon$. Here $\theta(n)$ is defined by Eq. (A· 1).

Then in this case $\theta(n)$ can cover (almost) all range from 0 to 2π and then Eq. (6) holds; this was confirmed by numerical simulation (Fig.A· 1). Similar arguments are valid also for Eq. (12).