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A New Coherent Sampling System with a Triggered Time Interpolation

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SUMMARY Equivalent-time sampling is a well-known technique to capture repetitive signals at finer time intervals than a sampling clock cycle time and it is widely used to implement waveform measurement with high time resolution. There are three techniques for implementing its time base (i.e., sequential sampling, random sampling and coherent sampling), and they have their respective advantages and disadvantages. In this paper we propose a new coherent sampling system which incorporates a pretrigger and time jitter reduction function for a fluctuating input signal which a random sampling system has, while maintaining the waveform recording efficiency of a conventional coherent sampling system. We also report on a technique for measuring a reference trigger time period accurately which is necessary to implement the proposed sampling system, and show its effectiveness through numerical calculations of its data recording time.

key words: *equivalent-time sampling, coherent sampling, random sampling, high time resolution, data recording time*

1. Introduction

There is a growing demand for a wideband digital storage oscilloscope (DSO) as a means for directly observing an ultra high-speed signal waveform [1]. Generally, the DSO uses an equivalent-time sampling technique to measure waveforms during high-speed sweeping, and there are three sampling systems for implementing its time base: sequential, random and coherent sampling systems [2]–[5]. Figure 1 shows the features of these sampling systems.

1) A sequential sampling system generates sampling pulses using the triggering time as a reference timing point, and using these sampling pulses, its data recording speed does not slow down even during high-speed sweeping; hence it is widely used for wideband sampling oscilloscopes on the market. However, since it has no self-running clock, a delay line is required for capturing sampling waveforms which precede the triggering time (i.e., pretrigger function), and this delay line restricts the frequency bandwidth of the system [6].

2) A random sampling system samples an input signal with a clock which is independent of an input signal, and measures the time difference between a trigger and the clock (using so-called a "time-interpolation" technique) to determine the sampling time. Hence, it incorporates a pretrigger function (without any delay line) that can measure an input waveform before triggering. However, a fixed clock random sampling system sometimes results in so-called a "bunching effect," where some of the waveform data are not captured at specific time points depending on the relationship between the signal and clock period and this is also called a "waveform missing phenomenon" [7]–[9]. On the other hand, a random sampling system that randomly shifts the sampling clock phase every time data is recorded, can avoid these phenomena, but it takes a relatively long time to randomize the clock phase and record the waveform data during high-speed sweeping [7], [10].

3) A coherent sampling system generates a sampling clock using a PLL so that the sampling clock period has a specific relationship with the time period of the input signal. Using this scheme, it can record data with high efficiency and without the waveform missing phenomenon. However, it suffers from fluctuations in input signal time period; the fluctuation of the input signal period has the same effect as sampling clock jitter on the waveform measurement [11].

Function / System	PreTrigger	Jitterless	Recording Time
Sequential	×	○	○
Random	○	○	×
Coherent	○	×	○
Proposed coherent sampling	○	○	○

Fig. 1 Features of equivalent-time sampling systems.

From the above discussions, we consider that if a sampling system has a sampling clock associated with an input signal time period as well as a trigger function, it can incorporate the pretrigger ability and record waveforms with high efficiency and without suffering from the effect of the input signal period fluctuation. Here, we propose such a new coherent sampling system, and in the following sections we describe its operation principle and implementation method, and show its effectiveness by numerical simulation.

2. Operation Principle

Figure 2 shows a block diagram of the proposed system. The synchronization circuit generates a synchronizing signal Sync at a trigger input when the Hold signal is "L" (called

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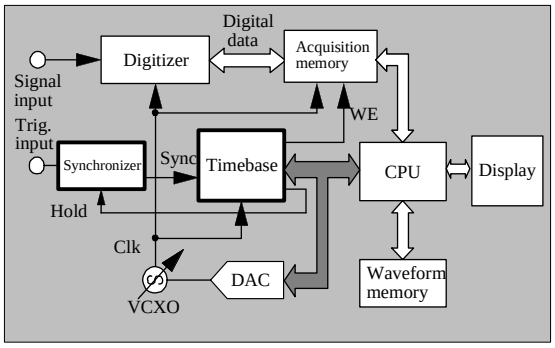


Fig. 2 Block diagram of the proposed sampling system.

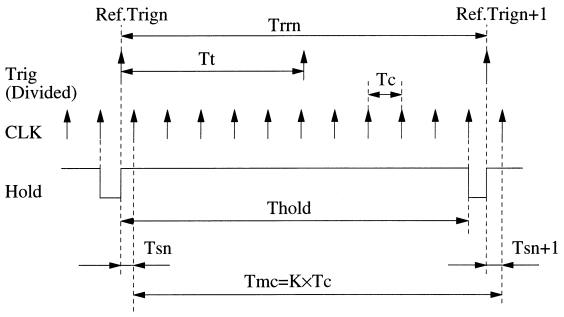


Fig. 3 Measurement of reference trigger time period.

"Ref.Trig") and makes trigger inputs invalid thereafter until the Hold signal becomes "L." The time base generates a ramp signal using Sync (= Ref.Trig) as a start signal, and it stops generating the ramp signal when a clock is input. Then it performs analog-to-digital conversion for the held voltage and obtains time-interpolated value Ts which is the time difference between Ref.Trig and the clock generation timing [12]. Instantaneous values of the input signal sampled in synchronization with the sampling clock in the digitizer are sequentially recorded in the acquisition memory. Then they are combined with the timing data Ts and transferred to the waveform memory to reconstruct a signal waveform. Note that those operations are to implement jitterless and pretrigger functions, and are the same as those in the fixed clock random sampling system.

In the proposed system, we also use the coherent sampling operations; first, reference trigger time period Trr is obtained from the timing information of the time base. Then, based on the result, clock period Tc can be controlled using a digital-to-analog converter (DAC) and a voltage controlled crystal oscillator (VCXO). In this proposed system, Tc is set so that the following Eq. (1) is satisfied for reference trigger time period Trr:

$$Tc = M/N \times Trr \tag{1}$$

where, N is the number of clock cycle times required for data recording, and M is the amount of data recorded per clock period. Also N and M are relatively prime integers.

On the other hand, note that a conventional coherent sampling system sets clock period Tc so that the following coherent sampling condition is met for input signal time period Tt [13]:

$$Tc = Nt/Md \times Tt \tag{1'}$$

where, Nt is the number of trigger time periods required for data recording, and Md is the record length to reconstruct a signal waveform. Also Nt and Md are relatively prime integers.

Figure 3 shows the relationship among reference trigger time period Trr_n, trigger which is picked-off from the input signal, clock and interpolated time. Let Thold be the duration from the time when $Ref.Trig_n$ is valid to the time when a series of operations of time-interpolation, data recording and data transfer are finished. Trr_n satisfies the following equation by expressing the trigger input timing for the first time after the Thold duration finishes as $Ref.Trig_{n+1}$.

$$Trr_n = Tt \times Ceiling[Thold/Tt] \tag{2}$$

where Ceiling[x] is the smallest integer equal to or greater than x.

If constant hold-off [9] is used, Thold becomes constant regardless of the value of Ts_n, and then if Tt is constant, Trr_n is also constant.

Suppose that the period from the clock immediately after $Ref.Trig_n$ to the clock immediately after $Ref.Trig_{n+1}$ is Tmc and also the number of clocks included in the period is K. Then we obtain the following equation and can calculate Trr_n using the two interpolated time data, Ts_n and Ts_{n+1}.

$$Trr_n = Ts_n + Tmc - Ts_{n+1} = K \times Tc - \delta Ts_n \tag{3}$$

where $\delta Ts_n = Ts_{n+1} - Ts_n$.

Then Eq. (4) is sufficient to satisfy Eq. (1):

$$Tc = Trr_n/(N/M) = Trr_n/(Y+X/M) \tag{4}$$

where, Y=Floor[N/M] and X<M, X and M are relatively prime integers, and Floor[x] is the greatest integer equal to or less than x.

For the sake of simplicity, suppose that "M" is the power of 2, then X is an odd number and clock period Tc can take any of M/2 values. However, by imposing a condition that the value of Tc should be the nearest to reference value Tc_0, Tc can be uniquely determined, and also X and Y can be determined by Eqs. (6) to (8) using a discriminant D given by Eq. (5):

$$D = Ceiling[Mod[Trr_n, Tc_0]/Tc_0 \times M] \tag{5}$$

$$Y = Floor[Trr_n/Tc_0]. \tag{6}$$

If D is an even number, X is given by:

$$X = Ceiling[Mod[Trr_n, Tc_0]/Tc_0 \times M]. \tag{7}$$

If D is an odd number, X is given by:

$$X = Floor[Mod[Trr_n, Tc_0]/Tc_0 \times M]. \tag{8}$$

3. Measurement Method of Reference Trigger Time Period

To determine the sampling clock period based on the reference trigger time period, it is necessary to measure the reference trigger time period highly accurately. Here, we report on such a measurement scheme which can avoid metastable phenomena of a synchronizing signal and reduce quantization errors during measurement of interpolation time Ts.

3.1 Synchronization Circuit Incorporating Frequency Division with Hysteresis Characteristics and Variable Hold-off Function

Since the input signal and the sampling clock are inherently asynchronous, the sampling system suffers from so-called a "metastable phenomenon" [14]. This metastable phenomenon occurs when the time (hold-off release) at which the Hold signal changes from "H" to "L" coincides with the time at which a trigger signal is input (see Fig. 3); in this case, synchronizing signal Sync is likely to remain at the output level close to the threshold. Once a metastable phenomenon occurs, the synchronizing signal remains in a non-defined logic state (i.e., it is not in state "1" nor state "0," but is at the middle level between logic "1" and "0") until the next trigger signal is input. As a result, the reference trigger time period will not satisfy the condition of "integer multiple of trigger cycle" in Eq. (2) and in such a case, controlling the clock period by measuring the reference trigger time period has no meaning.

We have devised a synchronization circuit which works as follows: first, it detects whether there is a trigger signal or not, using a time window of one-clock pulse width whose center is the time when a hold-off signal is released. Then if a trigger is detected, it changes the hold-off release timing to avoid generation of further metastable states.

If a constant hold-off is used, the time difference between the hold-off release and the next trigger input becomes constant [9]. Hence in this case Tc is enough to release the hold-off. As a result, the timing of the detection pulse is also shifted by 1-clock cycle. A sufficient condition for not generating any trigger during this time-shifted detection pulse period is that the trigger cycle must be longer than 2×Tc. If a hold-off is released in synchronization with the clock without using constant hold-off, the next trigger input timing will be distributed over one-clock period. At this time, as shown in Fig. 4, it is necessary to shift the timing for releasing the hold-off by 2×Tc and the trigger time period should be longer than 4×Tc. To meet these requirements, a frequency divider that automatically changes the division factor according to the trigger time period is needed.

This synchronization circuit controls the time period of the divided trigger signal to be within a certain range. Figure 5 shows a block diagram of the frequency divider and Fig. 6 shows the input/output characteristics of the control. When the number of triggers counted in the time window is smaller than a specified lower limit, the division factor is controlled to be decreased. On the other hand, when it is greater than a specified upper limit, the division factor is controlled to be increased. Moreover, hysteresis characteristics are provided to the control logic so that the divided time period does not repeat fluctuations between two values for a single input frequency; this is accomplished by setting the upper limit to a value greater than twice the lower limit. Then stable measurement of a reference trigger time period is possible if the

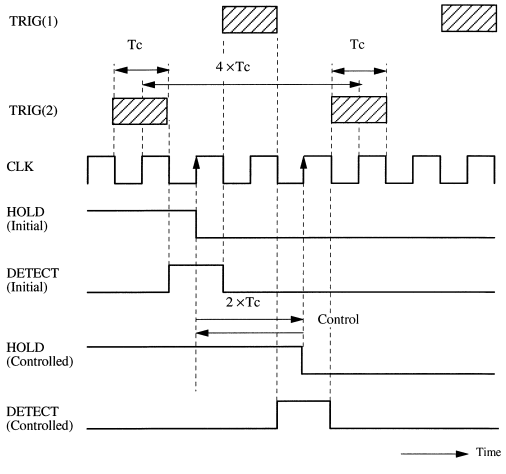


Fig. 4 Variable hold-off for metastable prevention. The minimum output time period of the frequency divider is determined on condition that it is not detected by a detection pulse when trigger input is in position (2) in the figure.

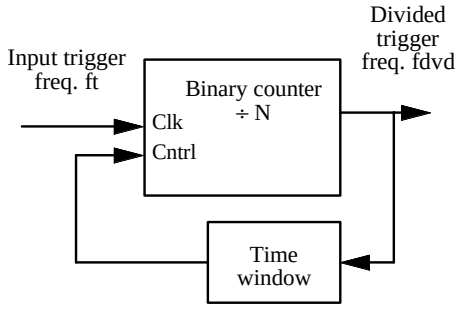


Fig. 5 Trigger signal frequency divider.

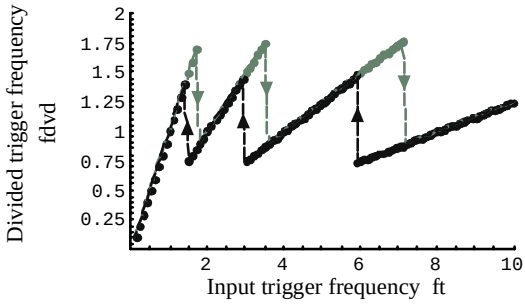


Fig. 6 Trigger signal frequency division control characteristics of circuit in Fig. 5. It has hysteresis characteristics so that the frequency after division does not repeat fluctuations between two values.

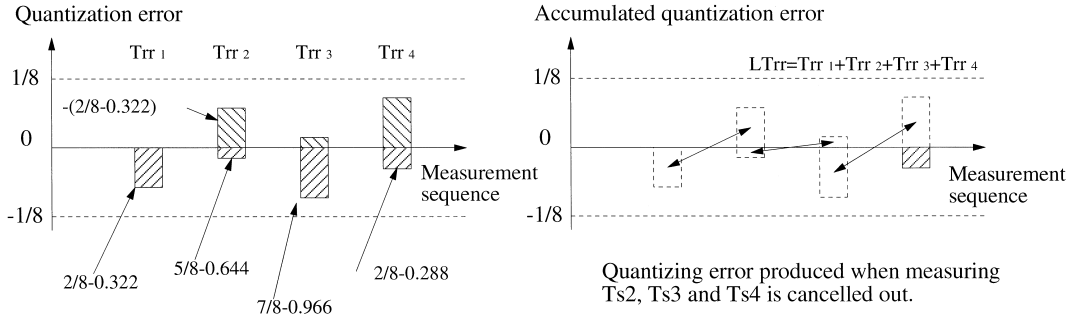


Fig. 7 Reduction of measurement errors.

fluctuations of the input frequency do not exceed the hysteresis width.

3.2 Reduction of Quantization Error

"M" shown in Eq. (1) is normally a finite value and the system design is carried out by specifying a maximum value Mmax (generally several hundred to several thousand). In this system, Tc/Mmax is a nominal time resolution (without considering noise or timing jitter) and interpolation time Ts has a quantization error of Tc/Mmax. On the other hand, even if we attempt to set a clock period so that measured value Trr meets the second term of Eq. (9) below, in order to record M data pieces per one clock period, Tc may be a value that satisfies the third term of Eq. (9) when the true value of Trr is Trr'. In this case, the system repeats recording of M' data pieces per clock period and causes the waveform missing phenomenon, even if it continues the sampling operation.

$$Tc=Trr/(Y+X/M)=Trr'/(Y+X/M') \quad (9)$$

where, M'<M, M' and X are relatively prime integers.

The strictest measuring accuracy of Trr is required when M=Mmax, M'=Mmax–1 and X=1. We have found that if the measuring accuracy of the reference trigger time period is $Tc/Mmax^2$, the waveform missing phenomenon can be avoided. However, this value is 1/Mmax of the system time resolution.

In order to solve this problem, we measure reference trigger time period Trr_n more than one time, average the measurements and improve the time resolution by a factor of the reciprocal of the square root of the number of measurement times. However, if Mmax is 2^{10}, it is necessary to average approximately 1 million reference trigger time periods, which requires a great deal of time.

Since the reference trigger time period Trr is expressed with highly-stable clock period Tc and the difference δTs between two successive time-interpolation values Ts's (as shown in Eq. (3)), we can improve the accuracy by a factor of the number of accumulation times by simply accumulating successive reference trigger time periods.

The left part of Fig. 7 is an example of a quantization error of Trr_1 to Trr_4 when Tt=2.0537, Tc=1, M=8, Thold=11 and an initial value of Ts (=Ts_1) is 0. The negative error shown with Trr_1 is a quantization error when Ts_2 is measured, and the negative error shown with Trr_2 is a quantization error when Ts_3 is measured. On the other hand, the quantization error of Ts_2 is added as a positive error (which has the opposite sign when Trr_2 is measured) and the difference between these two errors becomes the quantization error of Trr_2. The same arguments are valid for Trr_3 and Trr_4. Here, suppose that the accumulated value of measurement results of successive Trr_1, Trr_2, Trr_3 and Trr_4 is LTrr, then the quantizing error produced when measuring Ts_2, Ts_3 and Ts_4 is cancelled out and only the quantization error when Ts_5 is measured remains for Ltrr (see the right part of Fig. 7). When Trr is obtained by dividing this Ltrr by the accumulation number of times of Trr_n, the quantization error is reduced to 1/4.

4. Numerical Calculations

We have conducted numerical calculation of waveform recording times for the fixed clock random sampling, random sampling and proposed coherent sampling systems in order to evaluate the effectiveness of the proposed system, and here we report on the comparison results. The calculation conditions are as follows (which, we believe, are reasonable for practical situation):

1: The total number of data pieces recorded is set to 1,024. The number of interpolation points M per one clock period is set to 64 and 512. We record waveform data after the trigger input time point, and calculate the waveform recording time by repeating the sampling operation until the total data is recorded twice and averaging the required time. If the total data is not recorded during operation of M×200 time-interpolations, the sampling operation is suspended and the value obtained by dividing the total recording time by the number of the recorded data pieces is used.

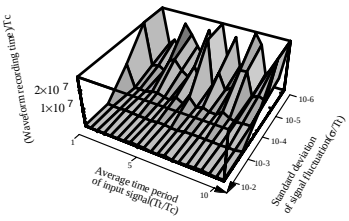
2: The period required for time-interpolation is set to 8×Tc, and data transfer time is set to 8×Tc/data. We also assume that the time required to randomize the clock phase in the random sampling system and the time required to change the clock period in the proposed system are 1,000×Tc.

3: We suppose that the clock period Tc or reference clock period Tc_0 is 1, and the clock is ideal (without fluctuations in time periods). Also, we assume that the input signal has fluctuations in time periods with a Gaussian distribution, and we consider the following two cases for the input signal:

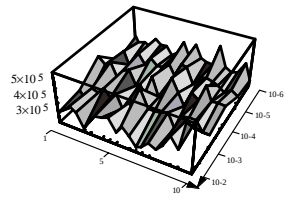
(A) The average time period of the target input signal has 21

levels (in 0.45 steps) in the range of 1 to 10 and the standard deviation of its fluctuations has 5 levels in the range of 10^{-2} to 10^{-6}.
(B) The average time period of the target input signal has 21 levels (in 0.005 steps) in the range of 10 to 10.1 and the standard deviation of its fluctuations has 4 levels in the range of 10^{-3} to 10^{-6}.
4: The accumulation number of times to find the reference trigger time period in this system is 8 when M=64 and 128 when M=512.

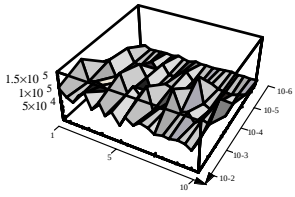
Figures 8 and 9 show the numerical calculation results; the same tendency is observed regardless of the value of M or the condition of the input signal. Table 1 shows maximum value Tmax and minimum value Tmin of waveform recording times with 84 target input signals in condition (B). From these results, we have obtained the following observations:
1: In the fixed clock random sampling, Tmax/Tmin reaches approximately 7,000 when M=64 and approximately 10,000



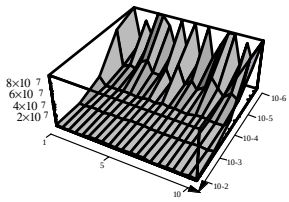
(a) Fixed clock random sampling. M = 64.



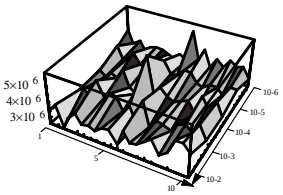
(c) Random sampling. M = 64.



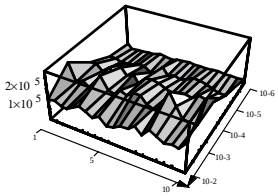
(e) Proposed coherent sampling. M = 64.



(b) Fixed clock random sampling. M = 512.

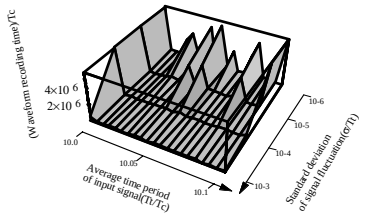


(d) Random sampling. M = 512.

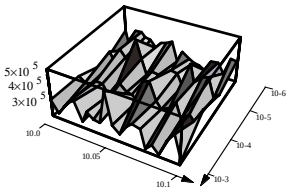


(f) Proposed coherent sampling. M = 512.

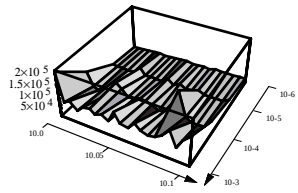
Fig. 8 Calculated waveform recording time in condition (A). The x-axis indicates the average time period of input signal, and the y-axis indicates the standard deviation of the fluctuation of the signal period, while z-axis indicates waveform recording time.



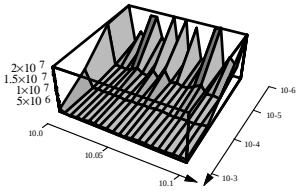
(a) Fixed clock random sampling. M = 64.



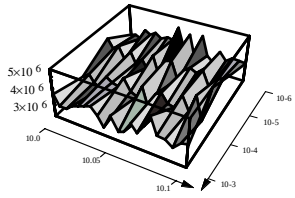
(c) Random sampling. M = 64.



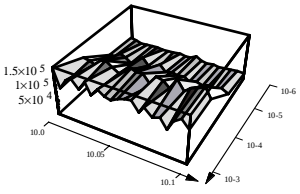
(e) Proposed coherent sampling. M = 64.



(b) Fixed clock random sampling. M = 512.



(d) Random sampling. M = 512.



(f) Proposed coherent sampling. M = 512.

Fig. 9 Calculated waveform recording time in condition (B). The x-axis indicates the average time period of input signal, and the y-axis indicates the standard deviation of the fluctuation of the signal period, while z-axis indicates waveform recording time.

Table 1 Comparison of calculated waveform recording time in sampling systems.

Sampling system	M	Maximum valueTmax	Minimum Value Tmin	Tmax/Tmin
Fixed clock random sampling	64	1.3×10^{8}	1.8×10^{4}	7.3×10^{3}
	512	9.0×10^{8}	8.8×10^{4}	1.0×10^{4}
Random sampling	64	5.0×10^{5}	2.2×10^{5}	2.3
	512	5.0×10^{6}	2.3×10^{6}	2.1
Proposed coherent sampling	64	2.0×10^{5}	1.1×10^{4}	19
	512	1.6×10^{5}	1.8×10^{4}	9.0

when M=512, which shows that the waveform recording time greatly varies depending on the property of the input signal. The recording time is longer when the waveform missing phenomenon occurs, and it occurs more frequently when an input signal with small fluctuations is recorded with high time resolution (with large M).

2: In the random sampling, Tmax/Tmin is approximately 2.3 when M=64 and approximately 2.1 when M=512, which shows that the waveform recording time is almost independent of the property of the input signal. However, Tmin reaches approximately 13 times (M=64) and 27 times (M=512) that of fixed clock random sampling. This means that the clock period randomizing scheme results in long waveform recording time.

3: In our proposed system, Tmax/Tmin is approximately 19 when M=64 and approximately 9 when M=512, which is at the middle between fixed clock random sampling and random sampling systems. However, it has a feature that the waveform recording time is short when signal fluctuation is small while it is long when signal fluctuation is large, as is clear from Fig. 8, and the reason is as follows: when the input signal fluctuation is small, the system performs a coherent sampling operation and records waveform data with high efficiency. On the other hand, when it is large, the system ends up recording waveform data randomly no matter how much the clock period is controlled. Tmin of the proposed method is smaller than that of fixed clock random sampling and Tmax of the proposed method is smaller than Tmin of random sampling. The ratio of the latter for high time resolution waveform measurement when M=512 (which is equivalent to 2ps time resolution at the clock frequency of 1GHz) reaches approximately 15 times. We see that this proposed sampling system can record data with a time less than 1/10 of that of the random sampling system for a signal with fluctuations and less than 1/100 for a signal without fluctuations.

5. Future Works

1) We will soon complete the prototype system currently under development and use it to confirm that the waveform recording speed is improved by the proposed sampling method.

2) We have presented an algorithm for calculating an optimal clock period from several times of Trr measurement and their average for the repetitive input signals with periodic fluctuations. We will continue our study on improving the algorithm to maximize the waveform recording efficiency in measurement of input signals with fluctuations. Some of the results are described in [15].

6. Conclusion

We have proposed a new equivalent-time sampling for wideband high-speed waveform measurement which incorporates both the high waveform recording efficiency of coherent sampling and the pretrigger ability of random sampling. The numerical simulation results show that the proposed system can record data more than ten times faster than a conventional random sampling system for signals with fluctuations and more than one hundred times faster for signals without fluctuations, and that the system can be used to implement a high performance DSO.

Acknowledgment

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