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PAPER

High-Efficiency Charge-Pump Circuits with Large Current Output for Mobile Equipment Applications

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SUMMARY This paper presents improved versions of three-stage positive-output and two-stage negative-output Dickson charge-pump circuits which are intended to replace switching regulators in video-product CCD driver applications (where 12 V and −6.5 V are needed), and are designed and fabricated in a custom CMOS process. From a power supply V_{dd} of 4.0 to 5.5 V, the positive charge pump generates a positive output voltage of greater than $3.9V_{dd}$, while the negative charge pump generates a negative voltage of greater than $-1.9V_{dd}$, both with efficiencies of greater than 94% at 2 mA output currents.

key words: *charge-pump circuit, DC-DC converter, high-efficiency high-voltage generation*

1. Introduction

Recent video products such as digital video cameras, digital still cameras (DSC), and DSC phones incorporate charge coupled devices (CCDs) for video image acquisition; these require generation of high voltages such as +12 V (at output currents of several mA) and −6.5 V (at several mA) from a power supply of $V_{dd} = 5$ V. At present, switching regulators are widely used for such high voltage generation, because they can generate high voltages with high efficiency. However, switching regulators generate harmonic noise during switching, and they also require off-chip coils which are bulky and costly. Charge-pump circuits, on the other hand, generate little noise and do not require coils. However, conventional charge-pump circuits [1], [4], [5] suffer from relatively low efficiency at large output currents, which makes it difficult to use them in power supply circuits of mobile products. In this paper we propose new charge-pump circuit designs which have high efficiency at high output currents—for miniature, low-cost mobile equipment.

The proposed charge-pump circuits generate a voltage of $2V_{dd}$ internally, and use it as the gate-source voltage (V_{gs}) of all the charge transfer MOSFETs, to lower their impedance significantly. Also, we have designed appropriate clock timing for controlling the gate-source voltages (V_{gs}), and designed new level-shift circuits for the clock-timing implementation, in order to prevent reverse charge-transfer current. Using these techniques, we have succeeded in developing charge-pump circuits that realize both high output current and high efficiency. Measured results from a test element group (TEG) show that efficiency of our 3-stage positive-output charge-pump circuit (with output current, $I_{out} = 2$ mA and output voltage $V_{out} = 3.9\,V_{dd}$) is 95%, and that of our two-stage negative-output charge-pump circuit (with $I_{out} = 2$ mA and $V_{out} = -1.9\,V_{dd}$) is 94%.

2. Principles and Theory of Charge-Pump Circuits

Figure 1 shows a Dickson charge-pump circuit [1] that uses diodes as charge-transfer devices. We now analyze this circuit theoretically, paying attention to the relationship between output voltage (in terms of multiplication factor, number of times V_{dd}) and efficiency. Note that, in Fig. 1, CLK and CLKB have opposite phase, and we define the current that flows through the diodes from the input line to the output line as the charge-transfer current. When the output current (I_{out}) is constant in the steady state, the input current to the charge-pump circuit is equal to the total current provided from V_{in} and clock drivers. If charge and discharge currents associated with parasitic capacitance are ignored, these currents from V_{in} and clock drivers are expressed as follows [2]:

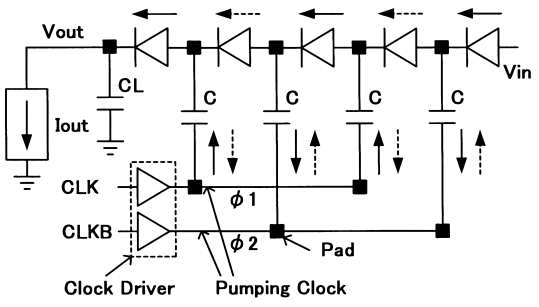

Fig. 1 A four-stage Dickson charge-pump circuit.

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① During the period when $\phi 1$ = High, $\phi 2$ = Low: An average current of $2I_{out}$ flows in the direction shown by the arrows with solid lines in Fig. 1.
② During the period when $\phi 1$ = Low, $\phi 2$ = High: An average current of $2I_{out}$ flows in the direction shown by the arrows with dashed lines in Fig. 1.

We see that average current during one clock cycle is I_{out} [2]. Note that the output voltage (V_{out}) of the charge-pump circuit in the steady state can be expressed as follows [1], [3]:

$$V_{out} = V_{in} - V_d + n(V'_\phi - V_l - V_d), \tag{1}$$

where V'_ϕ is the voltage amplitude at each pumping node associated with coupling capacitance of the clock signal, V_l is the voltage fluctuation caused by current I_{out} that flows through the diodes, and V_{in} is the input voltage to the circuit (that is specified as V_{dd} for positive boosting and specified as 0 V for negative boosting), V_d is voltage drop of a diode, and n is the number of charge pump stages. Also V_l and V'_ϕ are expressed as

$$V_l = \frac{2I_{out}T/2}{C + C_s} = \frac{I_{out}}{f(C + C_s)}, \tag{2}$$

$$V'_\phi = V_\phi \frac{C}{C + C_s}, \tag{3}$$

where C is clock coupling capacitor, C_s is parasitic capacitance at each node, and V_ϕ, f and T are respectively the amplitude, frequency and period of the pumping clock.

Neglecting parasitic capacitance charge and discharge currents from clock drivers, and assuming that I_{out} flows at the output, then the efficiency of the charge-pump circuit is given by:

$$\eta = \frac{V_{out}I_{out}}{(n+1)V_{dd}I_{out}} = \frac{V_{out}}{(n+1)V_{dd}}. \tag{4}$$

Here note that V_{in}=V_{dd}.

When a charge-pump circuit has output load current of several mA, it requires capacitors C of 0.1 μF or larger—according to Eq. (2)—and these are too large to be incorporated inside an LSI package; such capacitors must be attached externally, and both terminals of the capacitor have to be connected to pads of the LSI chip. Since parasitic capacitance of several tens of pF associated with the pads cannot be ignored, the efficiency of the charge pump circuit is degraded significantly. We denote the parasitic capacitance of the pad as C_p, and C_p must be added to C_s in Eqs. (2) and (3); the charge and discharge current that flows from the clock driver to each of the pump stages is given by:

$$I_{fcv} = fC_pV_\phi + f(C_s + C_p)V'_\phi. \tag{5}$$

Hence the total current that flows in each of the pump stages is given by:

$$I_{dv} = I_{out} + I_{fcv}. \tag{6}$$

Thus, when the charge and discharge currents associated with parasitic capacitance are taken into consideration, the efficiency is expressed as:

$$\eta = \frac{V_{out}I_{out}}{nV_{dd}I_{dv} + V_{dd}I_{out}}. \tag{7}$$

Note that when we control the pumping clock frequency f to keep the value of V'_{out} constant, according to Eq. (2), the efficiency is expressed as:

$$\eta = \frac{V'_{out}I_{out}}{nV_{dd}I_{dv} + V_{dd}I_{out}}. \tag{8}$$

Also note that when we add an regulator (such as an operational amplifier or a Zener diode) to the output node to keep the value of V'_{out} constant, the efficiency is given by:

$$\eta' = \frac{V'_{out}I_{out}}{nV_{dd}(I_{dv} + I_{rg}) + V_{dd}(I_{out} + I_{rg})}. \tag{9}$$

Here, I_{rg} is the current that flows in the regulator in parallel with I_{out}. Note that, in this case, Eq. (2) reduces to:

$$V_l = \frac{I_{out} + I_{rg}}{f(C + C_s + C_p)}. \tag{10}$$

When an operational amplifier is used as a series regulator, the value of I_{rg} can be made extremely small. On the other hand, when a Zener diode is used as a parallel regulator to regulate V_{out}, current I_{rg} varies so as to maintain V_l in Eq. (10) constant, and note that I_{rg} flows from V_{in} and all the clock drivers. This usually requires that $I_{rg} > I_{out}$, and hence the efficiency is quite low. Figure 2 shows the relationship between pumping clock frequency and charge transfer current. In most charge pump circuits with small output current, as represented by type A [3], the charge transfer current falls to zero during 1/2 cycle of the clock. On the other hand, for charge pump circuits with large output current, as represented by type B [3], the load transfer current does not always fall to zero in 1/2 cycle of the clock. Thus, letting the power supply voltage of the clock driver be V_{dd}, and the charge transfer current at the end of 1/2

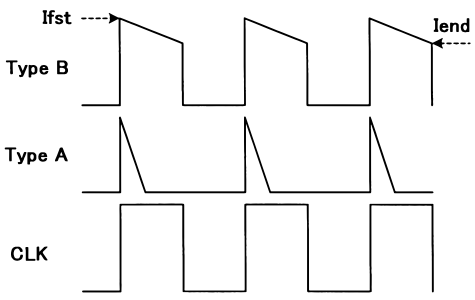

Fig. 2 Type of charge transfer current.

cycle of the clock be I_{end}, V_ϕ is given by

$$V_\phi = V_{dd} - \Delta V_{ds(P)} - \Delta V_{ds(N)}. \quad (11)$$

Here, $\Delta V_{ds(P)}$ and $\Delta V_{ds(N)}$ are drain-source voltages of the clock driver p-channel and n-channel MOSFETs respectively, in a static CMOS inverter configuration, when current I_{end} is flowing.

One advantage of the Dickson charge-pump circuit is its wide operating frequency range. Equation (2) shows that, for given V_l, we can decrease the value of capacitors (C) (smaller capacitors make for smaller mobile equipment) by increasing the operating frequency (f). However, in this case, we have to allow for charge and discharge currents associated with parasitic capacitance in Eq. (5), because as frequency (f) increases, the current I_{fcv} in Eq. (5) increases, which degrades the efficiency (see Eq. (7)).

3. Comparison between Measured and Simulated Output Voltages

In this section we describe how we validated our output voltage calculation method, based on Eqs. (1) and (11), by measuring actual values from a prototype three-stage positive-output charge-pump circuit consisting of discrete circuit elements on a board. Schottky diodes were used as charge transfer elements, due to their small V_d values, and test conditions were as shown below: $V_{dd} = 4.0$ to $5.5\,\mathrm{V}$, $I_{out} = 8\,\mathrm{mA}$, $f = 500\,\mathrm{kHz}$, $V_d = 0.2\,\mathrm{V}$ and $\Delta V_{ds(P)} = \Delta V_{ds(N)} = 0.28\,\mathrm{V}$ (V_d values measured), $C = 0.1\,\mu\mathrm{F}$.

As Fig. 3 shows, there are large discrepancies between measured and simulated results if we neglect the effect of $\Delta V_{ds(P)}$ and $\Delta V_{ds(N)}$. On the other hand, when we assume $\Delta V_{ds(P)} = \Delta V_{ds(N)} = 0.28\,\mathrm{V}$, we obtain good agreement between measured and simulated results. Results show that introducing Eq. (11) leads to highly accurate simulations. However, there are still small discrepancies between measured and calculated results, and we have found that they are caused by clock overshoot and ringing, since the circuit is composed of discrete elements, and the parasitic inductance associated with the clock circuits causes clock signal overshoot and ringing.

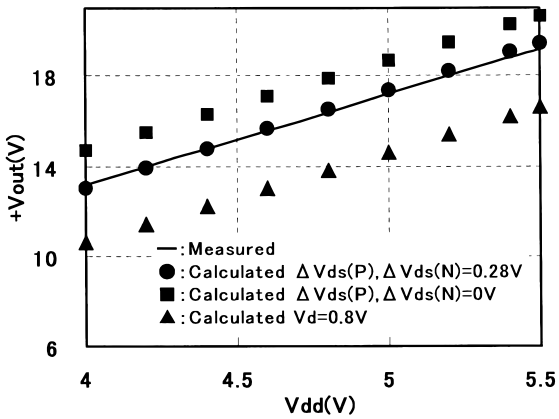

Fig. 3 Comparison between measured and calculated results for a three-stage positive-voltage charge-pump circuit implemented with discrete circuits.

Further, we calculated the multiplier voltages when $V_d = 0.8\,\mathrm{V}$ (i.e., conventional diodes are used as charge transfer elements) and plotted the results with ▲. Results show that smaller values of V_d, $\Delta V_{ds(P)}$ and $\Delta V_{ds(N)}$ result in higher output voltages in the charge pump circuit. Also note that the following conditions have to be satisfied in order to increase the efficiency in Eq. (7):

① $V_l \approx 0$, ② $V_d \approx 0$, ③ $\Delta V_{ds(P)} \approx 0$,

④ $\Delta V_{ds(N)} \approx 0$, ⑤ $I_{fcv} \approx 0$

When the charge transfer elements are MOSFETs rather than diodes, we also have to validate the assumption that:

⑥ Reverse charge transfer current=0

Reverse charge transfer current (called "reverse current" below) is the current that flows in the opposite direction to the charge transfer flow (see Fig. 7).

We have taken the following precautions to satisfy the above conditions of ① to ⑥:

- Choose the most appropriate values for C and f to satisfy ① and ⑤.
- Use MOSFETs as charge transfer elements, and decrease their impedance sufficiently to satisfy ②.
- Decrease clock driver impedance, so as to satisfy ③ and ④.
- For charge transfer MOSFETs, don't overlap gate-control and pumping clocks, so as to satisfy ⑥.

4. Limitations of Conventional Charge-Pump Circuits in Mobile Equipment Applications

In this section we consider limitations of conventional charge-pump circuits in power supply circuits of mobile equipment.

In [1], Dickson proposed a charge-pump circuit using so-called "diode-connected" MOSFETs, with their gates and drains shorted together, in place of diodes. When the charge transfer MOSFETs are ON, their gate-source voltage V_{gs} (which is equal to their drain-source voltage) is greater than their threshold voltage V_{th}, which significantly degrades efficiency. Note that while Fig. 3 shows that quite a high efficiency charge-pump circuit can be made with Schottky diodes—because their voltage drop is relatively small—they cannot be fabricated in a standard CMOS LSI chip; if they are externally connected, the charge-pump circuit does not have any commercial value at all, due to price and size considerations. We decided to realize high efficiency charge-pump circuits by separating

the gate and drain nodes of the charge transfer MOSFET and making their V_{gs} higher than V_{dd} to decrease their impedance in accordance with the value of I_{out}. This idea has already been applied in several cases [4], [5], however the application was flash memories, and in general, requirements for flash memory charge-pump circuits using a p-substrate are as follows:

① Output load current is small (approx. 100 μA).
② Change transfer MOSFETs are n-channel.
③ Capacitors are incorporated inside an LSI.
④ High output voltage as well as small chip area are most important. However, efficiency is not a high priority. (Note that in order to attain high efficiency, the value of C must be large, in accordance with Eq. (2), which would result in large chip area.)

The features of the charge-pump circuit shown in Fig. 4 of Ref. [4] are as follows:

① The body of the charge transfer MOSFET is grounded. Hence the charge transfer MOSFETs close to the output node may suffer from gate-substrate breakdown problems. However, since output current is small (i.e., impedance of the charge transfer MOSFET does not need to be really small) we can make the gate oxide (T_{ox}) of the charge transfer MOSFET thicker, to avoid breakdown voltage problems.
② The multiplier voltage from the following stage, $2V_{dd}$, is used as the gate-source voltage (V_{gs}) of each n-channel charge-transfer MOSFET, which contributes to high efficiency.
③ The gate and drain of the final-stage charge transfer MOSFET (MDO) are shorted. However since the circuit does not need high efficiency, the small voltage loss does not cause problems.
④ A capacitor C5 is added for V_{gs} of the charge transfer MOSFET (MS4). However since C5 can be fabricated on chip, its addition does not cause a problem.
⑤ The circuit does not have any measures to prevent reverse current. However, a small reverse current is not a big problem, because efficiency is not so important in this application.

In summary, the charge-pump circuit in [4] has superior characteristics for flash memory applications. However, it is not suitable for mobile equipment applications which require large output current, high efficiency, and few externally-connected components, and items ②,③,④, and ⑤ above represent serious drawbacks of conventional charge-pump circuits in such applications.

Also in [5], [8], the charge transfer MOSFET gate boosting method is used, and this is acceptable for small-output-current charge-pump circuits. However, for large-output-current applications, charge transfer MOSFETs require large W/L to realize low impedance, which makes the MOSFET gate capacitance extremely large, so the capacitors for gate boosting have to be very large which degrades efficiency [8] and also may not be able to be fabricated on chip. Hence this method is not applicable for large-output-current charge-pump circuits.

5. Proposed Charge-Pump Circuit with Positive Output Voltage and Large Current Output

In this section we propose a high efficiency charge-pump circuit, with positive output voltage, that can supply several mA output current (hereafter we call it "a positive charge-pump circuit"). Note that our proposed circuit does not have the problems listed in ②,③,④, and ⑤ of the previous section. Figure 4 shows our proposed three-stage positive-voltage charge-pump circuit which provides output voltage V_{out} of 12 V with target output current I_{out} of 2 mA for an input voltage V_{dd} from 4.0 to 5.5 V, and this circuit has the following features:

① n-channel MOSFETs are used as charge transfer devices in the first two stages, while p-channel MOSFETs are used in the second two stages.
② The drain and body of the charge transfer MOSFET are shorted to make their electric potentials equal for the following purposes: first, body effect is avoided. Second, we can fabricate a thin gate oxide (T_{ox}) layer in the charge transfer MOSFET to achieve large transconductance, because the gate-body voltage (V_{gb}) is reduced, and hence gate-substrate breakdown problems are alleviated. Note in Fig. 4 that when the charge transfer MOSFET is ON, its higher-voltage node is defined as drain (D) for n-channel, and source (S) for p-channel.
③ When the charge transfer MOSFET is ON, $2V_{dd}$ is provided to $|V_{gs}|$ through a level-shift circuit connected to a boosted-voltage node in the circuit.
④ The input clock timing of the level shift circuit is controlled so as to reduce reverse current to zero.
⑤ The design minimizes the number of capacitors.
⑥ Design parameters of the charge transfer MOSFETs are as follows:
$W/L = 4000\,\mu\text{m}/1.8\,\mu\text{m}$ (p-channel), $W/L =$

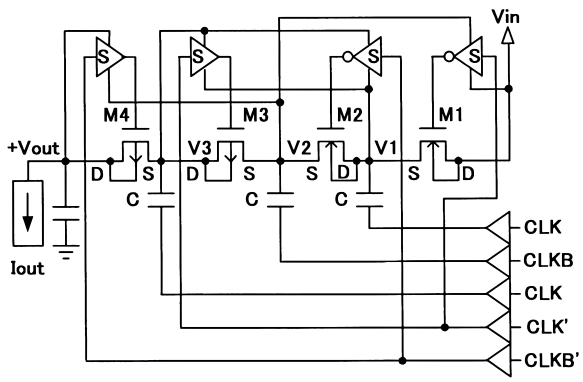

Fig. 4 Proposed three-stage positive charge-pump circuit.

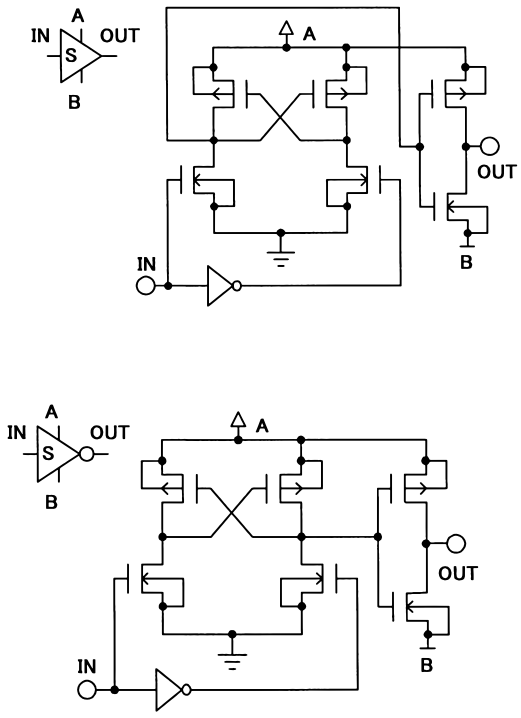

Fig. 5 New level shift circuits.

$1000\,\mu$m/$1.8\,\mu$m (n-channel), where W is channel width and L is channel length.

⑦ Design parameters of the clock driver MOSFETs for each pump are as follows:
$W/L = 6000\,\mu$m/$1.8\,\mu$m (p-channel),
$W/L = 2000\,\mu$m/$1.8\,\mu$m (n-channel)

⑧ Other design parameters are as follows, for I_{out}=2 mA:
– V_d =0.04 V
– $\Delta V_{ds(P)} = \Delta V_{ds(N)} = 0.04$ V

We have designed the value of $|V_{ds}|$ (when the charge transfer MOSFET is ON) to be lower than the built-in voltage V_{bi} of the parasitic diode, to avoid bipolar action in the steady state. Figure 5 shows our newly-designed level shift circuits composed of high-voltage MOSFETs [6], [7], and their outputs are provided from node A and also node B, where the voltage at node B is between that of node A and ground. Note that the output of a conventional circuit is from between node A and ground.

The value of gate-source voltage V_{gs} of the charge transfer MOSFET (when it is ON) is given by
– V_{gs}(M1) = V_2 (High) − V_{dd}
– V_{gs}(M2) = V_3(High) − V_1(Low)
– V_{gs}(M3) = V_1 (Low) − V_3(High)
– V_{gs}(M4) = V_2 (Low) − V_{out}

We see that for each of the charge transfer MOSFETs (M1, M2, M3 and M4), the value of $|V_{gs}|(= |V_{gb}|)$ is approximately equal to $2V_{dd}$ when it is ON, and hence its gate-oxide layer thickness (T_{ox}) can be made very thin, provided that gate-bulk breakdown voltage is

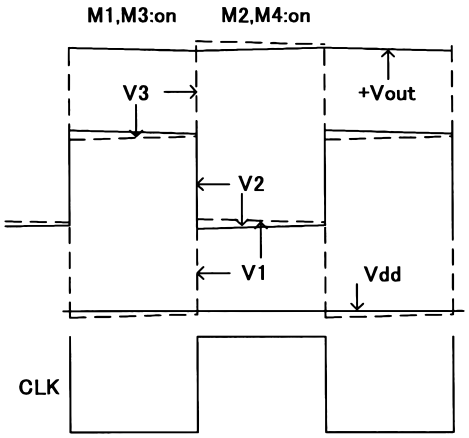

Fig. 6 Waveform at each pumping node in the three-stage positive-output charge-pump circuit of Fig. 4.

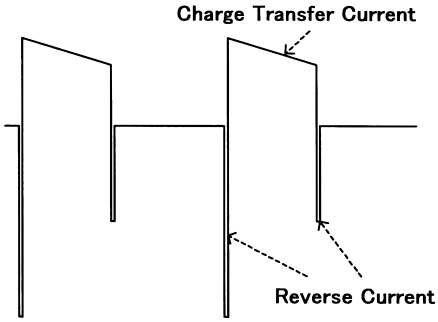

Fig. 7 Charge transfer current and reverse current.

larger than $2V_{dd}$; this helps reduce the impedance of the charge transfer MOSFET significantly. In the circuit of Fig. 4, the number of pump stages can be increased according to the specification, and note that in such a case p-channel MOSFETs should be used as charge transfer MOSFETs in the last two stages while n-channel MOSFETs should be used in the other stages.

6. Clock Timing Design

This section describes the clock timing used to prevent reverse current. First note that the operation of the charge transfer MOSFET in Fig. 4 is not equivalent to that of a diode, and Fig. 6 shows voltage waveforms at each pumping node in the proposed positive-voltage charge-pump circuit. For example, if M2 turns ON (even very shortly) when $V_2 - V_1 \approx 2V_{dd}$, reverse current flows from V_2 to V_1 as shown in Fig. 7, and our SPICE simulation showed that the reverse current can reach several hundred mA if we do not take any precautions to prevent it. In such a case, the efficiency of the charge pump is degraded by 3 to 10% (depending on the operating frequency (f)) even though the charge transfer current compensates for the charge returned from the output to the input by reverse current, and the circuit works as a charge-pump circuit. We

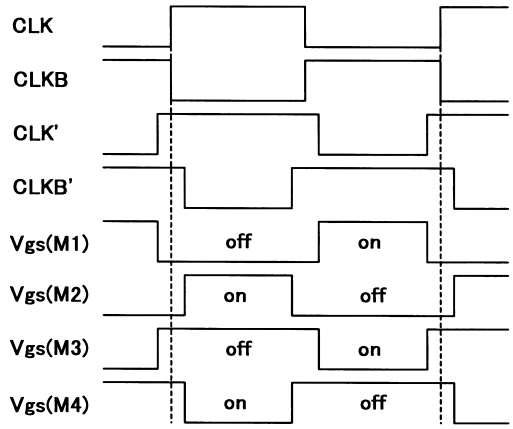

Fig. 8 V_{gs} timing of each charge transfer MOSFET in the positive charge-pump circuit.

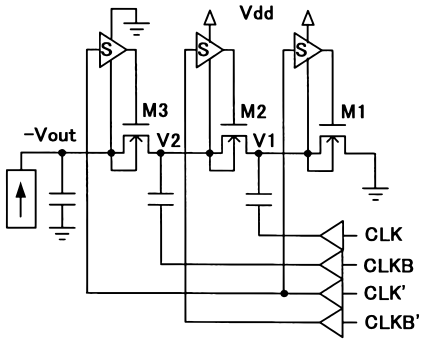

Fig. 9 Proposed two-stage negative voltage charge-pump circuit.

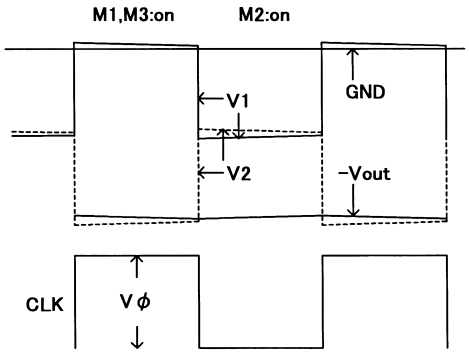

Fig. 10 Voltage waveforms at each pumping node in a two-stage negative-output charge-pump circuit.

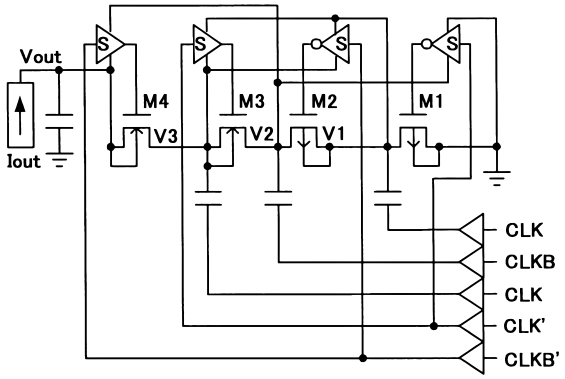

Fig. 11 Proposed three-stage negative charge-pump circuit.

propose the clock timing shown in Fig. 8, where all the charge transfer MOSFETs are OFF during the state transition of CLK and CLKB in order to prevent reverse current. We have used these level-shift circuits (Fig. 5) to implement the timing design (Fig. 8); we can control timing of V_{gs} of the charge transfer MOSFETs by controlling the input clock timing of the level-shift circuits. On the other hand, in the conventional charge-transfer MOSFET gate boosting method [5], the gates of charge-transfer MOSFETs are directly connected to internal boosted voltage nodes, and hence arbitrary V_{gs} timing control is difficult there.

7. Proposed Charge-Pump Circuit with Negative Output Voltage and Large Current Output

In this section we propose a high-efficiency charge pump circuit with negative output voltage and large current output (hereafter we call it "a negative charge-pump circuit") based on the idea of the positive charge pump in previous sections. Figure 9 shows our proposed two-stage negative charge-pump circuit for providing $V_{out} = -6.5\,\mathrm{V}$, $I_{out} = 2\,\mathrm{mA}$ from a power supply V_{dd} of from 4.0 to 5.5 V, and it has the following features:

① Charge transfer devices, M1, M2 and M3 are n-channel MOSFETs.
② The gate-source voltage of M1 is V_{dd} when it is ON.
③ The gate-source voltage of M2 and M3 are $2V_{dd}$ when they are ON.
④ External voltages are used to provide the gate-source voltages of the charge transfer MOSFETs (when they are ON). This is to compare the minimum operating supply voltages (due to their self-starting function) between the negative charge pump circuit (where external voltages are used for V_{gs} of the charge transfer MOSFETs) and the positive charge pump circuit (where internal voltages are used).
⑤ Design parameters of the charge transfer MOSFETs are $W/L = 1000\,\mu\mathrm{m}/1.8\,\mu\mathrm{m}$.
⑥ Design parameters of clock drivers for each pump stage are $W/L = 6000\,\mu\mathrm{m}/1.8\,\mu\mathrm{m}$ (p-channel) and $W/L = 2000\,\mu\mathrm{m}/1.8\,\mu\mathrm{m}$ (n-channel).
⑦ Other design parameters are as follows, with target output current I_{out}=2 mA:
– $V_d = 0.08\,\mathrm{V}$ for M1 and 0.04 V for M2 and M3.
– $\Delta V_{ds(P)} = \Delta V_{ds(N)} = 0.04\,\mathrm{V}$.

Figure 10 shows voltage waveforms at each pumping node of the two-stage negative-output charge-pump circuit. Figure 11 shows a three-stage negative-output charge-pump circuit, and we can increase the number of

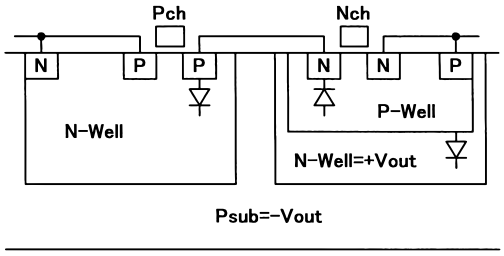

Fig. 12 Conceptual schematic of CMOS process for proposed charge-pump circuits.

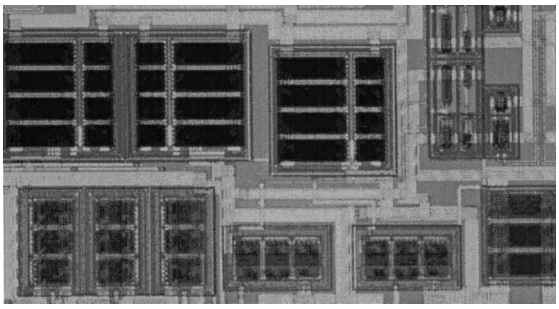

Fig. 13 Photograph of a three-stage positive-output charge-pump circuit in TEG (3.99 mm × 4.35 mm).

the pump stages according to the specification, however note that in such cases p-channel MOSFETs should be used as charge transfer MOSFETs in the first two stages, while n-channel MOSFETs should be used in the other stages.

8. CMOS Process for Charge-Pump Circuit

Figure 12 shows a conceptual schematic of the CMOS process to realize our proposed positive and negative charge-pump circuits in a one-chip LSI circuit, and it has the following characteristics:

① Triple-well structure is adopted, to integrate positive and negative charge-pump circuits on one chip.
② 30 V high-voltage MOSFETs and 10 V LDD MOSFETs exist together on one chip.
③ 30 V high-voltage MOSFETs with $T_{ox} = 910$ Å and $L = 5.0\,\mu$m are used for level shift circuits.
④ 10 V LDD MOSFETs with $T_{ox} = 440$ Å, $L = 1.8\,\mu$m are used for clock drivers and charge transfer MOSFETs.
⑤ The forward-current gain β of parasitic bipolar transistors is designed to be a minimum, in order to reduce the effects of bipolar action during start-up.

Figure 13 shows a photograph of the three-stage positive-output charge-pump circuit in TEG (whose purpose is to establish fundamental technology for power supply circuits, and the charge-pump circuit is one of them.)

9. Start-up of Positive-Output Charge-Pump Circuit

In this section we show that the proposed positive-output charge-pump circuit has a self-starting function, and hence there is no need to apply initial node voltages from outside. When we start up the circuit in Fig. 4, V_{dd} is applied and voltages are transmitted to all nodes through parasitic diodes shown in Fig. 12. Suppose that V_{dd} is 5 V, then the initial voltages (i.e., before clocks have been applied) at pumping nodes are given as follows:

– $V_1 = 4.3$ V
– $V_2 = 3.6$ V
– $V_3 = 2.9$ V
– $V_{out} = 4.3$ V.

Note that these values are confirmed by our measurements.

The self-starting mechanism of the circuit is as follows:

① Since $V_2 > V_{tn}$ (where V_{tn} is the threshold voltage of n-channel MOSFET) as shown above, M1 operates as a MOSFET from start-up.
② Under the above initial conditions, let CLK be low and CLKB be high, then the gate voltage of M1 becomes $V_2 = V_{dd} + 3.6$ V and V_1 is equal to V_{dd}.
③ Next let CLK be low and CLKB be high, then V_1 is boosted close to $2V_{dd}$.
④ M2 turns ON when its $V_{gs} = V_3(\text{high}) - V_2(\text{Low})$ and then boosts the voltage of V_2.
⑤ Since $V_1 - V_2 > V_{bi}$ at the initial stage of the start-up, the boosted voltage of V_1 is transmitted to V_2 through parasitic diodes, too. At this time, bipolar action takes place temporarily.
⑥ Similarly M3 turns ON when $V_{gs} = V_1(\text{Low}) - V_2(\text{High})$, and the boosted voltage of V_2 is transmitted to V_3 through parasitic diodes because $V_2 - V_3 > V_{bi}$.

As explained above, the initial condition of $V_2 > V_{tn}$ enables self-starting of the circuit. Our measured results of TEG showed that the circuits in Fig. 4 and Fig. 9 start-up satisfactory with a supply voltage range of $V_{dd} = 4.0$ V to 5.5 V, and the minimum operating supply voltages for positive and negative charge pump circuits are 1.8 V and 1.9 V at $I_{out} = 2$ mA, respectively. We see that there is no problem using the internal node voltages to provide V_{gs} of charge transfer MOSFETs because the minimum operating supply voltages are almost the same for positive and negative charge pump circuits.

10. Measured Results for Proposed Charge-Pump Circuit

This section describes measured results for output voltage and efficiency of the charge-pump circuits in Figs. 4

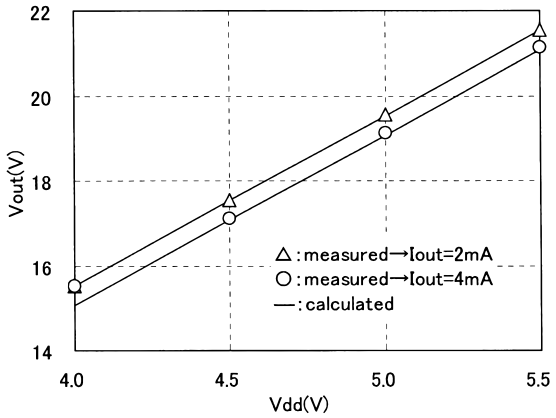

Fig. 14 Boosted voltage of the positive three-stage charge-pump circuit.

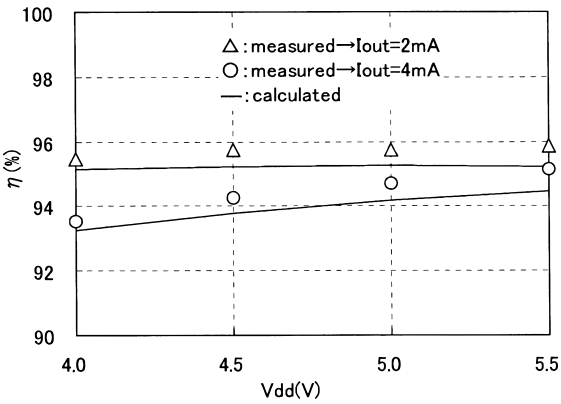

Fig. 15 Efficiency of the positive-output three-stage charge-pump circuit.

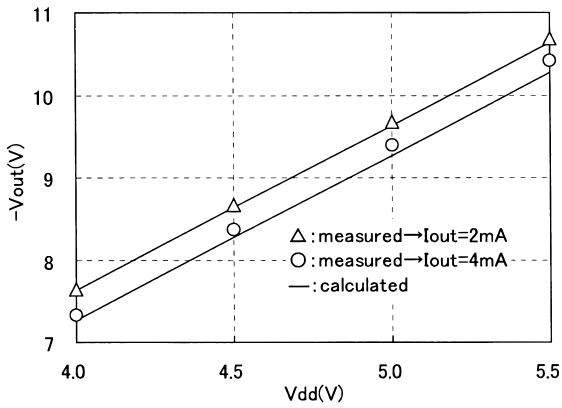

Fig. 16 Boosted voltage of the negative two-stage charge-pump circuit.

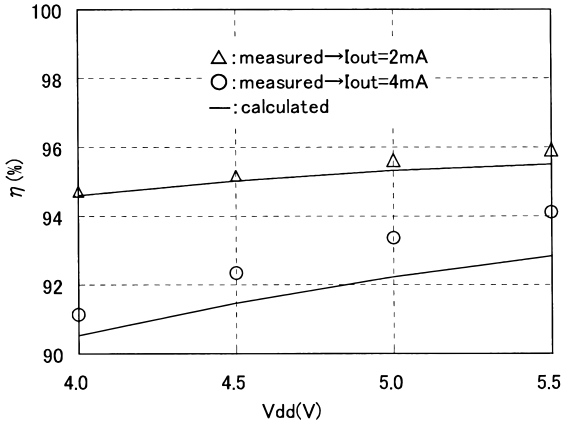

Fig. 17 Efficiency of the negative-output two-stage charge-pump circuit.

and 9, and compares them with theoretical calculations under the following conditions:
– $C = 0.47\,\mu$F
– $f = 200\,$kHz.
Also we use the following to obtain the circuit efficiency:

$$\eta = \frac{V_{out} I_{out}}{V_{dd} I_{drv} + V_{in} I_{in}} \tag{12}$$

Here, I_{drv} is the current provided from the clock drivers for CLK and CLKB, while I_{in} is the current provided from V_{in}.

Figure 14 shows the measured and theoretical results of the positive-output charge-pump circuit. The theoretical calculation is performed based on Eq. (1), taking into consideration Eq. (11). Boosted voltage is increased by the reduction amount of V_d, $\Delta V_{ds(P)}$ and $\Delta V_{ds(N)}$, compared to the results in Fig. 3. Figure 15 shows the measured and theoretical efficiency results, and the theoretical calculation was based on Eq. (7) and measured data of V_{out}, where the estimated value of 10 pF is used as the parasitic capacitance value C_p of a pad. Figure 15 shows that this circuit displays high efficiency. Figure 16 shows the measured and theoretical results of the negative-voltage charge-pump circuit, while Fig. 17 shows its efficiency. We consider that the reason that the efficiency of the negative charge pump is a little smaller than that of the positive charge pump is that V_{gs} of the charge transfer MOSFET M1 (when it is ON) is V_{dd} for the negative charge pump circuit while it is $2V_{dd}$ for the positive charge pump circuit. Also we see that the effect of final-stage losses on the efficiency is larger when the number of the stages is smaller.

11. Improvement of Charge-Pump's Efficiency after Its Output Voltage Regulation

The large difference between switching regulator and charge-pump lies in their efficiency after their output voltage is regulated. The efficiency of switching regulator remains almost the same even when the clock frequency or duty is changed to regulate its output voltage. The efficiency of charge-pump, on the other hand, goes down according to the regulated output voltage. The following Eq. (13) shows the efficiency when current loss is completely ignored in Eq. (9):

$$\eta = \frac{V'_{out}}{(n+1)V_{dd}} \tag{13}$$

Also the regulated voltage (V_{reg}) is given by

$$V_{reg} = (n+1)V_{dd} - V'_{out} \quad (14)$$

In conventional charge-pump circuit, n in above equations is an integer. In this case, the efficiency becomes the lowest when n is 1 and V_{reg} is large; for example, let us consider the case that $V'_{out} = 6.5\,\mathrm{V}$ is obtained from $V_{dd} = 5\,\mathrm{V}$. In this case $n = 1$ and according to the simple calculation, the maximum obtainable efficiency is 65% even when the voltage and current losses are ignored. If some reasonable losses are taken into account, the efficiency will be lower to approximately 60%.

To overcome this problem, we proposed '$0.5V_{dd}$ pumping up method' in [9] and verified its effectiveness through an experiment by the test element group (TEG). The measured efficiency of the charge-pump using this method showed good agreement with our theoretical results in [9]. Using our method, n in the Eq. (13) can be 0.5. When n is 0.5, the efficiency mentioned above will be 86% for ideal case (without related losses), and 81% for some practical cases (with some reasonable losses); of course, these efficiency values can be varied according to V_{dd} fluctuation. We estimate that the efficiency of the charge-pump is only 0% to 10% lower than that of the switching regulator even when V_{dd} fluctuation is taken into account.

12. Conclusions

In this paper we have proposed improved versions of the Dickson charge pump circuit to provide large current output with high efficiency, for our target application of power supply circuitry in mobile equipment; the advantages of our proposed charge pump circuits over conventional power supply circuitry (such as switching regulators) for mobile equipment are that (for small size and low cost) they require neither coils nor large capacitors, and generate little noise. The conventional Dickson charge-pump circuit is difficult to apply directly to mobile equipment applications where both large output current (several mA) and high efficiency are required. We have improved the charge-pump circuit design to make it suitable for such applications. In our circuit, $2\,V_{dd}$ is provided to the gate-source voltage (V_{gs}) of each charge-transfer MOSFET, utilizing an internal node voltage of the charge-pump circuit, to lower its impedance. Also, we have designed clock timing to control V_{gs}, and designed level shift circuits to prevent reverse flow of charge transfer current. These techniques contribute to the power efficiency of the circuit. Measured results of TEG showed that the efficiency of our positive and negative charge pump-circuits is as high as their theoretical value of over 94% with 2 mA output current. Commercialization of our proposed charge-pump circuits has already started.

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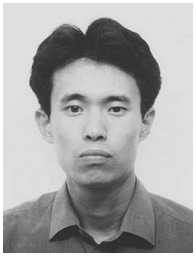

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