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PAPER

Analysis of CMOS ADC Nonlinear Input Capacitance

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SUMMARY This paper describes the nonlinear behavior of CMOS ADC input capacitance. Our SPICE simulation, based on the BSIM3v3 model, shows that the input capacitance of a typical CMOS flash-type ADC (with a single-ended NMOS differential pair preamplifier as the input stage) decreases as its input voltage increases; this is the opposite of what we would expect if we considered only MOSFET gate capacitance nonlinearity. We have found that this can be explained by the nonlinearity of the total effective input capacitance of each differential amplifier stage, taking into account not only MOSFET capacitance but also the fact that the contributions of the gate-source and gate-drain capacitances to the input capacitance of the differential pair change according to its input voltages (an ADC input voltage and a reference voltage). We also discuss design methods to reduce the value of the CMOS ADC effective input capacitance.

key words: *ADC, CMOS, input capacitance, nonlinearity, BSIM3*

1. Introduction

It is well-known [1], [2] that the input capacitance of a CMOS Analog-to-Digital Converter (ADC) is nonlinear, and the nonlinearity of the CMOS ADC is one of the important issues when designing high-speed, high-precision CMOS ADCs. For example, their step responses are different for rising and falling step inputs, due to nonlinear input capacitance [3]. However, to our knowledge, there are no references which discuss how nonlinear they are, and why they are.

This paper analyzes the nonlinear behavior of CMOS ADC input capacitance using SPICE simulation based on the BSIM3v3 model with the aim of improving the AC performance of our CMOS ADC designs [4]. There are many architectures and circuit topologies for CMOS ADCs [1], [2], and in this paper we will focus on a flash type with single-ended input stages, and with the reference voltage provided to one of the inputs of each NMOS differential pair (preamplifier). Our SPICE simulation results show that the input capacitance decreases as the ADC input voltage increases, and we have found that this cannot be explained by MOS gate-capacitance nonlinearity alone, but we have to consider the total effective input capacitance of a MOS differential amplifier. We will also discuss design methods for reducing the value of the input capacitance.

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2. Analysis of Input Capacitance Nonlinear Behavior of CMOS ADC

This section describes why the input capacitance of a CMOS ADC decreases as its input level increases. (The definition of the input capacitance for a general circuit is given in Appendix.) First, nonlinearity of the MOS gate-capacitance is described, and second, the input capacitance nonlinearity of the differential pairs with resistive load is clarified. Finally the nonlinearity of the CMOS ADC input capacitance is discussed.

2.1 Nonlinearity Analysis of MOS Gate Capacitance

In this subsection, we will obtain NMOS gate-capacitance characteristics with respect to gate-source voltage V_{GS} and drain-source voltage V_{DS} using SPICE simulation based on BSIM3v3 model [5]. Figure 1 shows the circuit configuration with AC input voltage V_{ac} (biased at the voltage of V_{GS}) fed to an NMOS gate through a resistor R_{on} of 1 MΩ which is intentionally added to aid to determining the value of C_{gate}. Note that the drain of the NMOS FET is biased to a voltage V_{DS}. As a first-order approximation, we can assume

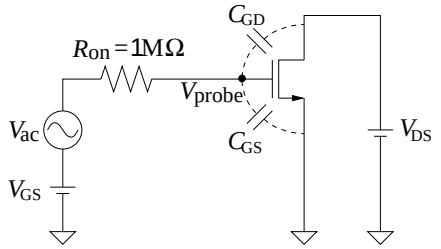

Fig. 1 Circuit configuration to obtain the gate capacitance value of an NMOS (biased at the voltages of V_{DS} and V_{GS}) by SPICE simulation.

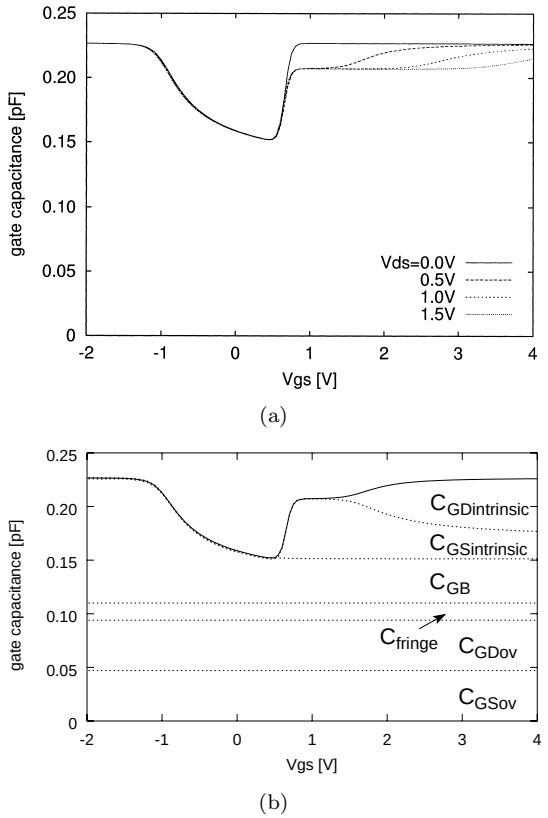

Fig. 2 (a) Characteristics of the gate capacitance versus the gate-source voltage ($V_{\rm GS}$) as a function of the drain-source voltage ($V_{\rm DS}$) obtained from SPICE simulation of the circuit in Fig. 1. (b) Gate capacitance components for $V_{\rm DS} = 0.5\,{\rm V}$ obtained from SPICE simulation. Here $C_{\rm fringe} = C_{\rm GDfr} + C_{\rm GSfr}$.

that, for large values of $R_{\rm on}$, $R_{\rm on}$ and $C_{\rm gate}$ are a first-order system with a time constant of $R_{\rm on}C_{\rm gate}$. From SPICE AC analysis, we can obtain the bandwidth $f_{\rm BW}$ of $V_{\rm out}$ with respect to $V_{\rm ac}$ from the gain characteristics. ($f_{\rm BW}$ is the frequency where gain decreases by 3 dB.) Thus we can obtain the value of $C_{\rm gate}$ for given $V_{\rm GS}$ and $V_{\rm DS}$ as follows:

$$C_{\rm gate} = 1/(2\pi f_{\rm BW} R_{\rm on}).$$

Figure 2 shows the characteristics, obtained from SPICE simulation, of the input capacitance ($C_{\rm gate}$) versus the gate-source voltage ($V_{\rm GS}$) for different drain-source voltages ($V_{\rm DS}$).

Next we will try to interpret the results in Fig. 2. Note that the MOS gate capacitance is given by

$$C_{\rm gate} = C_{\rm GD} + C_{\rm GS} + C_{\rm GB}.$$

Here $C_{\rm GD}$ is the gate-drain capacitance, $C_{\rm GS}$ is the gate-source capacitance and $C_{\rm GB}$ is the gate-substrate capacitance, and their capacitance values are varied according to the MOS operating range (i.e., they depends on $V_{\rm DS}$ and $V_{\rm GS}$). According to the Meyer MOS capacitance model [5]–[7], their values can be approximated as follows:

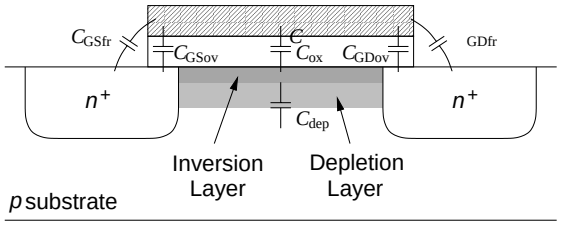

Fig. 3 Explanation of gate-oxide capacitance ($C_{\rm ox}$), depletion capacitance ($C_{\rm dep}$), gate-drain and gate-source overlap capacitances ($C_{\rm GDov}$, $C_{\rm GSov}$), and their fringe capacitances ($C_{\rm GDfr}$, $C_{\rm GSfr}$).

A. Accumulation Region ($V_{\rm GS} \ll 0$):

$$C_{\rm GB} = WLC_{\rm ox},$$
$$C_{\rm GD} = WC_{\rm GDov} + WC_{\rm GDfr},$$
$$C_{\rm GS} = WC_{\rm GSov} + WC_{\rm GSfr}.$$

Here W is the gate width, L is the gate length, $C_{\rm ox} = \varepsilon_{\rm ox}/t_{\rm ox}$ ($t_{\rm ox}$ is the gate-oxide thickness and $\varepsilon_{\rm ox}$ is the permittivity of the gate-oxide). Also $C_{\rm GDov}$ and $C_{\rm GDfr}$ are the gate-drain overlap and fringe capacitances respectively, and $C_{\rm GSov}$ and $C_{\rm GSfr}$ are the gate-source overlap and fringe capacitances respectively; these are illustrated in Fig. 3. The gate-drain and gate-source overlap capacitances are specified by *CGDO* and *GGSO* respectively, and the total gate-drain and gate-source fringe capacitance ($C_{\rm GDfr} + C_{\rm GSfr}$) is specified by C_F in BSIM3 model parameters [5]. Then the total gate capacitance is given by

$$C_{\rm gate} = WLC_{\rm ox} + WC_{\rm ov} \tag{1}$$

where $C_{\rm ov}$ is defined as

$$C_{\rm ov} = C_{\rm GDov} + C_{\rm GDfr} + C_{\rm GSov} + C_{\rm GSfr}.$$

B. Depletion Region ($0 \approx V_{\rm GS} < V_{\rm th}$):
In this operating region, the depletion layer is formed under the gate, and its capacitance ($C_{\rm dep}$) and the gate-oxide capacitance ($WLC_{\rm ox}$) are connected in series (Fig. 3). Hence the total gate capacitance is smaller than that in the accumulation region, and it is given by

$$C_{\rm gate} = \frac{1}{1/(WLC_{\rm ox}) + 1/C_{\rm dep}} + WC_{\rm ov} \tag{2}$$

C. Triode Region ($V_{\rm th} < V_{\rm GS}$, $0 < V_{\rm DS} < V_{\rm GS} - V_{\rm th}$):

$$C_{\rm GD} = (1/2)WLC_{\rm ox} + WC_{\rm GDov} + WC_{\rm GDfr}, \tag{3}$$

$$C_{\rm GS} = (1/2)WLC_{\rm ox} + WC_{\rm GSov} + WC_{\rm GSfr}. \tag{4}$$

The gate-bulk capacitance is neglected, because the inversion layer acts as a shield between the gate and the bulk:

$$C_{\rm GB} = 0.$$

Then the total gate capacitance is given by

$$C_{\rm gate} = WLC_{\rm ox} + WC_{\rm ov}. \quad (5)$$

D. Saturation Region ($V_{\rm th} < V_{\rm GS}$, $V_{\rm GS} - V_{\rm th} \le V_{\rm DS}$):

$$C_{\rm GD} = WC_{\rm GDov} + WC_{\rm GDfr}. \quad (6)$$

$$C_{\rm GS} = (2/3)WLC_{\rm ox} + WC_{\rm GSov} + WC_{\rm GSfr}. \quad (7)$$

Similar to the triode region case, the gate-substrate capacitance is given by

$$C_{\rm GB} = 0.$$

Then the total gate capacitance is given by

$$C_{\rm gate} = (2/3)WLC_{\rm ox} + WC_{\rm ov}. \quad (8)$$

Remark (i) Figure 2(b) shows the values of the gate capacitance components obtained using SPICE simulation. For example, $WC_{\rm GDov}$, $WC_{\rm GSov}$ and $WC_{\rm GDfr} + WC_{\rm GDfr}$ are obtained from SPICE simulation by setting each parameter value of $CGDO$, $GGSO$ or C_F to zero one by one.
(ii) Qualitatively speaking, the simulation results in Fig. 2 and the MOS capacitance model described above match fairly well; e.g., $C_{\rm gate}$ is larger in the accumulation region than in the depletion region, and it is larger in the triode region than in the saturation region. In our simulation results, the values of $C_{\rm GD}$, $C_{\rm GS}$ and $C_{\rm GB}$ change smoothly between the operating regions.
(iii) However the Meyer MOS capacitance model is a crude approximation, and there is an important difference between our simulation results and the model; in our simulation results, $C_{\rm GB}$ has a finite (non-zero) value in the triode and saturation regions. This is because Meyer model ignores the fact that the bulk (depletion region) charge $Q_{\rm b}$ (and hence $C_{\rm GB} = dQ_{\rm b}/V_{\rm GS}$) is determined by the channel potential which depends on $V_{\rm GS}$ and $V_{\rm DS}$ while BSIM3 model takes it into account [5]. The fact that $C_{\rm GB}$ has a finite value in triode and saturation regions is essential to our proposed method for ADC input capacitance reduction described in Sect. 3.
(iv) We have also solved Poisson's equation [8] numerically and confirmed the plausibility of the result in Fig. 2.
(v) The gate-capacitance $C_{\rm gate}$ becomes larger when an NMOS FET is ON (in saturation or triode region), compared to that when it is OFF (in depletion region). Hence one might think that as the input level of a CMOS ADC increases, the number of input differential pairs whose NMOS FETs connected to the input $V_{\rm in}$ are ON increases and thus input capacitance *increases*. However this contradicts the fact described in Sect. 2.3 that "as the input level of a CMOS ADC increases, its input capacitance *decreases*."

2.2 Nonlinearity Analysis of MOS Differential Pair Input Capacitance

In this subsection, we will obtain input capacitance characteristics of an NMOS differential pair with respect to the input level. Let us consider an NMOS differential pair with resistive loads R_l in Fig. 4(a), where the input voltage $V_{\rm in}$ and a fixed reference voltage $V_{\rm ref}$ are fed to their two input gates respectively. The input capacitance of the NMOS differential pair can be defined as the capacitance seen from the input $V_{\rm in}$.
A. SPICE Simulation Result:
Figure 4(b) shows the SPICE simulated characteristics of the input capacitance versus the input level of an NMOS input differential pair with resistive loads (Fig. 4(a)) for several voltage values of $V_{\rm ref}$, using the method in Sect. 2.1. We see that the input capacitance is large for $V_{\rm in} \ll V_{\rm ref}$, and it is small for $V_{\rm in} \gg V_{\rm ref}$, while it has the peak at $V_{\rm in} \approx V_{\rm ref}$. Now we will consider the input capacitance in three operating regions with different input levels $V_{\rm in}$.
B. In the case that $V_{\rm in} \ll V_{\rm ref}$:
In this operating region, $M1$ is OFF (in the accumulation or depletion region) while $M2$ is ON. Since $M1$ is in depletion region in our design, it follows from Eq. (2) that the input capacitance $C_{\rm in1}$ is given by

$$C_{\rm in1} = \frac{1}{1/(WLC_{\rm ox}) + 1/C_{\rm dep}} + WC_{\rm ov}. \quad (9)$$

C. In the case that $V_{\rm in} \approx V_{\rm ref}$:
In this operating region, both $M1$ and $M2$ are ON, and the differential pair circuit works as an amplifier. Note that its gain from the input $V_{\rm in}$ to the drain node of $M1$ is $-R_l \cdot g_m$ (where g_m is transconductance of $M1$), and due to the Miller effect [6], [9], the contribution of $C_{\rm GD}$ to the input capacitance is $(1+R_l \cdot g_m)C_{\rm GD}$. Then the total input capacitance $C_{\rm in2}$ is given by

$$C_{\rm in2} = (1 + R_l \cdot g_m)C_{\rm GD} + C_{\rm GS}. \quad (10)$$

Here $C_{\rm GD}$ and $C_{\rm GS}$ are given by Eqs. (6) and (7) respectively when $M1$ is in saturation region. We see that the input capacitance has the peak in this operating region due to the Miller effect.
D. In the case that $V_{\rm in} \gg V_{\rm ref}$:
In this operating region, $M1$ is ON while $M2$ are OFF, and hence all of the tail current I_b of the differential pair flows through $M1$. Thus the gate-source voltage of $M1$ (which is the voltage across $C_{\rm GS}$) keeps almost constant. Therefore little charge flows from $V_{\rm in}$ to $C_{\rm GS}$ when $V_{\rm in}$ varies, which makes the contribution of $C_{\rm GS}$ to the input capacitance of the differential pair very small. Thus the input capacitance $C_{\rm in3}$ is approximately given by

$$C_{\rm in3} \approx C_{\rm GD}. \quad (11)$$

Here $C_{\rm GD}$ is given by Eq. (6) when $M1$ is in saturation region while it is given by Eq. (3) in triode region.
Remark: (i) The input capacitance of the differential amplifier shown in Fig. 4(a) would be given by the dotted-line in Fig. 4(c) for $V_{\rm ref}$=1.75 V if we assume

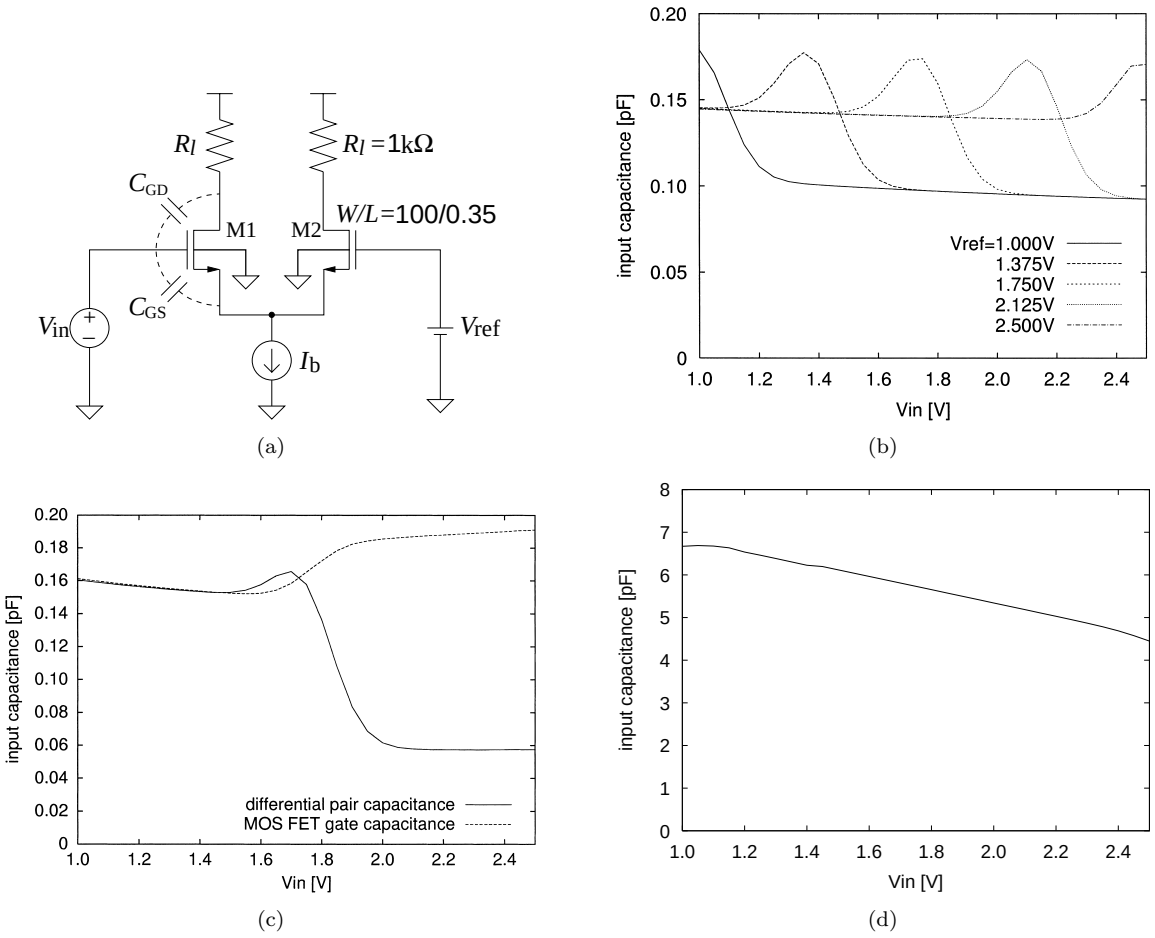

Fig. 4 (a) An NMOS input differential pair with resistive loads R_l, where the body of each NMOS FET is connected to $V_{\rm SS}$. (b) Characteristics of the input capacitance versus the input voltage level of each NMOS input differential pair with resistive loads (Fig. 4(a)) for several $V_{\rm ref}$ values of 1.000 V, 1.375 V, 1.750 V, 2.125 V and 2.500 V. (c) Characteristics of the input capacitance versus the input voltage level of each NMOS input differential pair with resistive loads (Fig. 4(a)) for $V_{\rm ref} = 1.750$ V (solid-line), and the input capacitance if we consider only the MOS FET gate capacitance (dotted-line). (d) Characteristics of the input capacitance versus the input voltage level of a CMOS ADC obtained from the summation of all the input capacitances of 45 input differential pairs with several different $V_{\rm ref}$'s. (This graph is the same as the solid-line in Fig. 7.)

that the input capacitance is equal to the MOS gate capacitance obtained in the previous subsection. However, the actual input capacitance is given by the solid-line in Fig. 4(c).

(ii) To confirm the validity of Eqs. (9), (10) and (11) we have performed SPICE simulations to obtain the bandwidth $f_{\rm BW}$ with a dummy capacitor $C_{\rm dummy}$ in parallel with $C_{\rm GD}$, $C_{\rm GS}$ or $C_{\rm GB}$ (Fig. 5).

- When $V_{\rm in} \ll V_{\rm ref}$, the effect of $C_{\rm dummy}$ between the gate and the drain is the same as that between the gate and the source; in both cases the bandwidth decreases by almost the same amount.
- When $V_{\rm in} \approx V_{\rm ref}$, the effect of $C_{\rm dummy}$ between the gate and the drain is more significant than that between the gate and the source; in both cases the bandwidth decreases, but in the former case the bandwidth reduction is more substantial. Also SPICE simulations showed that as we increase R_l, the bandwidth decreases (almost) proportionally in the former case, while it does not change much in the latter case.
- When $V_{\rm in} \gg V_{\rm ref}$, in the case of $C_{\rm dummy}$ between the gate and the drain, the bandwidth decreases significantly, while in the case of $C_{\rm dummy}$ between the gate and the source, it doesn't.

These simulation results using a dummy capacitor support the validity of our analysis above.

(iii)According to our simulation, the input capacitance $C_{\rm in1}$ (when $V_{\rm in} \ll V_{\rm ref}$) is larger than that of $C_{\rm in3}$ (when $V_{\rm in} \gg V_{\rm ref}$):

$$C_{\rm in1} > C_{\rm in3}. \tag{12}$$

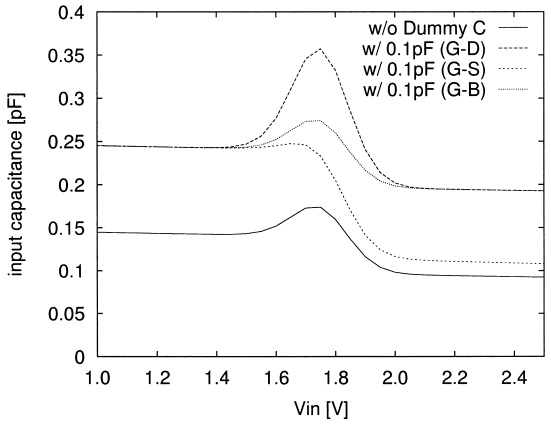

Fig. 5 Effects of dummy capacitance (0.1 pF) on the input capacitance of the differential pair (Fig. 4(a) with $V_{\rm ref}$=1.75 V). The cases of no dummy capacitor, a dummy capacitor between gate and drain of $M1$, one between gate and source, and one between gate and bulk are shown.

This can happen because
(a) when $V_{\rm in} \ll V_{\rm ref}$, $M1$ is OFF (in depletion region) and the total gate-capacitance $C_{\rm gateOFF}$ of $M1$ is smaller than $C_{\rm gateON}$, and the input capacitance $C_{\rm in1}$ is equal to the value of $C_{\rm gateOFF}$, and
(b) when $V_{\rm in} \gg V_{\rm ref}$, $M1$ is ON (in saturation region) and the input capacitance $C_{\rm in3}$ is approximately only the gate-drain capacitance part (which is mainly $C_{\rm GDov}$ and $C_{\rm GDfr}$ in saturation region) in $C_{\rm gateON}$ and its gate-source capacitance part does not affect the value of $C_{\rm in3}$.
(c) In other words, since

$$C_{\rm in1} = \frac{1}{1/(WLC_{\rm ox}) + 1/C_{\rm dep}} + WC_{\rm ov},$$

and

$$C_{\rm in3} = WC_{\rm GDov} + WC_{\rm GDfr},$$

then

$$C_{\rm in1} - C_{\rm in3} = \frac{1}{1/(WLC_{\rm ox}) + 1/C_{\rm dep}} + WC_{\rm GSov} + WC_{\rm GSfr}.$$

Hence $C_{\rm in1} > C_{\rm in3}$ holds.

2.3 Nonlinearity Analysis of CMOS ADC Input Capacitance

This section shows that the input capacitance of a CMOS ADC decreases as its input level increases and explains its reason. We consider the case that the ADC input is single-ended, and its input circuitry consists of an array of preamplifiers (NMOS differential pairs with resistive loads); for each differential pair, one of two inputs is connected to the ADC input, while the other is connected to the corresponding reference voltage (Fig. 6). This configuration is very popular in many flash-type CMOS ADCs. Figure 7 shows the characteristics of input capacitance ($C_{\rm in}$) versus the input level ($V_{\rm dc}$) obtained from SPICE simulation with BSIM3v3 parameters for 0.35 μm CMOS process, using the method of Sect. 2.1. For our SPICE simulation, we used the circuit topology of Fig. 6 with the following conditions [4]:

- the reference voltages are $V_{\rm refp} = 2.5$ V and $V_{\rm refm} = 1.0$ V,
- the unit resistor R in the resistor string is 5 Ω,
- the number of differential pairs (N) is 45,
- the resistive load R_l in each NMOS differential pair is 1kΩ,
- dimensions of each NMOS differential pair are $W = 100\,\mu$m and $L = 0.35\,\mu$m,
- the body of each NMOS FET is connected to either its source or $V_{\rm SS}$, and
- the bias current of the differential pair is 200 μA.

We see in Fig. 7 that the input capacitance decreases as the input level increases.

Next we will clarify this reason. Letting N_1 be

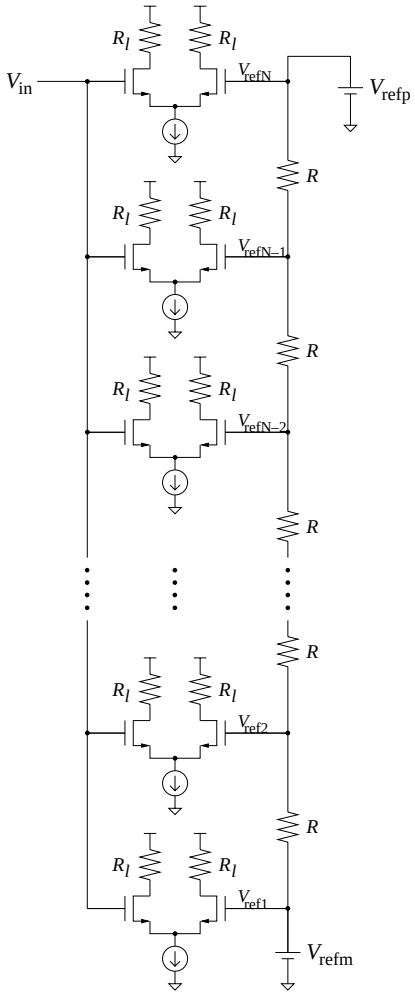

Fig. 6 A typical input circuitry of a flash-type CMOS ADC.

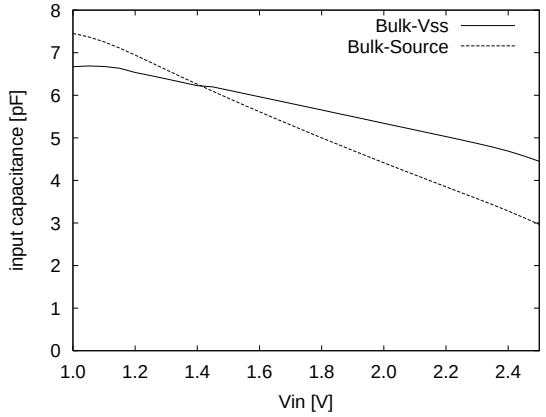

Fig. 7 Characteristics of the input capacitance versus the input voltage level of a CMOS ADC obtained from SPICE simulation of the circuit in Fig. 6. The solid-line indicates the case when the body of each NMOS is connected to $V_{\rm SS}$ in the input differential pair while the dotted-line indicates the case when it is connected to its source.

the number of input differential pairs of a CMOS ADC in the operating region of $V_{\rm in} \ll V_{\rm ref}$ (where $V_{\rm ref}$ is the corresponding reference voltage for each differential pair), N_2 be that for $V_{\rm in} \approx V_{\rm ref}$ and N_3 be that for $V_{\rm in} \gg V_{\rm ref}$. Then the total input capacitance ($C_{\rm total}$) of the CMOS ADC is given by

$$C_{\rm total} = N_1 C_{\rm in1} + N_2 C_{\rm in2} + N_3 C_{\rm in3},$$

where $N_1 + N_2 + N_3 = N$ and N is the total number of differential pairs at the input circuitry of the CMOS ADC (in our case $N = 45$). As the input voltage $V_{\rm in}$ increases, N_1 decreases and N_3 increases while N_2 keeps constant. Since we have the relationships of Eq. (12), we see that $C_{\rm total}$ decreases as the input voltage $V_{\rm in}$ increases, which explains the SPICE simulation result in Fig. 7. See also Figs. 4 and 8.

3. Effects of NMOS Body in Input Differential Pair

In this section, we will study the design issue that affects CMOS ADC input capacitance nonlinearity. As Fig. 7 shows, the input capacitance of a CMOS ADC is more nonlinear but its average value is smaller when the body of each NMOS in the input differential pairs is connected to its source (Fig. 8(a)) compared to the case when it is connected to $V_{\rm SS}$ (Fig. 4(a)). Figure 8(b) shows simulated characteristics of the input capacitance versus the input voltage level of each NMOS input differential pair with resistive loads for several $V_{\rm ref}$ values, and Fig. 8(c) shows the input capacitance characteristics of a whole CMOS ADC.

Remark: (i) The Meyer MOS capacitance model tells us that the gate-substrate capacitance $C_{\rm GB}$ is approximated to be zero in saturation and triode regions. However, in our simulation it has a finite (non-zero) value even in these regions (Fig. 2(b)). Hence precisely speaking, in case that $V_{\rm in} \gg V_{\rm ref}$, the input capacitance of the differential pair is given by

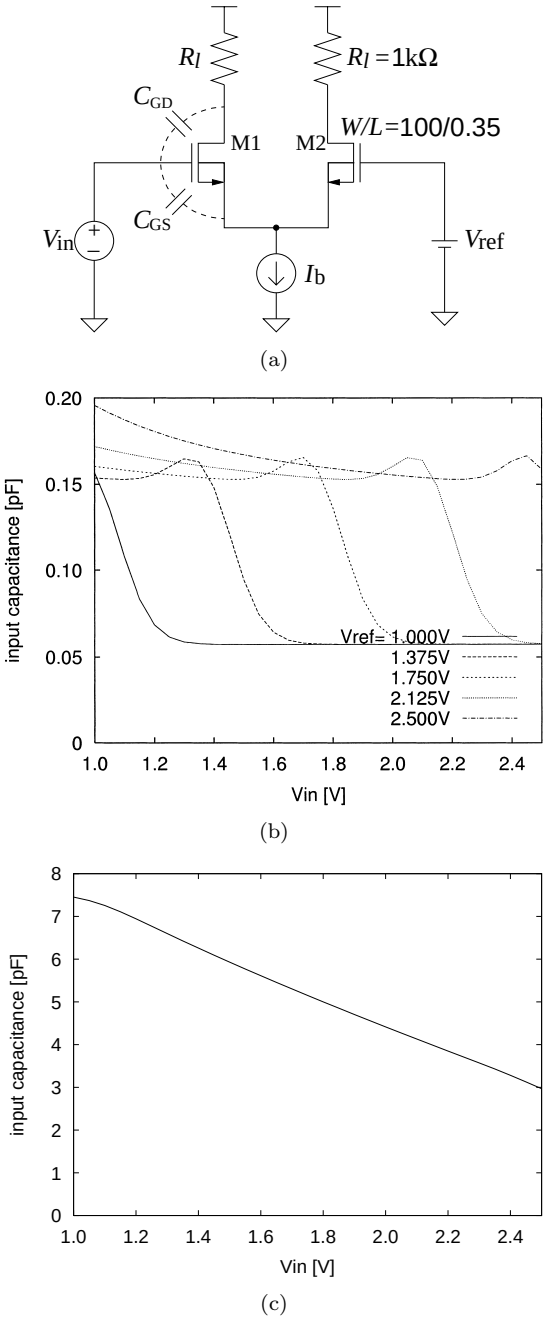

Fig. 8 (a) An NMOS input differential pair with resistive loads R_l, where the body of each NMOS FET is connected to its source. (b) Characteristics of the input capacitance versus the input voltage level of each NMOS input differential pair with resistive loads (Fig. 8(a)) for several $V_{\rm ref}$ values of 1.000 V, 1.375 V, 1.750 V, 2.125 V and 2.500 V. (c) Characteristics of the input capacitance versus the input voltage level of a CMOS ADC obtained from the summation of all the input capacitances of 45 input differential pairs with several different $V_{\rm ref}$'s. (This graph is the same as the dotted-line in Fig. 7.)

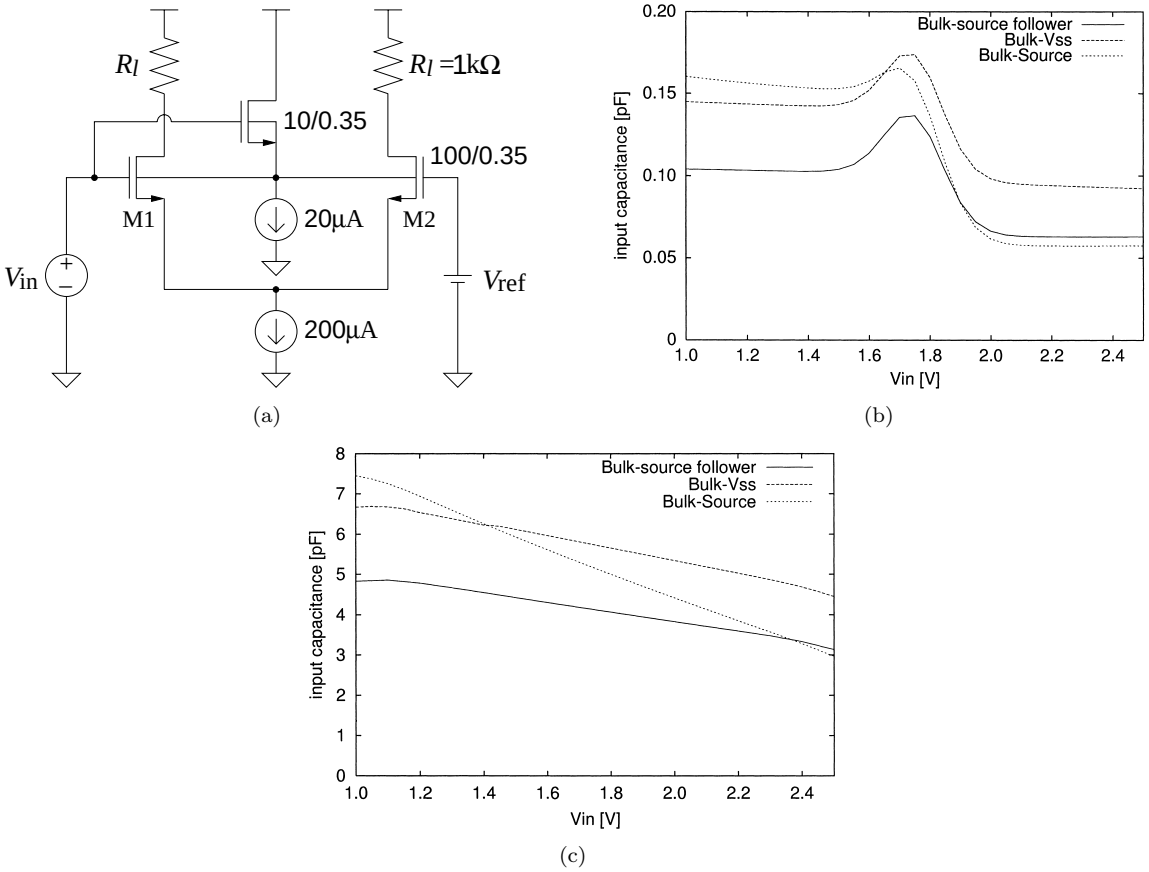

Fig. 9 (a) Proposed preamplifier with the body of an NMOS input differential pair driven by a source follower circuit. (b) Characteristics of the input capacitance versus the input voltage level of the proposed pre-amplifier for $V_{\rm ref} = 1.75$ V. "Bulk-source follower" line indicates the input capacitance in Fig. 9(a), "Bulk-Vss" line shows the one in Fig. 4(a) while "Bulk-Source" line shows the one in Fig. 8(a). We see that the input capacitance of the proposed preamplifier in Fig. 9(a) becomes smaller. (c) Characteristics of the input capacitance versus the input voltage level of CMOS ADCs. "Bulk-source follower" line indicates the input capacitance of a ADC when the pre-amplifiers in Fig. 9(a) are used, and "Bulk-Vss" line shows the one when those in Fig. 4(a) are used. Also "Bulk-Source" line shows the one when those in Fig. 8(a) are used. We see that when the proposed preamplifiers in Fig. 9(a) are used, the (average) input capacitance value of a CMOS ADC is reduced even though its input voltage dependency remains as almost the same.

$$C_{\rm in3} = C_{\rm GD} + C_{\rm GB}$$

when the NMOS body is connected to $V_{\rm SS}$. However when the NMOS body is connected to its source, it is given by

$$C_{\rm in3} = C_{\rm GD}$$

because $V_{\rm GB}$ $(= V_{\rm GS})$ does not change much when $V_{\rm in}$ changes for $V_{\rm in} \gg V_{\rm ref}$ (which is the same reason as in Sect. 2.2 D). This explains the results in Figs. 8(b) and (c).

(ii) The input capacitance of a CMOS ADC may be required to be linear for its better AC performance and in such a case the body of NMOS FET should be connected to $V_{\rm SS}$, rather than its source; for example, the input capacitance of the CMOS ADC can be used as a hold capacitance for its preceding track/hold circuit and in such a case the capacitance nonlinearity degrades its AC performance [10].

Next we propose a preamplifier circuit in Fig. 9(a) where the differential pair NMOS body is driven by a source follower circuit. In this case, $C_{\rm GB}$ of $M1$ does not contribute to the input capacitance of the preamplifier circuit for the whole input range of $V_{\rm in}$. Figure 9(b) shows the simulated input capacitance of the preamplifier in Fig. 9(a) for $V_{\rm ref} = 1.75$ V and Fig. 9(c) shows the simulated CMOS ADC input capacitance when the preamplifiers in Fig. 9(a) are used. We see that the (average) input capacitance value of a CMOS ADC is reduced even though its input voltage dependency remains as almost the same.

Remark: (i) According to our SPICE simulation, the effect of the size variation of a small MOS-

FET ($10\,\mu$m/$0.35\,\mu$m) is small; when the size of ($10\,\mu$m/$0.35\,\mu$m) changes by $\pm 50\%$, the input capacitance changes by less than $\pm 5\%$.
(ii) If we incorporate this method (Fig. 9(a)) in our ADC design [4], it is estimated that the power dissipation of the ADC increases about by 1% and its chip area increase is about 5%.
(iii) We note that a similar method has been also used in a track/hold circuit [11].

4. Conclusions

We have described the nonlinear behavior of CMOS ADC input capacitance. With SPICE AC simulation based on BSIM3v3 model, we showed that the input capacitance of a CMOS ADC decreases as the input voltage increases. However this characteristics cannot be explained by the nonlinear property of MOS gate-capacitance alone; we have to consider the input capacitance of an MOS differential pair for three operating regions. Using this method, we can explain the nonlinear behavior of CMOS ADC input capacitance. Also we have discussed the design issues for the input capacitance; we have found that the CMOS ADC input capacitance is more nonlinear but its total value is smaller when the NMOS body of the input differential pair (preamplifier) is connected to its source compared to the case when it is connected to V_{SS}. Further, we propose a preamplifier circuit where the differential pair NMOS body is driven by a source follower circuit to reduce the ADC input capacitance. The followings are left for the future work:

- Clarification of the relationships between the CMOS ADC overall performance and its input capacitance nonlinearity.
- Experimental verification of the results described here.

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References

[1] B. Razavi, Principles of Data Conversion System Design, IEEE Press, 1995.
[2] R.V. Plassche, Integrated Analog-to-Digital and Digital-to-Analog Converters, Kluwer Academic Publishers, 1994.
[3] H. Kobayashi, K. Kobayashi, H. Sakayori, and Y. Kimura, "ADC standard and testing in japanese industry," Computer Standards & Interfaces, vol.23, pp.57–64, Elsevier Science, March 2001.
[4] K. Kobayashi, N. Takahashi, H. Kobayashi, Y. Onaya, H. San, H. Sugawara, Y. Takahashi, H. Kogure, K. Ishiwata, Y. Kimura, Y. Yuminaka, Y. Sasaki, K. Tanaka, and F. Abe, "Design of a 3.0 V 200 MS/s 8 bit folding/interpolation ADC with $0.35\,\mu$m CMOS process," Proc. 13th Workshop on Circuits and Systems in Karuizawa, pp.349–354, April 2000.
[5] Y. Cheng and C. Hu, MOSFET Modeling & BSIM3 User's Guide, Kluwer Academic Publishers, 1999.
[6] B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2001.
[7] J.E. Meyer, "MOS models and circuit simulation," RCA Review, vol.32, March 1971.
[8] Y. Tsividis, Operation and Modeling of the MOS Transistor, 2nd ed., McGraw-Hill, 1999.
[9] D. Johns and K. Martin, Analog Integrated Circuit Design, John Wiley and Sons, New York, 1997.
[10] H. Kobayashi, M.A. Mohamed Zin, H. Sato, K. Kobayashi, H. San, J. Ichimura, Y. Onaya, N. Kurosawa, Y. Kimura, Y. Yuminaka, K. Tanaka, T. Myono, and F. Abe, "High-speed CMOS track/hold circuit design," Analog Integrated Circuits and Signal Processing, vol.27, pp.161–170, Kluwer Academic Publishers, April 2001.
[11] A. Boni, A. Pierazzi, and C. Morandi, "A 10b 185 MS/s track-and-hold in $0.35\,\mu$m CMOS," IEEE J. Solid-State Circuits, vol.36, no.2, pp.195–203, Feb. 2001.

Appendix: Definition of Input Capacitance

Let us consider a general circuit in Fig. A· 1. If we change the input voltage from $V_{\rm in}$ to $V_{\rm in} + dV_{\rm in}$ and an amount of charge, $dQ_{\rm in}$, flows from the input voltage source to the circuit, then the input capacitance $C_{\rm in}$ at the input voltage operating point of $V_{\rm in}$ is defined as

$$C_{\rm in} = \frac{dQ_{\rm in}}{dV_{\rm in}}.$$

If the value of $C_{\rm in}$ is constant regardless of the value of $V_{\rm in}$, the input capacitance is said to be *linear*. On the other hand, if $C_{\rm in}$ is a function of the input voltage $V_{\rm in}$ (i.e., $C_{\rm in}$ is expressed as $C_{\rm in}(V_{\rm in})$), it is said to be *nonlinear*.

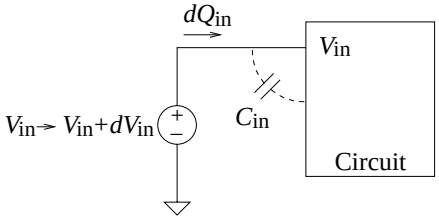

Fig. A· 1 Definition of input capacitance for a general circuit whose input is $V_{\rm in}$.

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