PAPER *Special Section on Analog Circuit Techniques and Related Topics*

High-Efficiency Charge-Pump Circuits which Use a $0.5V_{dd}$-Step Pumping Method

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SUMMARY This paper presents a $0.5V_{dd}$-step pumping method for Dickson-type charge-pump circuits that achieve high overall efficiency, including regulator circuitry, even at large output currents, and these circuits are targeted at mobile equipment applications. We have designed positive and negative charge-pump circuits which use a $0.5V_{dd}$-step pumping method, are implemented with advanced control functions, and are fabricated with our custom CMOS process. Measured results showed that efficiency of a 2.5-stage positive charge-pump circuit before regulation is more than 93% (power supply $V_{dd} = 5\,\mathrm{V}$, output voltage $V_{out} = 16.9\,\mathrm{V} \fallingdotseq 3.5V_{dd}$, output current $I_{out} = 4\,\mathrm{mA}$), and that of a 1.5-stage negative charge-pump circuit is 93% (power supply $V_{dd} = 5\,\mathrm{V}$, output voltage $V_{out} = -7.2\,\mathrm{V} \fallingdotseq -1.5V_{dd}$, output current $I_{out} = 4\,\mathrm{mA}$).

key words: *charge-pump circuit, DC-DC converter, high-efficiency, high-voltage generation*

1. Introduction

Recently video products such as digital video cameras, digital still cameras (DSC), and DSC phones incorporate charge coupled devices (CCDs) for video image acquisition, and to drive CCDs it is necessary to generate high voltages such as +12 V (at output current of several mA) and −6.5 V (at several mA) from a $V_{dd} = 5\,\mathrm{V}$ supply. At present, switching regulators are widely used for such applications because they can generate high voltages with excellent power efficiency. However, they generate harmonic noise during switching, and also require bulky, costly, off-chip coils. Charge-pump circuits, on the other hand, have the advantage of low noise, and do not require coils, but conventional charge-pump circuits [3]–[8] suffer from relatively low efficiency at large output current loads, which makes it difficult to apply them to power supply circuits in mobile products where high efficiency is the top priority.

In a previous paper [2] we proposed a new charge-pump circuit design with high efficiency at large output current loads, to realize miniature, low-cost mobile equipment. However it had the following disadvantage: Let us consider the 2-stage Dickson charge-pump circuit [3] in Fig. 1, and for simplicity neglect the diode voltage drop and other voltage and current losses. Then the output voltage (V_{out}) is $3V_{dd}$ when V_{in} is equal to V_{dd} and the clock amplitude is V_{dd}. Similarly the output voltage of an n-stage charge-pump is $(n+1)V_{dd}$; in other words, the output of such a charge-pump circuit can take only values that are a multiple of V_{dd} [2]–[8], such as $2V_{dd}$, $3V_{dd}$, $4V_{dd}$, $5V_{dd}$. Thus when a power supply voltage of V'_{out} is needed, an n-stage charge-pump circuit is used to generate $V_{out} = (n+1)V_{dd}$, where $nV_{dd} < V'_{out} < (n+1)V_{dd}$, and the following regulator produces V'_{out} from $(n+1)V_{dd}$ $(= V_{out})$ (Fig. 1). Hence the power loss corresponds to the voltage drop $V_{out} - V'_{out}$ in the regulator, and the maximum achievable total efficiency η' including the regulator is $\eta' = 1 - (V_{out} - V'_{out})/V_{out}$. For example, when $V_{dd} = 5\,\mathrm{V}$ and $V'_{out} = 6.5\,\mathrm{V}$, then $n = 1$ is chosen and $V_{out} = 10\,\mathrm{V}$ and $\eta' = 1 - (V_{out} - V'_{out})/V_{out} = 65\%$; this efficiency is substantially lower than a switching regulator and thus limits usefulness of such charge-pump circuits.

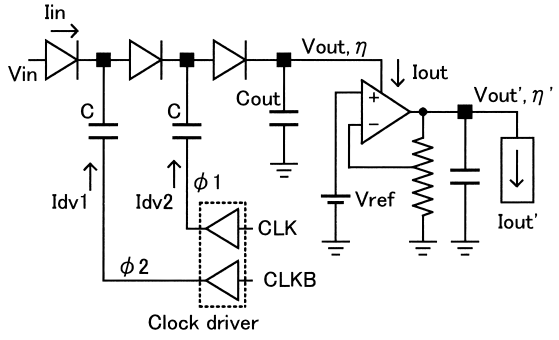

Fig. 1 Dickson charge-pump, and output voltage control regulator circuit.

In this paper we describe a new "$0.5V_{dd}$-step pumping method" developed to overcome this problem; this method allows the output voltage of a charge-pump circuit to take values that are a multiple not of V_{dd} but of $0.5V_{dd}$ — e.g. $1.5V_{dd}$, $2V_{dd}$, $2.5V_{dd}$, $3V_{dd}$, $3.5V_{dd}$, $4V_{dd}$, etc. For example, when $V_{dd} = 5\,\mathrm{V}$ and $V'_{out} = 6.5\,\mathrm{V}$, then $n = 0.5$ is chosen and $V_{out} = 7.5\,\mathrm{V}$

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and $\eta' = 1 - (V_{out} - V'_{out})/V_{out} = 87\%$, which is much higher than the 65% of the conventional charge-pump circuit above. Our proposed $0.5V_{dd}$-step pumping method can be implemented with two first-stage capacitors which can be switched in series or in parallel [1], and the effectiveness of this circuit is demonstrated by actual chip implementation and measurements.

Section 2 discusses output voltage and total efficiency of charge-pump circuits. Section 3 describes positive charge-pump circuit design using our proposed $0.5V_{dd}$-step pumping method, while Sect. 4 discusses negative charge-pump circuit design using our proposed method. Section 5 describes related test element group (TEG) chip design and our custom CMOS fabrication process, and Sect. 6 presents measurement results. Finally Sect. 7 provides conclusions.

2. Total Efficiency of Charge-Pump Circuit

2.1 Basics of Charge-Pump Circuit

Figure 1 shows a Dickson charge-pump circuit, and its boosted output voltage (V_{out}) in the steady state is given by

$$V_{out} = V_{in} - V_d + n(V'_\phi - V_l - V_d). \quad (1)$$

Here V'_ϕ is the voltage amplitude of the clock signal at each pumping node associated with coupling capacitance, V_l is the voltage fluctuation caused by current I_{out} that flows through the diode and V_d is the voltage drop of the diode. Also V_{in} is the circuit input voltage; it is V_{dd} for a positive pumping circuit and 0 for a negative one, and n is the number of charge-pump stages. Note that V_l is expressed as follows [2], [3]:

$$V_l = \frac{2I_{out}T/2}{C + C_s} = \frac{I_{out}}{f(C + C_s)}, \quad (2)$$

where C is clock coupling capacitor, C_s is parasitic capacitance at each node, f and T are the pumping clock frequency and period respectively. Let V_ϕ be the pumping clock amplitude, and then V_ϕ and V'_ϕ are expressed as follows [2]:

$$V_\phi = V_{dd} - \Delta V_{ds(P)} - \Delta V_{ds(N)}, \quad (3)$$

$$V'_\phi = V_\phi \frac{C}{C + C_s}, \quad (4)$$

where $\Delta V_{ds(P)}$ and $\Delta V_{ds(N)}$ are drain-source voltages (V_{ds}) of the clock-driver p-channel and n-channel MOSFETs respectively when current $2I_{out}$ flows through the clock-driver. Neglecting voltage drops and leakage current in the charge-pump circuit, the efficiency before regulation is given by

$$\eta = \frac{V_{out}I_{out}}{V_{dd}(I_{in} + I_{dv} + I_{fcv})}. \quad (5)$$

Here I_{in} is the input current from V_{in}, I_{dv} is the total current from the clock drivers into the charge pump circuit (i.e., $I_{dv} = I_{dv1} + I_{dv2}$), and I_{fcv} is the total current of clock driver circuits to charge and/or discharge parasitic capacitances at external nodes. Note that in practice the amount of bias current that flows in the regulator is designed to be small enough to be ignored, so that the output current (I_{out}) from the charge-pump circuit is almost equal to the output current (I'_{out}) from the regulator.

2.2 Output Voltage Regulator Circuit and Total Circuit Efficiency

Operational-amplifier regulator circuits (Fig. 1) are widely used to produce required output voltages (V'_{out}) from boosted output voltages (V_{out}). However, the drawback is that circuit efficiency is degraded due to the voltage drop ($V_{out} - V'_{out}$) of the operational amplifier. Note that the smaller the value of $(V_{out} - V'_{out})/V_{out}$, the higher the efficiency of the whole circuit including regulator circuit. Also note that when the number n of pump stages is small, $(V_{out} - V'_{out})/V_{out}$ can be quite large. For example, suppose that $V_{dd} = 4.5\,\mathrm{V}$, $5.0\,\mathrm{V}$ or $5.5\,\mathrm{V}$ and $V'_{out} = 6.5\,\mathrm{V}$, then the optimal value of n is 1 for the conventional charge-pump circuit because the number n must be an integer ($n = 1, 2, 3, \cdots$). The maximum achievable efficiency (η') of this charge-pump circuit including regulator circuit is given in Table 1, where η' is given by

$$\eta' = 1 - \frac{V_{out} - V'_{out}}{V_{out}} = 1 - \frac{(n+1)V_{dd} - V'_{out}}{(n+1)V_{dd}} \quad (n = 1, 2, 3, \cdots). \quad (6)$$

On the other hand, η'' in Tables 1 and 2 represents the actual efficiency when losses in charge-pump circuits are taken into account; these losses depend on the specification, design and operating conditions of the charge pump circuit. However from our experiences, we assume here that they are 5% [2] for a V_{dd}-step charge pump circuit and they are 7% for a $0.5V_{dd}$-step one(see Sect. 5.3).

Table 1 Efficiency of conventional charge-pump circuits including regulator circuits for $V'_{out} = 6.5\,\mathrm{V}$.

V_{dd} (V)	n	V_{out}(V)	η' (%)	η'' (%)
4.5	1	9	72	67
5	1	10	65	60
5.5	1	11	59	54

Table 2 Efficiency of $0.5V_{dd}$-step charge-pump circuits including regulator circuits for $V'_{out} = 6.5\,\mathrm{V}$.

V_{dd} (V)	n	V_{out}(V)	η' (%)	η'' (%)
4.5	1	9	72	67
5	0.5	7.5	87	80
5.5	0.5	8.25	79	72

Table 2 shows that high charge-pump circuit efficiency can be realized with a $0.5V_{dd}$-step pumping method where n can be 0.5, 1, 1.5, 2, 2.5, 3, ..., which results in smaller required voltage drop $V_{out} - V'_{out}$. η' in Table 2 is given by:

$$\eta' = 1 - \frac{V_{out} - V'_{out}}{V_{out}} = 1 - \frac{(n+1)V_{dd} - V'_{out}}{(n+1)V_{dd}} \quad (n = 0.5, 1, 1.5, 2, 2.5, \cdots). \tag{7}$$

Tables 1 and 2 show that the actual efficiency (η'') reaches approximately 93% of the corresponding value of η, and for a $0.5V_{dd}$-step charge-pump circuit, an efficiency η'' as high as 80% can be obtained if V_{dd} is between 4.9 V and 5.1 V, and n is fixed at 0.5.

3. Positive $0.5V_{dd}$-Step Charge-Pump Circuit

3.1 Principle of Proposed Positive $0.5V_{dd}$-Step Charge-Pump Circuit

In this subsection we will describe the principle of our proposed positive $0.5V_{dd}$-step charge-pump circuit. Figures 2 and 3 explain the operation of a positive $0.5V_{dd}$-step charge-pump circuit where a constant current (I_{out}) flows from an output node (V_{out}). The circuit is characterized by two capacitors (at the first pump) which are switched in series or in parallel. Its operation can be explained as follows, where all the current and voltage losses are neglected for simplicity:
(i) When CLK=Low (0), S1=off, S2=on, and S3=off (Fig. 2).

The two capacitors are connected in series and each capacitor is charged to $0.5V_{dd}$. Also V_1 becomes V_{dd}, and I_{in} becomes I_{out}.
(ii) When CLK=High (V_{dd}), S1=on, S2=off, and S3=on (Fig. 3).
The two capacitors are connected in parallel, and V_1 ($= V_{out}$) is pumped to $1.5V_{dd}$. The current which flows from the clock-driver (I_{dv}) is $2I_{out}$.

Remark: (i) The time averages of I_{in} and I_{dv} are $0.5I_{out}$ and I_{out}, respectively.
(ii) No deterioration in the efficiency is due to the $1.5V_{dd}$ pumping voltage, so if we assume that the circuits are ideal then the circuit efficiency is 100% as shown in Eq. (8).

$$\eta = \frac{V_{out}I_{out}}{V_{dd}(I_{in} + I_{dv})} = \frac{(1.5V_{dd})I_{out}}{V_{dd}(1.5I_{out})} = 100(\%) \tag{8}$$

(iii) If the two capacitors were always connected in parallel (or in series) during operation, the circuit would work as a V_{dd}-step charge-pump circuit, and V_{out} is pumped to $2V_{dd}$. In other words, either $1.5V_{dd}$ or $2V_{dd}$ output can be selected for V_{out} in Fig. 2, and the value of n (the number of stages) can be toggled between 0.5 and 1.

3.2 Circuit Design of a Positive $0.5V_{dd}$-Step Charge-Pump Circuit Using MOSFET Switches

In this subsection, we will describe circuit design of a positive $0.5V_{dd}$-step charge-pump circuit. Figure 4 shows the designed circuit where a $0.5V_{dd}$-step generation block (which has nodes A to F) is added to a positive charge-pump circuit [2]. Figures 5 and 6 explain the operation of a $0.5V_{dd}$-step generation circuit; Fig. 5 shows operation when the pumping clock (CLK) is low, while Fig. 6 shows when it is high. Figure 7 shows a normal level-shift circuit, while Fig. 8 shows an inverter-type level shift circuit; these are used in Figs. 4, 5, 6, 13, 14 and 15. A unique feature of the circuit in Fig. 4 is that internal node voltages of the charge-pump circuit are utilized to provide all the gate-source voltages (V_{gs}) for both the charge transfer MOSFETs (M1,

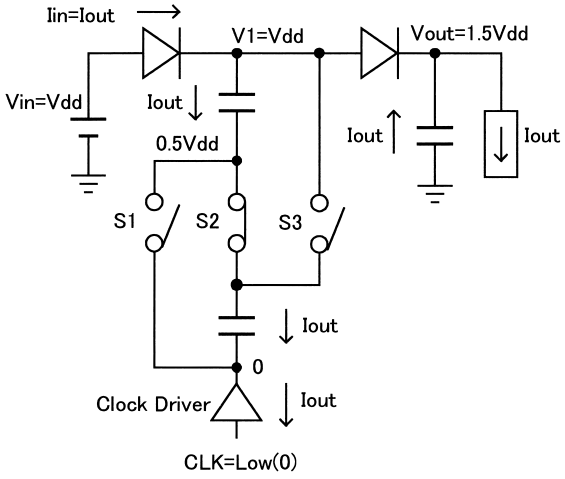

Fig. 2 Operation of a positive $0.5V_{dd}$-step charge-pump circuit (CLK=Low).

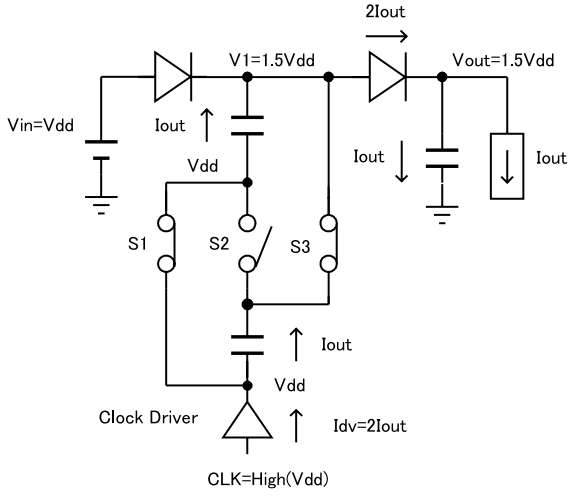

Fig. 3 Operation of a positive $0.5V_{dd}$-step charge-pump circuit (CLK=High).

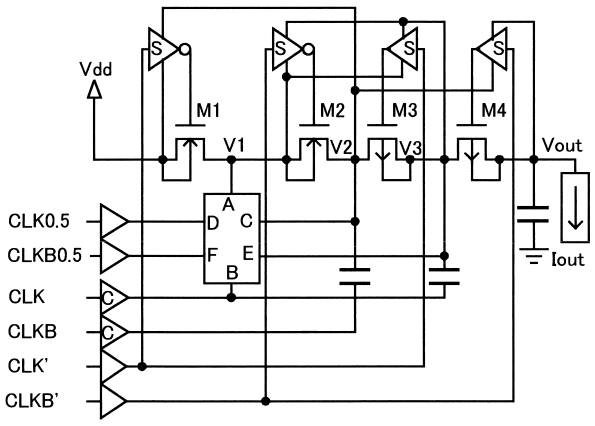

Fig. 4 Whole circuit of a positive $0.5V_{dd}$-step charge-pump circuit using MOSFET switches.

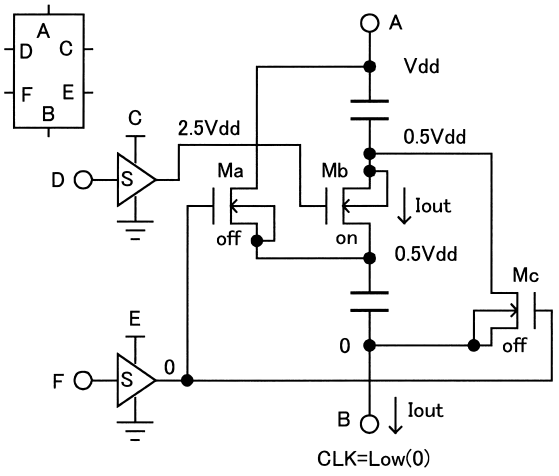

Fig. 5 Positive $0.5V_{dd}$-step generation block (CLK=Low).

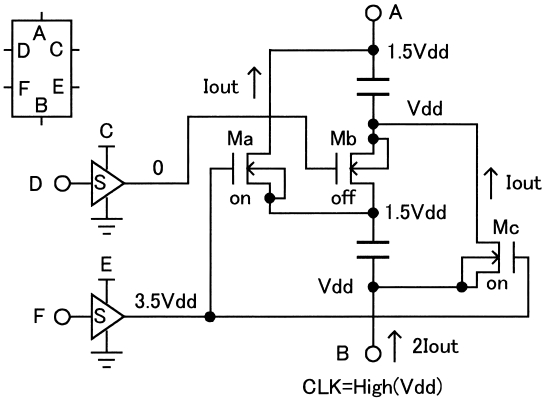

Fig. 6 Positive $0.5V_{dd}$-step generation block (CLK=High).

M2, M3, M4 in Fig. 4) and the switch MOSFETs (Ma, Mb, Mc) in the $0.5V_{dd}$-step generation block (Figs. 5 and 6); this can improve the efficiency. Figure 9 shows a clock driver circuit where the NMOS and PMOS never turn on simultaneously and hence no current flows from V_{dd} to V_{ss} directly. Figure 10 shows a clock timing diagram and approximate voltage waveforms at pumping nodes. Table 3 shows gate-source voltage (V_{gs}) and drain-source voltage (V_{ds}) values of charge transfer MOSFET (M1, M2, M3, M4 in Fig. 4).

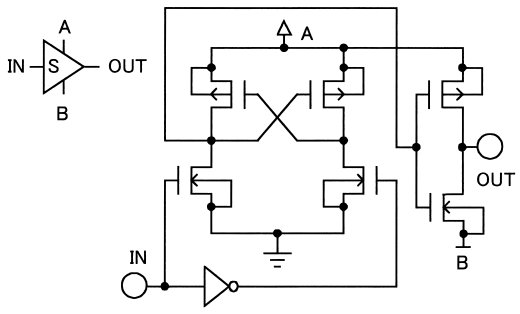

Fig. 7 Normal level shift circuit.

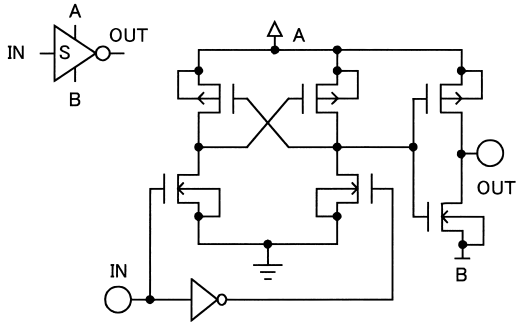

Fig. 8 Inverter-type level shift circuit.

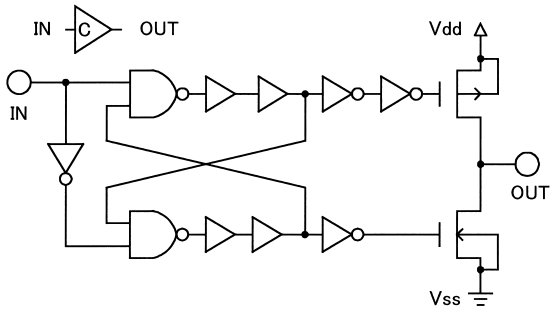

Fig. 9 Clock driver circuit.

The critical design issue is that node voltage V_1 should always remain between V_{dd} and $1.5V_{dd}$. If node voltage V_1 goes down below V_{dd}, the diode D1 becomes forward-biased and a large amount of excess charge flows from V_{dd} to V_1. Also if node voltage V_1 goes up above $1.5V_{dd}$, the diode D2 becomes forward-biased and a large amount of excess charge flows from V_1 to V_{out}. Furthermore, we have to design the circuit so that reverse currents [2] should not be generated in Fig. 6. Considering these points, we have designed clock timing (Fig. 10), and our positive $0.5V_{dd}$-step charge-pump circuit (shown in Figs. 4, 5, 6) operates in the following sequence:

① Turn off the charge transfer MOSFETs M1 and M3.

② Disconnect series connection of the two capacitors.
③ Make CLK high.
④ Connect the two capacitors in parallel.
⑤ Turn on the charge transfer MOSFETs M2 and M4.
⑥ Turn off the charge transfer MOSFETs M2 and M4.
⑦ Disconnect the parallel connection of the two capacitors.
⑧ Make CLK low.
⑨ Connect the two capacitors in series.
⑩ Turn on the charge transfer MOSFETs M1 and M3.

Table 4 shows gate-source and drain-source voltages applied to the switch MOSFETs in Figs. 5 and 6.

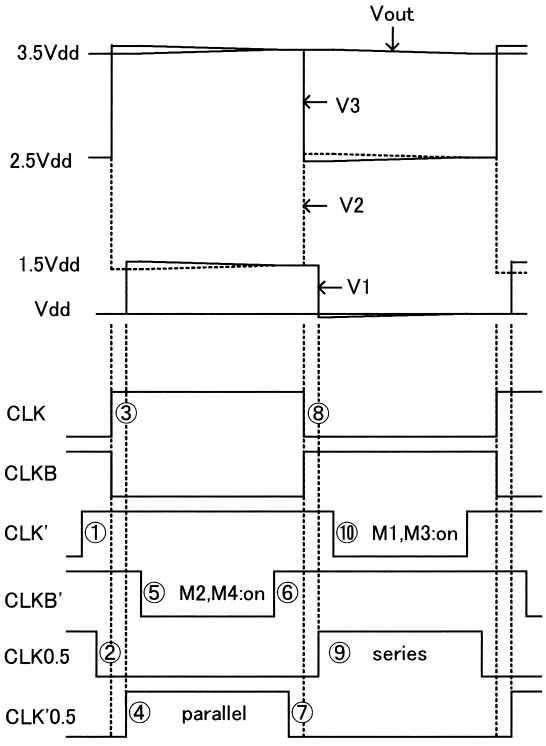

Fig. 10 Clock timing and voltage waveforms at pumping nodes of a positive $0.5V_{dd}$-step charge-pump circuit.

Table 3 Gate-source and drain-source voltages applied to charge transfer MOSFETs in Fig. 4.

MOSFET No.	$\|V_{gs}\|$ when on	$\|V_{ds}\|$ when off
M1	$1.5V_{dd}$	$0.5V_{dd}$
M2	$2V_{dd}$	$1.5V_{dd}$
M3	$2V_{dd}$	$2V_{dd}$
M4	$2V_{dd}$	V_{dd}

Table 4 Gate-source and drain-source voltages applied to the switch MOSFETs in a $0.5V_{dd}$-step generation block (Figs. 5 and 6).

MOSFET No.	V_{gs} when ON	V_{ds} when OFF
Ma	$2V_{dd}$	$0.5V_{dd}$
Mb	$2V_{dd}$	$0.5V_{dd}$
Mc	$2.5V_{dd}$	$0.5V_{dd}$

We see from Tables 3 and 4 that the maximum values of V_{gs} and V_{ds} are $2.5V_{dd}$ and $2V_{dd}$ respectively, and based on these values we can decide the (breakdown voltage) specification of the MOS devices required for the charge-pump circuit implementation.

4. Negative $0.5V_{dd}$-Step Charge-Pump Circuits

4.1 Principle of Proposed Negative $0.5V_{dd}$-Step Charge-Pump Circuit

In this subsection we will describe the principle of our negative $0.5V_{dd}$-step charge-pump circuit. Figures 11 and 12 explain the operation of a negative $0.5V_{dd}$-step charge-pump circuit where a constant current (I_{out}) flows into the output node (V_{out}). Again the unique feature of the circuit is that the two capacitors in the first stage are switched in series or in parallel. Circuit operation can be explained as follows, where all the current and voltage losses are neglected for simplicity.
(i) If CLK=High (V_{dd}), S1=off, S2=on, and S3=off (Fig. 11).

The two capacitors are connected in series, and each capacitor is charged to $0.5V_{dd}$ in the opposite direction to the positive $0.5V_{dd}$-step charge-pump circuit. Then V_1 becomes 0, and I_{dv} becomes I_{out}.
(ii) If CLK=Low (0), S1=on, S2=off, and S3=on (Fig. 12). The two capacitors are connected in parallel and V_1 ($=V_{out}$) is pumped to the negative voltage $-0.5V_{dd}$.

Remark: (i) For a positive charge-pump circuit, the two capacitors for the $0.5V_{dd}$-step pumping are connected in series when the corresponding pumping clock is low and they are connected in parallel when it is high. On the other hand, for a negative charge-pump

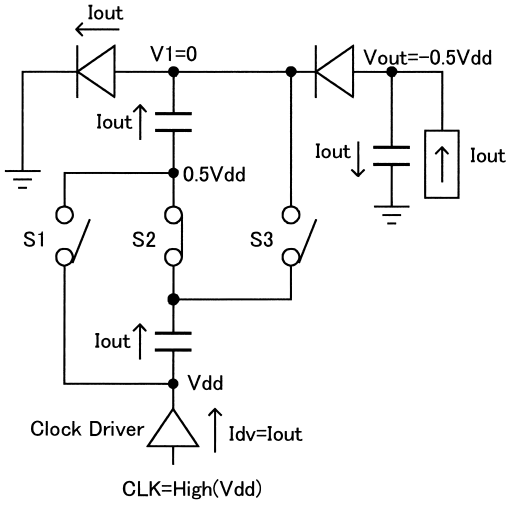

Fig. 11 Operation of a negative $0.5V_{dd}$-step charge-pump circuit (CLK=High).

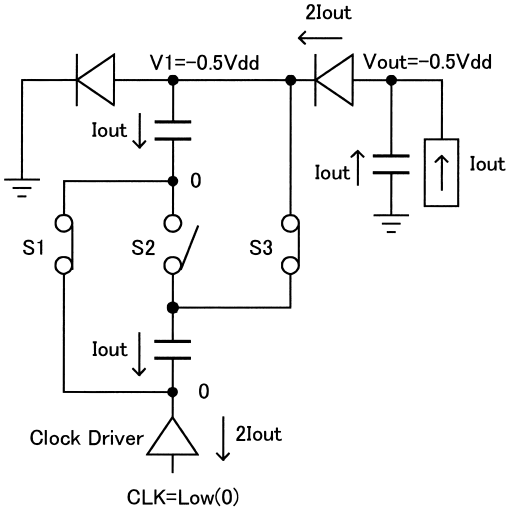

Fig. 12 Operation of a negative $0.5V_{dd}$-step charge-pump circuit (CLK=Low).

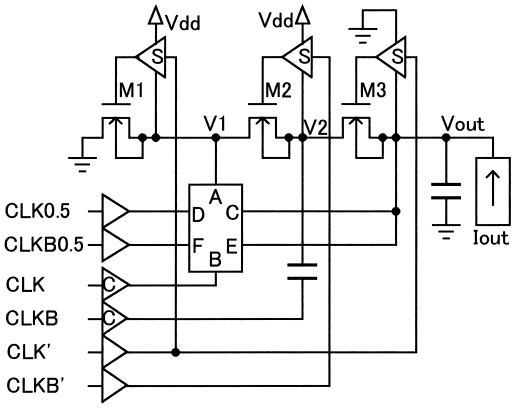

Fig. 13 Whole circuit of a negative $0.5V_{dd}$-step charge-pump circuit.

circuit, the two capacitors for the $0.5V_{dd}$-step pumping are connected in parallel when the corresponding pumping clock is low and they are connected in series when it is high.

(ii) Only the clock driver current flows into the circuit from the power source, and if the time-average is taken then $I_{dv} = 0.5I_{out}$ results.

(iii) No deterioration in the efficiency occurs due to $V_{out} = -0.5V_{dd}$; if we assume that the circuits are ideal then the circuit efficiency is 100% as shown in Eq. (9).

$$\eta = \frac{(0.5V_{dd})I_{out}}{V_{dd}(0.5I_{out})} = 100\% \tag{9}$$

(iv) When the two capacitors are always connected in parallel (or in series), we obtain $V_{out} = -V_{dd}$.

4.2 Circuit Design of a Proposed Negative $0.5V_{dd}$-Step Charge-Pump Circuit Using MOSFET Switches

In this subsection we describe circuit design of a negative $0.5V_{dd}$-step charge-pump circuit using MOSFET switches. Figure 13 shows its circuit design where a $0.5V_{dd}$-step generation block is added to a negative charge-pump circuit [2]. Figures 14 and 15 explains the

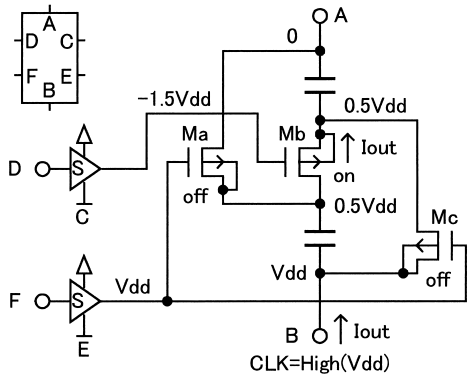

Fig. 14 Negative $0.5V_{dd}$-step generation block (CLK=High).

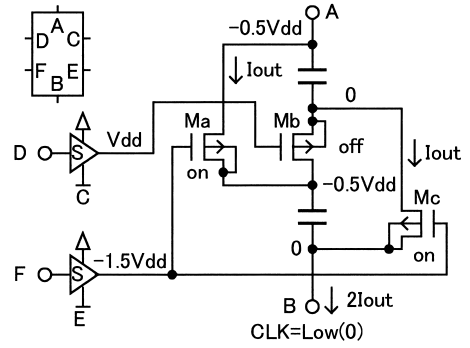

Fig. 15 Negative $0.5V_{dd}$-step generation block (CLK=Low).

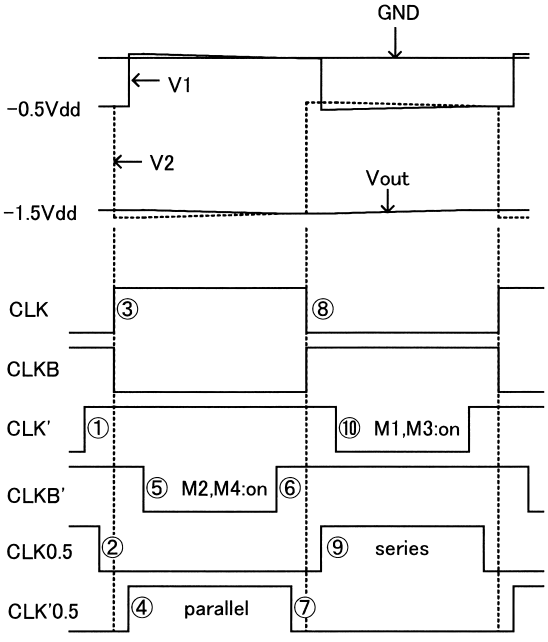

Fig. 16 Clock timing and voltage waveforms at pumping nodes of a negative $0.5V_{dd}$-step charge-pump circuit.

Table 5 Gate-source and drain-source voltages applied to the charge transfer MOSFETs in Fig. 13.

MOSFET No.	$\|V_{gs}\|$ when on	$\|V_{ds}\|$ when off
M1	V_{dd}	$0.5V_{dd}$
M2	$1.5V_{dd}$	$1.5V_{dd}$
M3	$1.5\ V_{dd}$	V_{dd}

Table 6 Gate-source and drain-source voltages applied to the switch MOSFETs in the negative $0.5V_{dd}$-step generation block in Figs. 14 and 15.

MOSFET No.	$\|V_{gs}\|$ when on	$\|V_{ds}\|$ when off
Ma	V_{dd}	$0.5V_{dd}$
Mb	$2V_{dd}$	$0.5V_{dd}$
Mc	$1.5V_{dd}$	$0.5V_{dd}$

operation of the $0.5V_{dd}$-step generation circuit; Fig. 14 shows its operation when the pumping clock (CLK) is high while Fig. 15 shows when the CLK is low. Also Fig. 16 gives clock timing diagram and approximate voltage waveforms at pumping nodes. Table 5 shows gate-source and drain-source voltages applied to the charge transfer MOSFETs (M1, M2, M3 in Fig. 13) and Table 6 shows those of the switch MOSFETs (Ma, Mb, Mc) in the $0.5V_{dd}$-step generation block (in Figs. 14 and 15).

5. TEG Chip Design and Fabrication

We have designed and fabricated a positive 2.5-stage ($0.5V_{dd}$-step) charge-pump circuit (Fig. 4) and a negative 1.5-stage ($0.5V_{dd}$-step) charge-pump circuit (Fig. 13) in one chip; both can output the current from 2 mA to 4 mA with $V_{dd} = 5$ V. The MOSFET sizes of the positive $0.5V_{dd}$-step charge-pump circuit are as follows:
- Charge transfer p-channel MOSFET:
$W/L = 6000/1.8\,(\mu\text{m}/\mu\text{m})$
- Charge transfer n-channel MOSFET:
$W/L = 3000/1.8\,(\mu\text{m}/\mu\text{m})$
- $0.5V_{dd}$ generation switch n-channel MOSFET:
$W/L = 3000/1.8\,(\mu\text{m}/\mu\text{m})$
- Clock driver p-channel MOSFET:
$W/L = 8000/1.8\,(\mu\text{m}/\mu\text{m})$
- Clock driver n-channel MOSFET:
$W/L = 8000/1.8\,(\mu\text{m}/\mu\text{m})$
Here, W is the channel width and L is the channel length. Also the MOSFET sizes of the negative $0.5V_{dd}$-step charge-pump circuit are as follows:
- Charge transfer n-channel MOSFET:
$W/L = 3000/1.8\,(\mu\text{m}/\mu\text{m})$
- $0.5V_{dd}$ generation switch p-channel MOSFET:
$W/L = 4000/1.8\,(\mu\text{m}/\mu\text{m})$
- Clock driver p-channel MOSFET:
$W/L = 8000/1.8\,(\mu\text{m}/\mu\text{m})$
- Clock driver n-channel MOSFET:
$W/L = 8000/1.8\,(\mu\text{m}/\mu\text{m})$

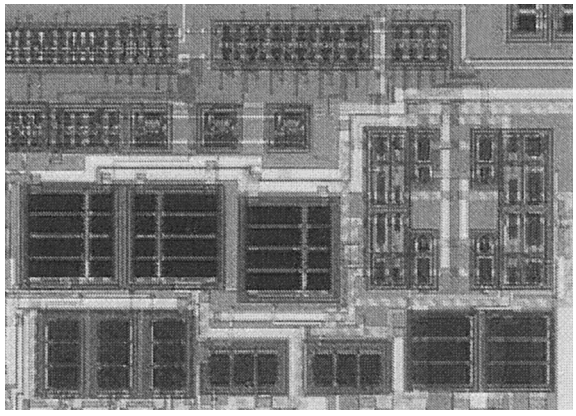

Fig. 17 Photograph of a positive 2.5-stage charge-pump circuit of TEG chip (3.99 mm × 4.35 mm).

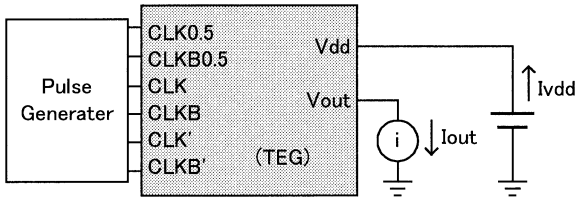

Fig. 18 Measurement set-up of the positive charge pump circuit.

An outline of our custom CMOS process used for fabrication of our proposed positive and negative charge-pump circuits in one chip [2] is given below. Note that the gate-source and drain-source voltage values in Tables 3, 4, 5, and 6 are used to determine the CMOS device (breakdown voltage) specification.
(i) A triple-well structure is used to be able to configure both positive and negative charge-pump circuits on one chip.
(ii) Both 30 V high-voltage MOSFETs [9]–[11] and 10 V LDD MOSFETs can be used in the same chip.
(iii) 30 V high-voltage MOSFETs with $T_{ox} = 910$ Å and $L = 5.0\,\mu$m are used for level shift circuits.
(iv) T_{ox} and L of the 10 V LDD MOSFETs are 440 Å and $1.8\,\mu$m, respectively, and they are used for clock drivers and charge transfer MOSFETs.

Figure 17 shows a photograph of a positive 2.5-stage charge-pump circuit of TEG chip.

6. Measured Results of Positive 2.5-Stage and Negative 1.5-Stage Charge-Pump Circuits

Figure 18 shows the equivalent circuit diagram of the TEG when we measured its efficiency η, where the current which flows from V_{dd} to the charge pump circuit consists of the followings:
(i) I_{in}: the input current from V_{in},
(ii) I_{dv}: the total current from the clock drivers into the charge pump circuit (i.e., $I_{dv} = I_{dv1} + I_{dv2}$),
(iii) I_{fcv}: the total current of clock driver circuits to

charge and/or discharge parasitic capacitances at external nodes.

We have obtained the efficiency η from measurements using the following equation:

$$\eta = \frac{V_{out} I_{out}}{V_{dd} I_{Vdd}} \tag{10}$$

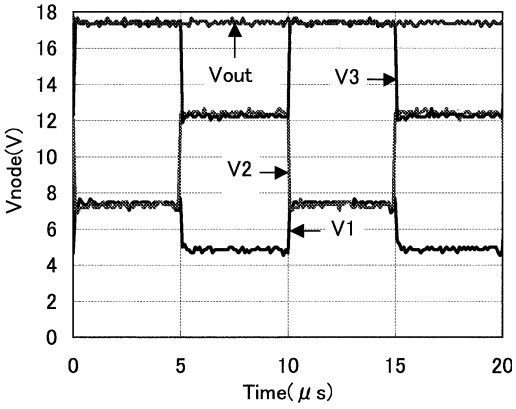

Fig. 19 Measured voltage waveforms of a positive 2.5-stage charge-pump circuit ($V_{dd} = 5\,\mathrm{V}$, $I_{out} = 0$).

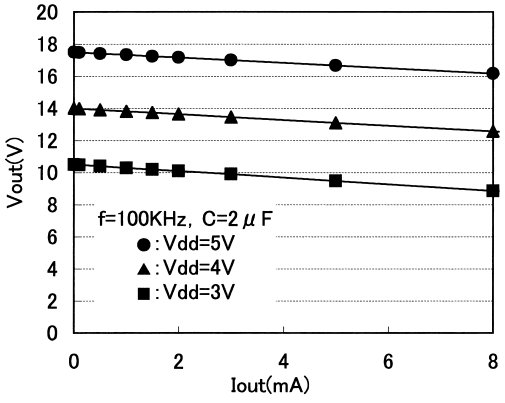

Fig. 20 Measured output voltage versus output current of a positive 2.5-stage charge-pump circuit.

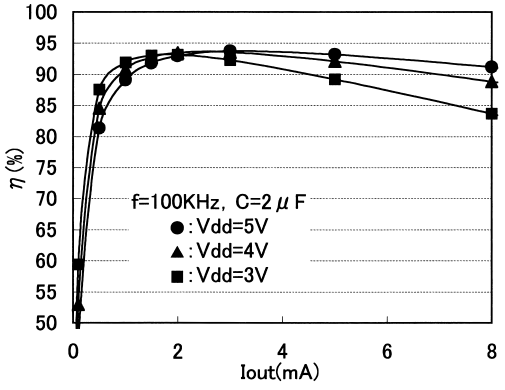

Fig. 21 Measured efficiency the efficiency before regulation versus output current of a positive 2.5-stage charge-pump circuit.

Here $I_{Vdd} = I_{in} + I_{dv} + I_{fcv}$

Figures 19, 20 and 21 show measured results of the positive 2.5-stage charge-pump circuit, while Figs. 22, 23 and 24 show those of the negative 1.5-stage charge-pump circuits. Figure 19 shows voltage waveforms at pumping nodes when $V_{dd} = 5\,\mathrm{V}$ and $I_{out} = 0\,\mathrm{mA}$, and we see that node V_1 is boosted by $0.5V_{dd}$ while nodes V_2 and V_3 are boosted by V_{dd}. Figure 20 shows the

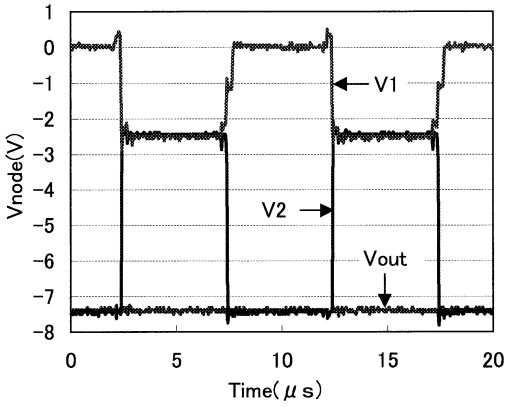

Fig. 22 Measured voltage waveforms of a negative 1.5-stage charge-pump circuit($V_{dd} = 5\,\mathrm{V}$, $I_{out} = 0$).

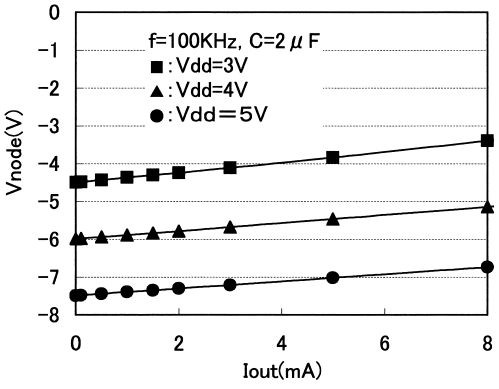

Fig. 23 Measured output voltage versus output current of a negative 1.5-stage charge-pump circuit.

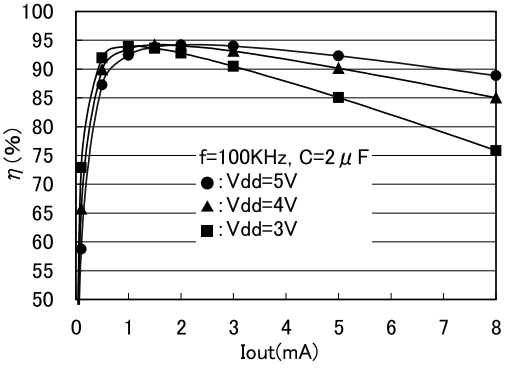

Fig. 24 Measured efficiency the efficiency before regulation versus output current of a negative 1.5-stage charge-pump circuit.

output voltage (V_{out}) with respect to the output current (I_{out}) while Fig. 21 shows the circuit efficiency before regulation; it is about 93% when $V_{dd} = 5\,\mathrm{V}$ and I_{out} ranges from 2 mA to 4 mA.

Figure 22 shows voltage waveforms at pumping nodes of a negative 1.5-stage charge-pump circuit, and we see that node V_1 is boosted by $-0.5V_{dd}$ while node V_2 is boosted by $-V_{dd}$. Figure 23 shows the output voltage (V_{out}) with respect to the output current (I_{out}) while Fig. 24 shows the circuit efficiency before regulation; it is about 93% when $V_{dd} = 5\,\mathrm{V}$ and I_{out} ranges from 2 mA to 4 mA.

The above measurement results give the validity to the values of the actual efficiency η'' in Table 2. Figures 21 and 24 show that the circuit efficiency in the small output current region is degraded; this is due to charge and discharge current losses associated with node parasitic capacitances, and its theoretical analysis is given in [12]. Note that we have to make the sizes of the charge transfer MOSFETs and the clock driver MOSFETs large in order to provide large output current (4 mA), however this results in relatively large parasitic capacitance at each pumping node which degrades the circuit efficiency. Thus we have to make their sizes small as much as possible to make node parasitic capacitance minimum while keeping the large current providing ability. Also note that external capacitors are used for the charge-pump circuits on our TEG chip because their output currents are in the order of several milli-Amperes (which is relatively large), and hence each pumping node suffers from parasitic capacitance of pads.

Therefore it is difficult to make their efficiency high for the output current (I_{out}) of less than 500 μA. Figure 24 shows the efficiency of the negative charge-pump deteriorates in the operating region where the output current is large (more than 5 mA). This is because the channel width of the p-channel MOSFET for $0.5V_{dd}$ generation switch was not sufficient in the TEG chip design and this can be improved in the next design.

Remark: The measured results here are only for $0.5V_{dd}$-step charge-pump circuits without regulator circuits. However, bias currents in regulator circuits can be designed to be negligibly small, and hence the total circuit efficiency (η') including regulator circuit can be estimated fairly accurately for a given V'_{out} from these measured data. For example, η' in Table 2 gives the total circuit efficiency of $0.5V_{dd}$-step charge-pump circuits for $V'_{out} = 6.5\,\mathrm{V}$ and $V_{dd} = 4.5\,\mathrm{V}$, 5.0 V or 5.5 V.

7. Conclusions

In this paper we have described a $0.5V_{dd}$-step pumping method for Dickson-type charge-pump circuits that achieves high overall circuit efficiency, including regulator circuitry, with large output current. This proposed method can significantly reduce the voltage drop between the target output voltage and the charge-pump output voltage (and hence reduce power loss) compared to a conventional charge-pump circuit, and hence it can improve the total efficiency; the output voltage of the conventional charge-pump circuit can be any of $2V_{dd}$, $3V_{dd}$, $4V_{dd}$, $5V_{dd}\cdots$ while that of a charge-pump circuit with our method can be any of $1.5V_{dd}$, $2V_{dd}$, $2.5V_{dd}$, $3V_{dd}$, $3.5V_{dd}\cdots$, and hence the voltage difference between charge-pump output voltage and any given target output voltage can be reduced by our method. To demonstrate the effectiveness of our proposed method, we have designed a 2.5-stage positive charge-pump circuit and a 1.5-stage negative charge-pump circuit using the $0.5V_{dd}$-step pumping method and fabricated them with our custom CMOS process. The $0.5V_{dd}$-step pumping method can be implemented with two capacitors which can be switched between series and parallel connection. Also internal node voltages provide gate-source voltages in all of the transfer MOSFETs in the charge-pump circuit so high efficiency [2] can be achieved. Measured results showed that efficiency of a 2.5-stage positive charge-pump circuit before regulation was better than 93% (power supply $V_{dd} = 5\,\mathrm{V}$, output voltage $V_{out} = 16.9\,\mathrm{V} \fallingdotseq 3.5V_{dd}$, output current $I_{out} = 4\,\mathrm{mA}$), and that of a 1.5-stage negative charge-pump circuit was 93% (power supply $V_{dd} = 5\,\mathrm{V}$, output voltage $V_{out} = -7.2\,\mathrm{V} \fallingdotseq -1.5V_{dd}$, output current $I_{out} = 4\,\mathrm{mA}$). Commercialization of our proposed charge-pump circuits has already been started.

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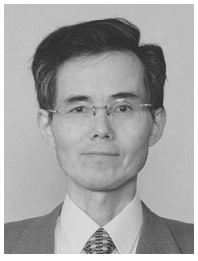

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