PAPER *Special Section on Analog Circuit Techniques and Related Topics*

Spread-Spectrum Clocking in Switching Regulators for EMI Reduction

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SUMMARY This paper describes a simple, inexpensive technique for intentionally broadening and flattening the spectrum of a DC-DC converter (switching regulator) to reduce Electro-Magnetic Interference (EMI). This noise spectrum broadening technique involves intentionally introducing pseudo-random dithering of control clock timing, which can be achieved by adding simple digital circuitry. This technique can significantly reduce noise power spectrum peaks at the DC-DC converter output. For our test case circuit, measurements showed that noise power was reduced by 5.7 dBm at the main peak, by 15.6 dBm at the second peak and by 12.8 dBm at the third peak. This simple, inexpensive technique can be applied to most conventional switching regulators by adding simple digital circuitry, and without any modification of the design of other parts.

key words: *switching regulator, DC-DC converter, spread spectrum, EMI, switching noise*

1. Introduction

Switching regulators are widely used—particularly in mobile equipment—as highly efficient DC-DC converters [1]. They consist of an input power supply V_{dd}, a power MOS switch, a choke coil (L), a capacitor (C), a diode (D) and PWM control circuitry (Fig. 1). To reduce the switching noise [2] that they generate, however, requires complex noise filtering and shielding which makes the switching power supply more costly and larger in size. This paper presents a technique for broadening and flattening their switching noise power spectrum to reduce Electro-Magnetic Interference (EMI) and to satisfy EMI regulations [3]. This technique involves pseudo-random dithering of the switching regulator control clock timing, and such clock jitter can be introduced by adding simple digital circuitry. This technique can significantly reduce noise power spectrum peaks at the DC-DC converter output.

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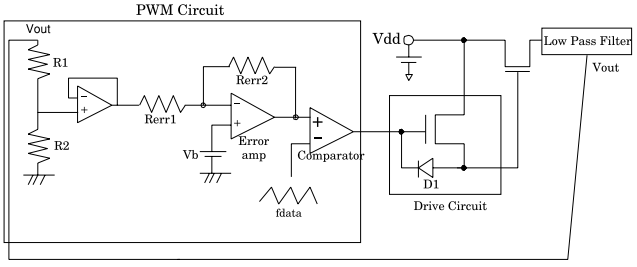

Fig. 1 A switching regulator (buck converter) with a PWM controller which sets the output voltage V_{out} to $(1 + R_2/R_1)V_b$. The minus input of the comparator is a ramp signal of a frequency f_{data}.

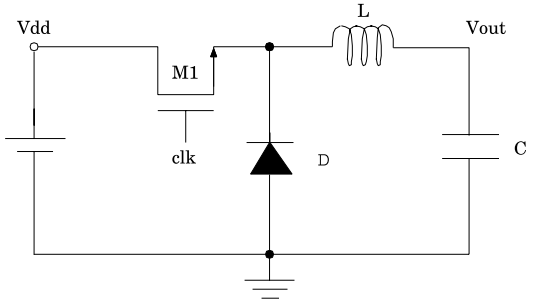

Fig. 2 A buck converter core circuit. V_{dd} is an input voltage, M1 is an MOS switch, *clk* is a control clock and L, C consist of a low pass filter. The value of the output voltage V_{out} is lower than the input voltage V_{dd} and is controlled by the duty of *clk*.

2. Switching Regulator

Figure 2 shows a voltage buck converter which consists of an input power supply V_{dd}, a power MOS switch, a diode (D), and a LC low-pass filter consisting of a choke coil (L) and capacitor (C) to smooth the output voltage V_{out}. Then we have

$$V_{out} \approx \frac{T_{on}}{T_{on} + T_{off}} V_{dd}, \tag{1}$$

where T_{on} is the switch ON time interval, and T_{off} is the switch OFF time interval. Since the output voltage is controlled by quickly turning the MOS switch on and off, high efficiency can be achieved. However, the choke coil L of the switching regulator generates

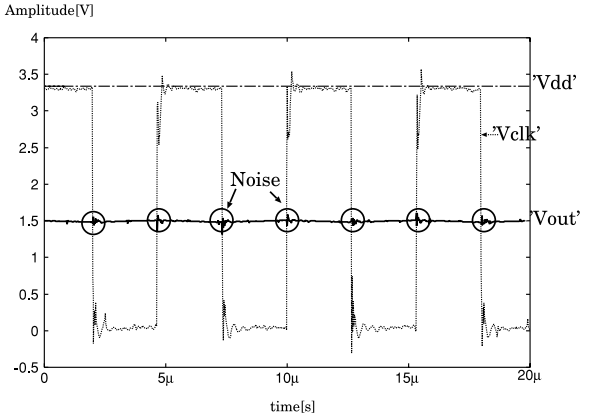

Fig. 3 Clock and output voltage waveforms (V_{clk} and V_{out} respectively) of a conventional switching regulator. We see that the output voltage V_{out} suffers from the switching noise at the rising and falling timings of V_{clk}.

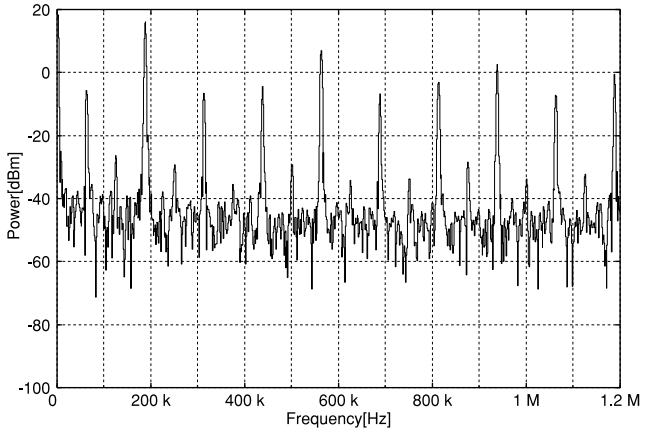

Fig. 4 Measured output power spectrum of a conventional switching regulator. We see that it has peaks at the multiples of the fundamental frequency.

$V = L(dI/dt)$ voltage transients (Fig. 3) when the switch turns on and off, so the switching noise power spectrum peaks are at multiples of the switching clock frequency (Fig. 4). As the switching frequency is increased (to reduce the size of choke coil and capacitor) and the size of portable equipment is reduced, this transient noise becomes more troublesome, and it becomes more difficult to satisfy EMI regulations [3] without costly and bulky shielding.

3. Proposed EMI Reduction Technique

3.1 Principle

We propose a digital Pseudo Random Modulation (PRM) technique to alleviate the above-described switching noise problem. This technique involves phase modulation (dithering) of the switching regulator control clock (Fig. 5) and spreads the noise power spectrum in the frequency domain to reduce EMI (Fig. 6).

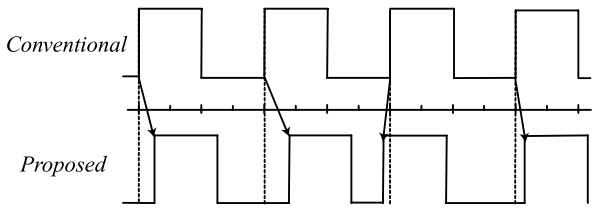

Fig. 5 Clock waveforms of conventional and proposed switching regulators. In the conventional one, the clock rising timing interval is constant, while in the proposed one it fluctuates in a pseudo random manner.

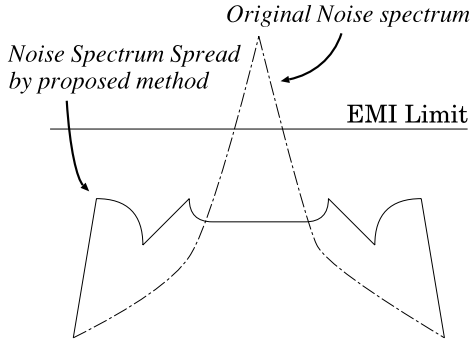

Fig. 6 Output voltage power spectrum of conventional and proposed switching regulators. The output power spectrum of the conventional one has peaks which may violate EMI regulations while the one of our proposed method spreads the noise peak power spectrum which helps to satisfy EMI regulations.

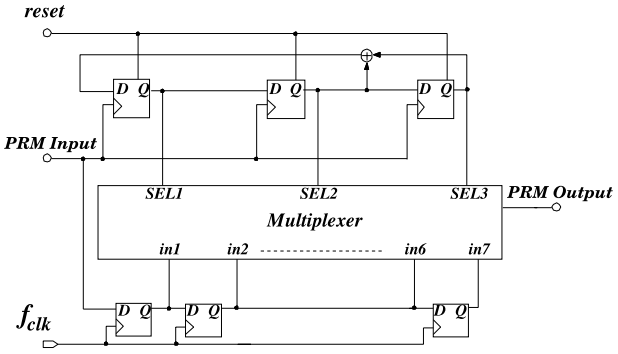

Fig. 7 Circuit implementation of the PRM when the number N of the M-sequence flip-flops is 3. The signal indicated by f_{data} is from the PWM controller output and the one indicated by "f_{clk}" is clock signal to produce the delayed signals of the "PRM Input" signal. The signal "PRM Output" goes to the switching regulator MOS gate, and the signal "reset" initializes the M-sequence circuit.

(However note that this technique does not reduce the total power of the switching noise.) This technique involves adding simple digital circuitry (Fig. 7), without any design modification of other parts. Usually clock jitter gives negative impacts to analog circuits [4], [5], but this technique utilizes it positively.

This proposed technique can be considered as the application of "Spread Spectrum Clocking (SSC)" (for synchronous digital circuits) [6]–[8] to switching reg-

ulators. However—because the switching clock frequency is just a few Megahertz—our PRM technique can use digital modulation, whereas the SSC technique has to use analog modulation because the clock frequency is very high (more than several hundred Megahertz). Note that it is easy to implement digital modulation circuitry that is little affected by CMOS process variations, operating temperature variations, and aging.

We note that the following merits are expected by spreading the noise spectrum in the switching regulator using the proposed method:

- The EMI level in the low frequency range (below several-hundred-kilo-hertz) measured especially with a "*quasi-peak detection method*" as well as with an "*average detection method*" [3], [9] can be reduced.
- Filter requirements for smoothing out the switching noise spectrum below a certain level can be relaxed because the noise peak spectrum is reduced by the proposed method.
- The proposed method can provide several positive effects in electromagnetic environments, e.g., the interference of the switching noise to AM radios can be reduced.

3.2 Circuit Implementation

Figures 7 and 8 show circuit implementation and timing chart for the PRM (Pseudo Random Modulation) technique; it consists of an N-bit M-sequence generator, a 2^N-bit shift-register and a (2^N-1)-to-1 multiplexer. The M-sequence generator is driven by the clock f_{data} (which is the same clock as the one used in the PWM controller) to produce a pseudo-random signal $SEL1, SEL2, ..., SEL(N)$. The shift-register is driven by the clock f_{clk} to delay the PWM controller output by n/f_{clk}, where $n = 1, 2, 3, ..., 2^N - 1$; the delay T_i of the i-th flip-flop output $IN(i)$ is i/f_{clk}. The data inputs of the multiplexer are $IN1, IN2, IN3, ..., IN(2^N-1)$, and its selector inputs are $SEL1, SEL2, ..., SEL(N)$. The multiplexer output drives the gate of the MOSFET switch. For example, when $IN2$ is selected as the multiplexer output, the switch is driven by the PWM output with $2/f_{clk}$ delay. Since the selection is done in a pseudo-random order, the multiplexer output is a PWM signal with pseudo-random phase modulation.

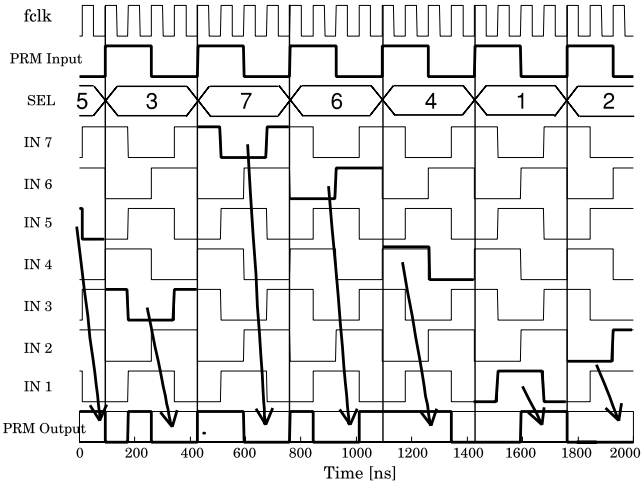

Fig. 8 Timing chart of the PRM circuit in Fig. 7. "Shift Register Control Clock" at the top corresponds to "f_{clk}" signal in Fig. 7 while "PRM input" signal corresponds to "f_{data}" signal in Fig. 7. Also "SEL" signal corresponds to SEL1, SEL2, SEL3 signals in Fig. 7 and "PRM output" corresponds to "OUTPUT" signal in Fig. 7.

If f_{clk} is much lower than $2^N f_{data}$, the output ripple of the switching regulator becomes very large. On the other hand, if f_{clk} is much higher than $2^N f_{data}$, then switching noise is not sufficiently spread in the frequency domain. From simulations and measurements, we have found that the following value of the shift register clock frequency f_{clk} is the best compromise:

$$f_{clk} \approx 2^N f_{data}. \tag{2}$$

Equation (2) can be also interpreted as follows: when the maximum delay of the multiplexer output from the PWM output equals the clock period $(1/f_{data})$ of the PWM controller, the noise spectrum is spread widely and output ripple is small.

In order to determine the number N of the M-sequence flip-flops, we have changed it and measured the maximum noise peak reduction. Then we have found that the best choice is N=5; this is because as N increases from 1 to 5 (one by one), the maximum noise power reduces significantly, but the reduction is almost the same between the cases for $N = 5$ and $N = 6$. On the other hand, as N increases, the PRM hardware as well as the shift register clock frequency f_{clk} have to increase.

The shift register control clock f_{clk} and the PWM clock f_{data} may be generated by a single oscillator and dividers.

4. Experimental Results

We have implemented the PRM circuit with an FPGA (ALTERA FLEX10K30EQC208-3), and applied it to a voltage buck converter (Fig. 9) and its experiment conditions are shown in Table 1.

Then we have compared the cases *with* and *without* the PRM circuit. Figure 10 shows the measured output power spectrum of a switching regulator *without* the PRM circuit, while Fig. 11 shows the spectrum *with* the PRM circuit. We see that the fundamental-frequency noise peak is reduced by 5.7 dBm, the second harmonic noise peak is reduced by 15.6 dBm, the third harmonic peak by 12.8 dBm, and as a whole, the maximum noise peak is reduced by 12.3 dBm. We see that the noise

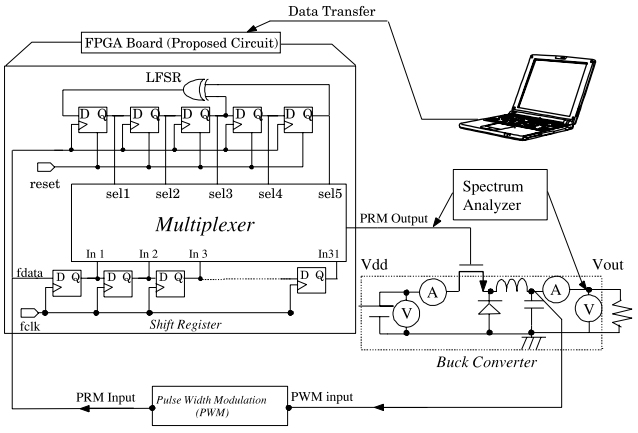

Fig. 9 Measurement setup of a buck converter system with the PRM circuit. A 5-bit M-sequence generator and a 32-bit shift register are used in the PRM circuit. A PC controls an Altera FPGA board and a spectrum analyzer measures the switching regulator output.

Table 1 Experiment conditions of the PRM circuit.

Shift register clock frequency f_{clk}	6 MHz
PWM clock frequency f_{data}	187 kHz
Number N of M-sequence flip-flops	5
Supply voltage	3.3 V

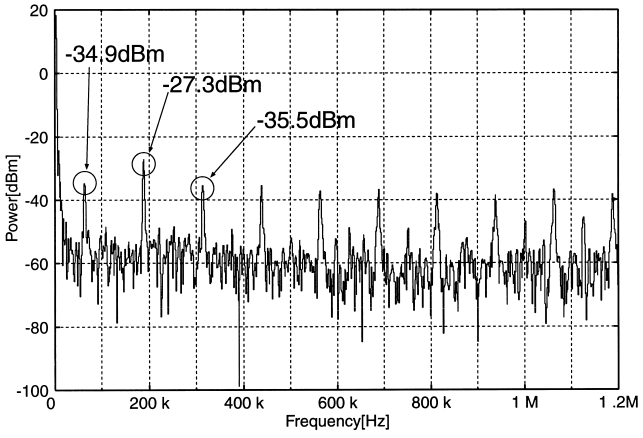

Fig. 10 Measured output power spectrum of the switching regulator *without* the PRM.

power spectrum peaks are significantly reduced. Figure 12 show the measured output voltage the switching regulator *with* and *without* the PRM, while Fig. 13 shows the measured output efficiency of the switching regulator *with* and *without* the PRM. (The power consumption of the PRM circuit as well as the PWM controller is not taken into account here because it is small CMOS digital hardware and its power consumption is negligible when implemented as a fraction of digital VLSI chip.) We see that the addition of the PRM does not significantly affect the output voltage and efficiency. We note that additional measurement

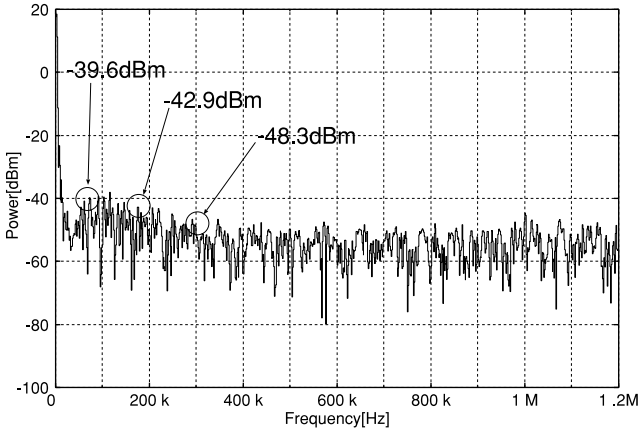

Fig. 11 Measured output power spectrum of the switching regulator *with* the PRM. We see that the noise power peaks are reduced compared to the ones in Fig. 10.

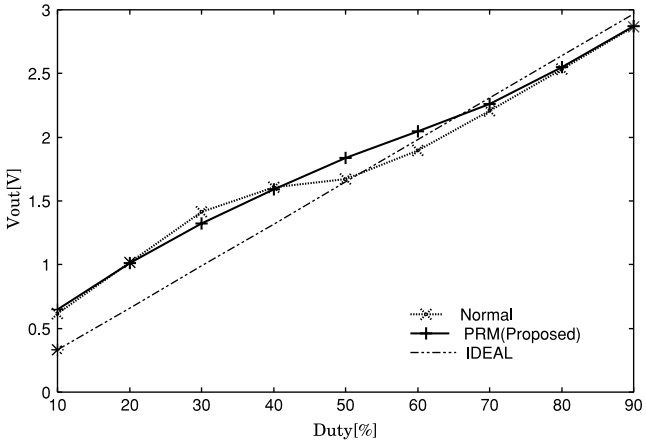

Fig. 12 Measured output voltages of a buck converter *with* and *without* the PRM with respect to the clock duty. The line of "Normal" indicates the output voltage *without* the PRM while the line of "PRM (Proposed)" indicates the one *with* the PRM. We see that in both cases the output voltages are almost the same and hence adding the PRM circuitry does not affect the output voltage. Note that the line of "IDEAL" shows the output voltage calculated using Eq. (1).

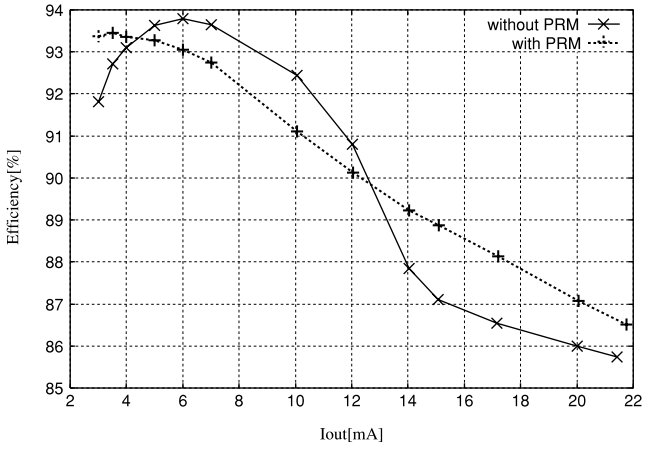

Fig. 13 Measured efficiencies of a buck converter *with* and *without* the PRM. The power consumption of the PRM circuit as well as the PWM controller is not taken into account here.

results using a standard EMI measurement system in an electro-magnetic shield room (anechoic chamber) are reported in [10].

5. Concluding Remarks

We have proposed a spread-spectrum clocking technique for switching regulators involving digital pseudo-random modulation of the switch control clock. Its effectiveness has been demonstrated by prototype implementation and its measurements, and it has the following advantages:
(i) **Small hardware requirement, low cost, low power:** The proposed technique can be implemented simply by adding a small low-cost, low-power-consumption digital circuit.
(ii) **Universality:** This technique can be applied to almost all types of switching regulator (e.g. not only voltage buck converters but also voltage boost converters).
(iii) **Compatibility:** There is no need to modify conventional switching regulator circuit design; simply add a small digital circuit. Also the proposed technique can be employed together with other conventional noise reduction techniques.
(iv) **Stability:** Since digital modulation is used, this is virtually unaffected by temperature variations, aging or CMOS process variations.
(v) **Flexibility:** Since digital modulation is used, not only pseudo-random phase modulation but also other types of modulation (such as frequency modulation) can readily be implemented.

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References

[1] A.J. Stratakos, C.R. Sullivan, S.R. Sanders, and R.W. Broderson, "High-efficiency low-voltage DC-DC conversion for portable applications," in Low-Voltage/Low-Power Integrated Circuits and Systems, Chapter 12, IEEE Press, 1999.
[2] S. Sakiyama, J. Kajiwara, M. Kinoshita, K. Satomi, K. Ohtani, and A. Matsuzawa, "An on-chip high-efficiency and low-noise DC/DC converter using divided switches with current control technique," ISSCC Digest of Tech. Papers, pp.156–157, Feb. 1999.
[3] International Special Committee on Radio Interference, CISPR16-I: Specification for Radio Disturbance and Immunity Measuring Apparatus and Methods, Part 1, International Electro-technical Commission, First edition, Geneva, Switzerland, 1993.
[4] H. Kobayashi, K. Kobayashi, M. Morimura, Y. Onaya, Y. Takahashi, K. Enomoto, and H. Kogure, "Sampling jitter and finite aperture time effects in wideband data acquisition systems," IEICE Trans. Fundamentals, vol.E85-A, no.2, pp.335–346, Feb. 2002.
[5] N. Kurosawa, H. Kobayashi, H. Kogure, T. Komuro, and H. Sakayori, "Sampling clock jitter effects in digital-to-analog converters," Measurement, vol.31, no.3, pp.187–199, March 2002.
[6] C.D. Hoekstra, "Frequency modulation of system clocks for EMI reduction," Hewlett-Packard Journal, Article 13, pp.101–107, Aug. 1997.
[7] H.-S. Li, Y.-C. Cheng, and D. Puar, "Dual-loop spread spectrum clock generator," ISSCC Digest of Tech. Papers, pp.184–185, Feb. 1999.
[8] Y. Moon, D.-K. Jeong, and G. Kim, "Clock dithering for electromagnetic compliance using spread spectrum phase modulation," ISSCC Digest of Tech. Papers, pp.186–187, Feb. 1999.
[9] C.R. Paul, Introduction to Electromagnetic Compatibility, Mimatsu Data System, 1996.
[10] H. Sadamura, M. Namekata, M. Kono, H. Kobayashi, and N. Ishikawa, "EMI reduction and measurement techniques of switching regulators," IEEJ Technical Meetings of Electronic Circuits, ECT-02-117, Tokyo, Dec. 2002.

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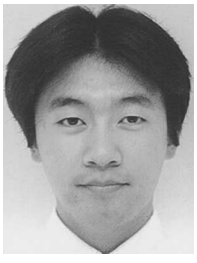

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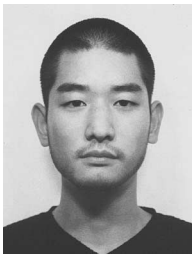

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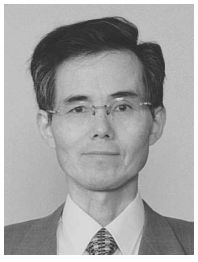

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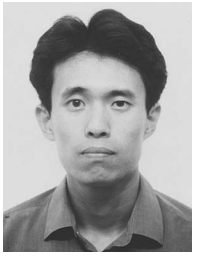

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