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Reducing Startup-Time Inrush Current in Charge-Pump Circuits

Takao MYONO[†a)], ***Member***, **Yoshitaka ONAYA**[††], **Kenji KASHIWASE**[†††], ***Nonmembers***, **Haruo KOBAYASHI**[†††], ***Member***, **Tomoaki NISHI**[††], **Kazuyuki KOBAYASHI**[†], **Tatsuya SUZUKI**[†], ***and*** **Kazuo HENMI**[†], ***Nonmembers***

SUMMARY We have developed a high-efficiency charge-pump power supply circuit with large output current capability for mobile equipment. However, during the commercialization phase, we found that the large inrush current of 270 mA at charge-pump circuit startup-time could cause problems. In this paper we analyze the mechanism that causes this inrush current, and we propose circuitry to reduce it. We show SPICE simulation and measurement results for our proposed circuitry that confirm its effectiveness. By incorporating this circuitry, startup-time inrush current was reduced to 30 mA.

key words: *charge-pump circuit, inrush current, DC-DC converter, high-voltage generator circuit, power supply circuit*

1. Introduction

Recent video products such as digital video cameras, digital still cameras (DSCs), and DSC phones incorporate charge coupled devices (CCDs) for video image acquisition, and their driver circuits require power supply circuits that generate positive and negative high-voltages (more than 10 V) with large output currents (several mA). In most cases, switching regulators are used to generate these high -voltages because they can provide large output currents with high-efficiency. However, they require off-chip coils, and also generate considerable switching noise [1]. On the other hand, Dickson charge-pump circuits (which consist of capacitors and switches) are another candidate for mobile equipment power supply circuits. They do not require coils, and generate relatively little noise. However conventional charge-pump circuits suffer from low efficiency and small output current drive capability [2], [3].

With this in mind, we have improved conventional Dickson charge-pump circuits and developed new ones which can provide large output currents (several mA) with high-efficiency (approx. 90%) [4], [5]. However, while attempting to commercialize them, we found that the large inrush current at charge-pump circuit startup-time would cause problems. The reason for this large inrush current is as follows: our charge-pump circuit uses relatively large off-chip capacitors to provide large output currents, but the capacitors are not fully charged before the circuit starts operation. Charging of the capacitors begins after the input voltage and clock signals are provided. The resultant large (inrush) current continues to flow to charge the capacitors from operation startup until the circuit reaches steady state. Note that this large inrush current may cause a relatively large drop in the input supply voltage V_{dd}, which could lead to malfunctioning of some peripheral circuits in mobile equipment.

In this paper, we analyze the mechanism that causes this startup-time inrush current, and propose circuitry to reduce it; we show the effectiveness of our solution by means of SPICE simulations and measurements of the actual chip implementation.

2. Prototype Charge-Pump Circuit

Figure 1 shows the prototype charge-pump circuit that we have developed previously [5], which is a three-stage booster circuit and consists of a pump block and a regulator block. M1, M2, M3, M4 in the pump block are charge-transfer MOSFETs, C1, C2, C3 are pump capacitors, C4 is an output voltage smoothing capacitor, P1, P2, P3 are pump drivers that boost each node voltage, S's are level-shift circuits, and K1, K2 are clock drivers that provide on/off control of the charge-transfer MOSFETs. Also V_{ref} at the input of the operational amplifier in the regulator block is a reference voltage.

The main specifications of our charge-pump circuit are:
(1) V_{dd} = 3.3±0.3 V
(2) V'_{out} = 13 V±0.5 V
(3) I'_{out} = 5 mA

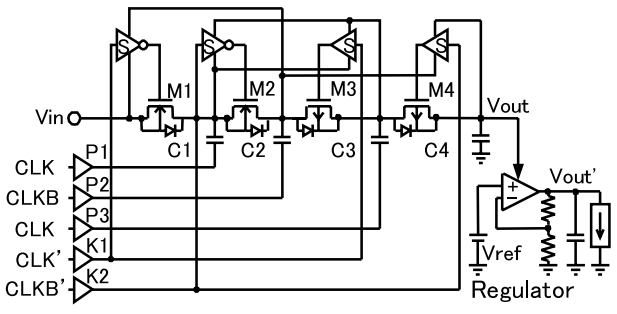

Fig. 1 Prototype charge-pump circuit diagram.

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[†]The authors are with Semiconductor Company, Sanyo Electric Co., Ltd., Gunma-ken, 370-0596 Japan.
[††]The authors are with Sanyo LSI Design-System Soft Co., Ltd., Gunma-ken, 370-0596 Japan.
[†††]The authors are with the Department of Electronic Engineering, Gunma University, Kiryu-shi, 376-8515 Japan.
a) E-mail: myon003877@sanyo.co.jp

(4) C1, C2, C3, C4 = 0.1 μF (off-chip).

The sizes of the MOSFETs used in the circuit are

(1) Charge-transfer MOSFETs (M1, M2, M3, M4):

PMOS: W/L= 4000 μm/1.8 μm

NMOS: W/L = 2000 μm/1.8 μm

(2) Pump driver MOSFETs:

PMOS: W/L = 10000 μm/1.8 μm

NMOS: W/L = 5000 μm/1.8 μm.

The features of the circuit that result in large output current capability and high-efficiency are as follows:

(1) For each MOSFET M1, M2, M3 and M4, the body and drain are connected to avoid high-voltage (beyond the breakdown voltage) being applied between gate and body.

(2) For each MOSFET M1, M2, M3 and M4, the gate-source voltage V_{gs} is applied from the corresponding level-shift circuit and it is twice the supply voltage V_{dd}.

We also note that the charge-transfer MOSFETs conduct current at startup-time from V_{in} to V_{out} through parasitic diodes, and this current determines the initial voltage at each node. This current flow stops after clock signals are applied and voltages of each node are boosted.

3. Simulation of Prototype Charge-Pump Circuit, and Inrush Current Measurement

This section shows the simulated and measured inrush current waveforms in the prototype charge-pump circuit of Fig. 1 (where no inrush current reduction measures were taken).

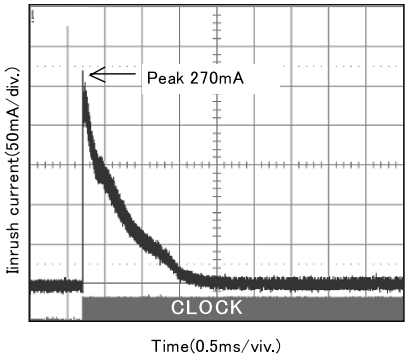


Fig. 2 Measured waveform of the inrush current at startup-time.

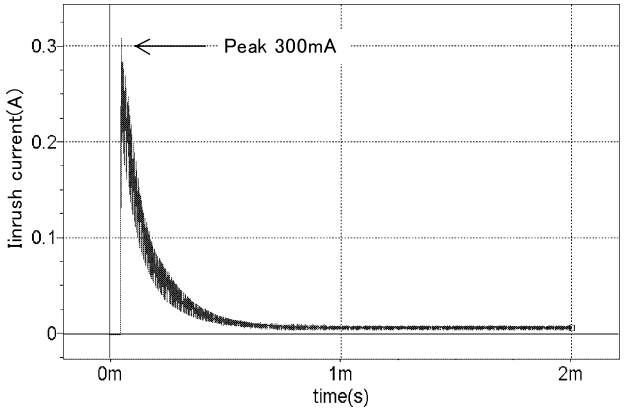


Fig. 3 SPICE simulation waveform of the inrush current.

Figure 2 shows the measured inrush current waveform of the circuit of Fig. 1. We see that the peak value of the inrush current is 270 mA, and this inrush current consists of current from the input V_{in} and current from the pump drivers. We found that the inrush current is independent of the clock frequency, where duty cycle is 50%.

Figure 3 shows the inrush current SPICE simulation results in Fig. 1, and the peak value is 300 mA.

We found that the peak value of the inrush current depends on the values of pump capacitors C1, C2, C3, C4 as well as the on-resistance values of the charge-transfer and pump driver MOSFETs. It also depends on the area of the parasitic diode associated with each charge-transfer MOSFET. In our SPICE simulation, we used the following values for each parasitic diode:

$$AS = AD = 1 \times 10^{-8}\,(\mathrm{m}^2)$$
$$PS = PD = 1 \times 10^{-3}\,(\mathrm{m})$$

where AS and AD represent the areas of the source and drain of the MOSFET, respectively, and PS and PD represent their perimeters respectively. Slight discrepancies are observed between the SPICE-simulated and measured results; however, they are within acceptable limits, and we see that the analysis using SPICE simulation is very effective.

4. Analysis of Inrush Current Paths

In this section we will clarify the paths of the inrush current flow and confirm them using SPICE simulations. We found that the paths of the inrush current are as shown in Fig. 4.

– When CLK = low, CLKB = high: Current paths from ① and ③

– When CLK = high, CLKB = low: Current paths from ② and ④

Figure 5 shows a parasitic diode associated with an n-channel charge-transfer MOSFET, and there are two inrush current paths in the charge-transfer MOSFET. One is from

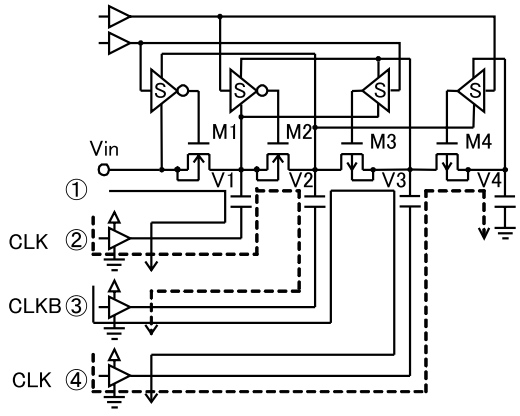


Fig. 4 Inrush current paths.

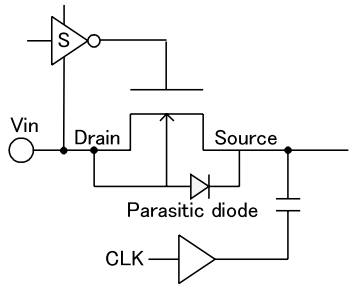
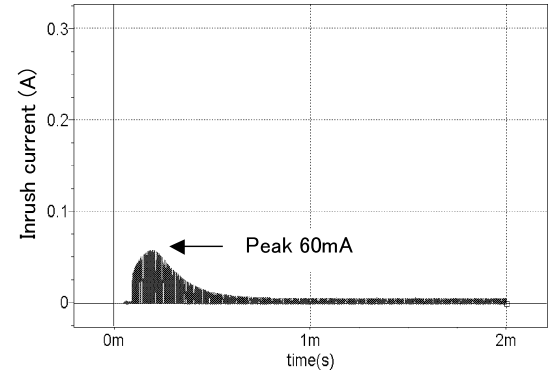
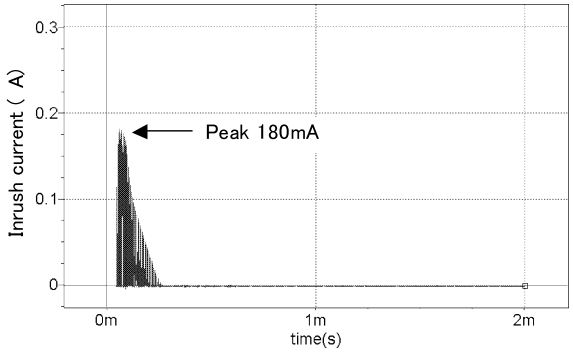


Fig. 5 Parasitic diode of an *n*-channel charge-transfer MOSFET.



(a) Drain-source current



(b) Parasitic diode current

Fig. 6 Waveforms of inrush current simulations.

the drain to the source of the charge-transfer MOSFET and the other is the parasitic diode that exists between the body and the source of the charge-transfer MOSFET. (Note that the parasitic diode is forward-biased when the charge-pump starts up.) Figure 6 shows SPICE simulation results for the inrush currents that flow along the two paths, and we see that the peak values of the inrush currents are 60 mA and 180 mA, respectively; a larger inrush current flows through the parasitic diode than through the path from the drain to the source of the MOSFET. We consider that there is no way to prevent the inrush current from flowing through this parasitic diode, and hence inrush current could not be reduced by modification of the charge-transfer part.

5. Proposed Circuit for Reducing Inrush Current

In this section we propose a circuit that reduces inrush current and show a SPICE simulation and measured results for it.

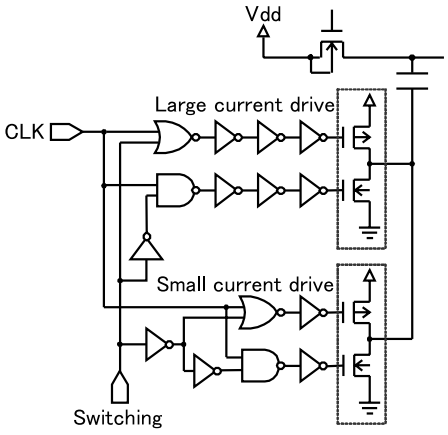


Fig. 7 Proposed circuit for reducing inrush current.

According to the analysis in Sect. 4 (Fig. 4), we found that the inrush currents that are fed into capacitors also flow into/from the pump drivers, and the parasitic diodes in the pump drivers are never forward-biased. Thus we considered that startup-time inrush current could be reduced by modification of the pump drivers. More specifically, at startup-time we can increase the impedance of the pump drivers to reduce the inrush current, and after a while, when the charge-pump circuit operation becomes stable, we decrease their impedance for large output current drive capability.

Figure 7 shows the main part of our proposed circuit (which implements the above idea) for reducing inrush current, and this circuit includes both pump drivers with small drive capability (used at startup-time) and those with large drive capability (used for normal operation) connected in parallel. At startup-time, only the pump drivers with small drive capability are enabled, and those with large drive capability are disabled; this ensures that only small currents can flow from the pump drivers to the pump capacitors, and hence this reduces the inrush current. When the pump capacitors are charged to a certain level, we disable the pump drivers with low drive capability and enable those with high drive capability for normal operation.

The MOSFET sizes of the pump drivers are given below:

(1) The pump drivers with large drive capability
PMOS: $W/L = 10000\,\mu\text{m}/1.8\,\mu\text{m}$
NMOS: $W/L = 5000\,\mu\text{m}/1.8\,\mu\text{m}$

(2) The pump drivers with small drive capability
PMOS: $W/L = 1200\,\mu\text{m}/1.8\,\mu\text{m}$
NMOS: $W/L = 600\,\mu\text{m}/1.8\,\mu\text{m}$

Figure 8 shows the configuration of the charge-pump circuit with the startup-time inrush current reduction circuitry, and Fig. 9 shows a hysteresis comparator circuit used there.

In Fig. 8, the comparator compares the supply voltage V_{dd} with the node voltage V_a in the regulator to determine whether the small or large drive capability pump drivers are

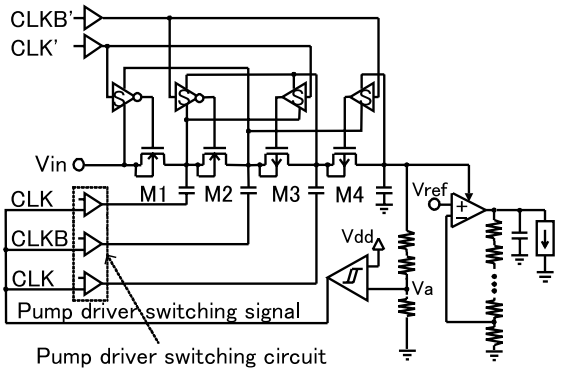


Fig. 8 Complete charge-pump circuit with the proposed inrush current reduction circuitry.

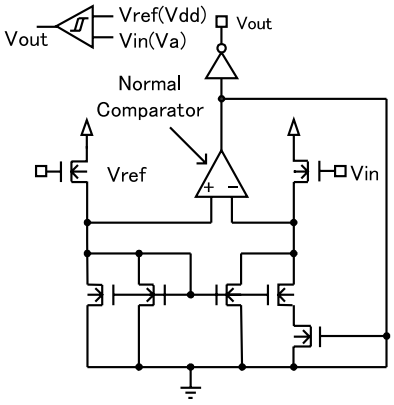


Fig. 9 Hysteresis comparator.

used. Note that $V_a < V_{dd}$ applies at startup-time and the small drive capability pump drivers are used. After clock signals are applied and the output voltage of the charge-pump increases sufficiently, $V_a > V_{dd}$ applies and the large drive capability pump drivers are used for normal operation. The hysteresis comparator compares these voltages of V_{dd} and V_a, and generates a switching signal to determine which pump driver is used. This proposed circuit is rather insensitive to the voltage drift of V_{dd} because V_{dd} and V_a (which is proportional to V_{dd}) are compared. According to our specifications for the charge-pump power supply circuit, it provides no output current during the 100ms after the circuit starts to operate, and this allows us to use the pump drivers with small drive capability to charge the pump capacitors at startup-time.

Figure 10 shows SPICE simulation results for inrush current of the circuit in Fig. 8.

We have implemented, for commercial use, a charge-pump power supply LSI that incorporates our proposed inrush current reduction circuit. Figure 11 shows measured inrush current results for it, and the measured peak inrush current is 30 mA, which is quite satisfactory for our requirements. We also confirmed by measurement that this amount of inrush current is not problematic for peripheral circuits.

We remark that many of DC-DC converters (such as

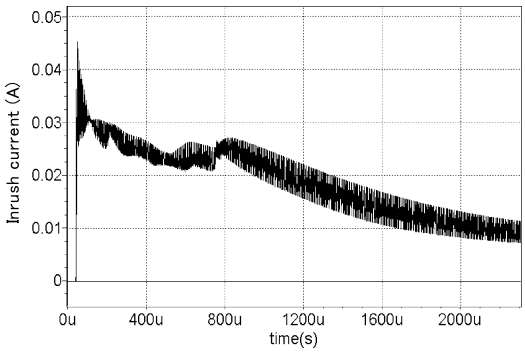


Fig. 10 SPICE simulation results for inrush current of the circuit in Fig. 8.

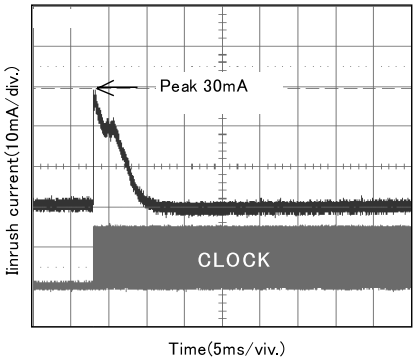


Fig. 11 Measured inrush current results.

switching regulators) which prevail in the market today, takes approximately 100 msec at startup-time in order to take care of the inrush current problem. The proposed method used in our charge-pump circuit takes less time (less than 10 msec) to do that, and hence the time increase to reach the steady state at the startup is not a problem for practical use. Also note that startup occurs at one and its time is relatively short so that the efficiency reduction during this time is not a problem.

6. Conclusions

In this paper we have analyzed the startup-time inrush current of a charge-pump circuit and proposed circuitry to reduce it. We have verified the effectiveness of our proposed circuitry through SPICE simulations and measurements of the actual chip implementation. Our measurements showed that the inrush current of the charge-pump circuit was reduced significantly from 270 mA to 30 mA when our proposed circuitry was used.

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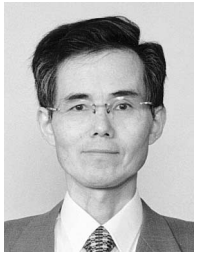

Takao Myono graduated from Kumagaya Technical High School in 1964. In 1964 he joined Sanyo Electric Corporation, Semiconductor Company, Gunma, Japan. From 1965 to 1968 he studied at Ibaraki University, Japan, and obtained the Ph.D. degree in electronic engineering from Gunma University in 2002. From 1968 to 1976 he was engaged in the design of PMOS and CMOS logic LSIs, and from1976 to 1995 he was involved in the development of CAD systems. Currently he is Senior Manager of Advanced Technology Business Unit, Semiconductor Company, Sanyo Electric Co., Ltd. His research interests include analog integrated circuit design.

Yoshitaka Onaya received the B.S. degree in electronic engineering from Gunma University in 1999. In 1999 he joined Sanyo LSI Design-System Soft Co., Ltd., Central Development Center, Gunma, Japan. Since 1999, he has been working on the development of analog CMOS integrated circuits.

Kenji Kashiwase received the B.S. degree and is expected to receive the MS degree in electronic engineering from Gunma University in 2002 and 2004 respectively. Currently he is a graduate student there and has been involved in research for analysis and design of charge pump and mixer circuits.

Haruo Kobayashi received the B.S. and M.S. degrees in information physics from University of Tokyo in 1980 and 1982 respectively, the M.S. degree in electrical engineering from University of California at Los Angeles (UCLA) in 1989, and the Dr. Eng. degree in electrical engineering from Waseda University in 1995. He joined Yokogawa Electric Corp. Tokyo, Japan in 1982, where he was engaged in the research and development related to measuring instruments and mini-supercomputers. From 1994 to 1997, he was involved in research and development of ultra-high-speed ADCs/DACs at Teratec Corp. In 1997 he joined Gunma University and presently is a Professor in Electronic Engineering Department there. He was also an adjunct lecturer at Waseda University from 1994 to 1997. His research interests include mixed-signal integrated circuits design and signal processing algorithms. He received Yokoyama Award in Science and Technology in 2003 and the Best Paper Award from the Japanese Neural Network Society in 1994.

Tomoaki Nishi received the B.S. and M.S. degrees in electronics from Nagaoka University of Technology, Niigata, Japan in 1985 and 1987. In 1987 he joined Shindengen Electric Manufacturing Co. Ltd., Semiconductor Division, Saitama, Japan. In 1998 he joined Sanyo LSI Design-System Soft Co., Ltd., Central Development Center, Gunma, Japan. Since 1998, he has been working on the development of analog ICs for switching power supply.

Kazuyuki Kobayashi received the B.S. and M.S. degrees in electronic engineering from Gunma University in 1994 and 1996 respectively. In 1996, he joined Sanyo Electric Corporation, Semiconductor Company, Gunma, Japan. He worked at the department of CMOS Device Engineering for seven years. Since 2002, he has been working on the development of analog CMOS integrated circuits.

Tatsuya Suzuki received the B.S. degree in electronics from Nihon University College of Science and Technology, Tokyo, Japan in 1986. In 1986 he joined Fuji Heavy Industries Ltd. (SUBARU), Automobile Division, Gunma, Japan. In 1991 he joined Sanyo Electric Corporation, Semiconductor Company, Gunma, Japan. Since 1991, he has been working on the development of analog CMOS integrated circuits.

Kazuo Henmi received the B.S. and M.S. degrees in applied physics from Tohoku University in 1994 and 1996 respectively. In 1996, he joined Sanyo Electric Corporation, Semiconductor Company, Gunma, Japan. He worked at the department of CMOS Device Engineering for seven years. Since 2002, he has been working on the development of analog CMOS integrated circuits.