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A Noise-Shaping Algorithm of Multi-bit DAC Nonlinearities in Complex Bandpass ΔΣAD Modulators

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SUMMARY This paper presents a technique for improving the SNR and resolution of complex bandpass ΔΣADCs which are used for wireless communication systems such as cellular phone, wireless LAN and Bluetooth. Oversampling and noise-shaping are used to achieve high accuracy of a ΔΣAD modulator. However when a multi-bit internal DAC is used inside a modulator, nonlinearities of the DAC are not noise-shaped and the SNR of the ΔΣADC degrades. For the conversion of complex intermediate frequency (IF) input signals, a complex bandpass ΔΣAD modulator can provide superior performance to a pair of real bandpass ΔΣAD modulators of the same order. This paper proposes a new noise-shaping algorithm—implemented by adding simple digital circuitry—to reduce the effects of nonlinearities in multi-bit DACs of complex bandpass ΔΣAD modulators. We have performed simulation with MATLAB to verify the effectiveness of the algorithm, and the results show that the proposed algorithm can improve the SNR of a complex bandpass ΔΣADC with nonlinear internal multi-bit DACs.

key words: *complex bandpass ΔΣAD modulator, bandpass filter, noise-shaping, ADC, DAC, element rotation, data-weighted averaging, low-IF receiver*

1. Introduction

Recently, research into bandpass ΔΣADCs has become popular for their applications to RF receivers in wireless communication systems such as cellular phone, wireless LAN and Bluetooth [1]–[5]. Shifting the ADC towards the antenna side in the receiver architecture relaxes the requirements placed on analog circuits at the expense of more complicated digital circuit, allowing more digital integration of analog function on a single chip, and resulting in a cheaper system with a higher level of integration. However, ADCs with high linearity, large dynamic range, bandwidth and strong image rejection capabilities are required, and a complex bandpass ΔΣADC is one of their candidates.

In communication systems applications using complex intermediate frequency (IF) input signals, image signals caused by mismatches between I and Q paths may adversely affect system performance, and a complex bandpass ΔΣAD modulator [1]–[6] can provide better suppression of image signals and thus superior performance to a pair of real bandpass ΔΣAD modulators of the same order. Also especially in low-IF receivers, it is known [3] that the complex bandpass ΔΣAD modulator relaxes the performance requirement (such as sampling speed) over a pair of real bandpass ΔΣAD modulators.

In ΔΣAD modulators, oversampling and noise shaping techniques are used to achieve high accuracy. When a single-bit modulator (i.e., internal ADC and DAC are 1-bit) is used to achieve high SNR, higher oversampling ratio (OSR) is needed which demands higher sampling rate, and/or a high-order filter inside a modulator (as well as a high-order digital filter following the ΔΣAD modulator) is required which may cause modulator stability problems. On the other hand, when a multi-bit ΔΣ modulator is used, higher resolution can be achieved with lower OSR, and the stability problems are alleviated [7], [8].

A multi-bit DAC cannot be made perfect linear, while a 1-bit DAC is inherently linear. Multi-bit DAC nonlinearity is equivalent to errors added directly to the input signal - it is not reduced by noise-shaping, and hence they may degrade the SNR of the ΔΣADC. The input and output of a bandpass ΔΣAD modulator shown in Fig. 1 are given by

$$M(z) = \frac{H(z)}{1+H(z)}\left[X(z) + \frac{1}{H(z)}E(z) + \frac{1}{H(z)}\delta(z)\right] \quad (1)$$

$$Y(z) = \frac{H(z)}{1+H(z)}\left[X(z) + \frac{1}{H(z)}E(z) - \delta(z)\right]. \quad (2)$$

Here the signal part $S(z)$ and the noise part $N(z)$ are defined as:

$$S(z) := \frac{H(z)}{1+H(z)}X(z)$$

$$N(z) := \frac{H(z)}{1+H(z)}\left[\frac{1}{H(z)}E(z) - \delta(z)\right]. \quad (3)$$

From Eq. (3), we see that nonlinearity errors $\delta(z)$ of DAC directly appears at output of the modulator without noise-shaping, while internal quantization noise $E(z)$ of ADC is noise-shaped by $1/H(z)$; this makes it difficult to realize a high resolution ADC.

One way to overcome this multi-bit DAC nonlinearity problem is (self-)calibration of the multibit DAC, and another way is to use signal processing algorithms to noise-shape the multi-bit DAC nonlinearities. There are already some algorithms for noise-shaping of multi-bit DAC nonlinearities in bandpass ΔΣAD modulators, such as dynamic element matching (DEM) [8] and element rotation (data-weighted averaging) [9]. However either of them is for *real* bandpass ΔΣAD modulators (single-input & output only)

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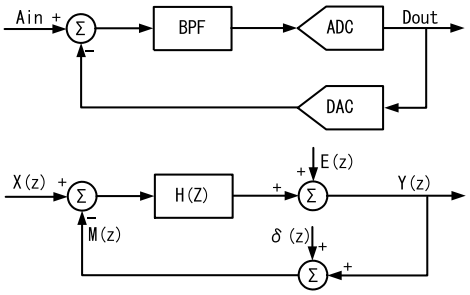

Fig. 1 A bandpass ΔΣAD modulator and its equivalent block diagram. $X(z)$ (Ain) is an analog input, $Y(z)$ (Dout) is a digital output, $E(z)$ is quantization noise of an ADC, and $\delta(z)$ is nonlinearity of a DAC.

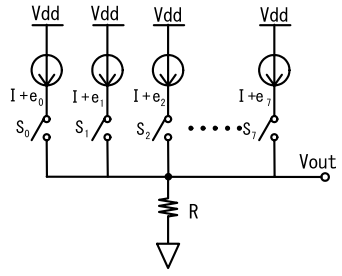

Fig. 2 A current-steering segmented DAC with 9-level resolution. Here $e_0, e_1, \ldots e_6$ and e_7 denote current source mismatches.

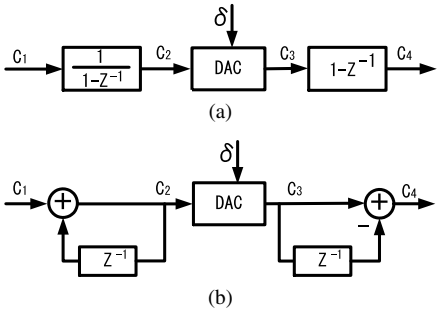

Fig. 3 (a) Lowpass element rotation architecture. (b) Equivalent block diagram.

shown in Fig. 1. This paper presents a new algorithm which noise-shapes nonlinearities of multi-bit DACs in a *complex* bandpass ΔΣAD modulator which has I, Q inputs and outputs. Adding simple digital circuitry can provide first-order complex bandpass noise-shaping of nonlinearities of multi-bit DACs, and improve the SNR of a multi-bit complex bandpass ΔΣADC. Our simulation results with MATLAB show the proposed method can improve the SNR and resolution of complex bandpass ΔΣADCs.

Section 2 reviews DAC nonlinearity noise-shaping algorithms (element rotation methods) for lowpass and highpass modulators with single-input & output, based on [9], [12]. Section 3 describes our proposed DAC nonlinearity noise-shaping algorithm for complex bandpass modulators, and Sect. 4 shows its MATLAB simulation results. Finally Sect. 5 provides conclusion.

Throughout this paper, we assume, without loss of generality, that internal DACs in ΔΣAD modulators have 9-level resolution; their digital input takes the value of 0, 1, 2, ..., 7, or 8. We also suppose that they are implemented with the segmented current-steering DAC architecture [14].

2. DAC Nonlinearity Noise-Shaping Algorithms in Lowpass and Highpass Modulators

In this section, we will describe element rotation (data-weighted averaging: DWA) first-order noise-shaping algorithms of DAC nonlinearities in (single-input & output) lowpass and highpass modulators [9], [12], which will be used for the algorithm derivation for complex bandpass modulators in Sect. 3.

2.1 Normal Segmented DAC and Unit Cell Mismatches

A normal segmented current-steering DAC with 9-level resolution in Fig. 2 consists of 8 unit-current-cells and a resistor. We denote I_k for the current of k-th unit-current-cell ($k = 0, 1, 2, \ldots, 7$). Ideally all currents I_k ($k = 0, 1, 2, \ldots, 7$) should be equal, however in practice they can be slightly different due to such as process variation inside an IC chip. Let

$$I_k := I + e_k \quad (k = 0, 1, 2, \ldots, 7).$$

Here

$$I := \big(I_0 + I_1 + I_2 + \ldots + I_7\big)/8,$$
$$e_0 + e_1 + e_2 + \ldots + e_7 = 0,$$

and e_k is the current mismatch part of I_k. When the digital input data is m, unit-current-cells of $0, 1, 2, \ldots m-1$ are ON in any sample time, and the output voltage V_{out} is given by

$$V_{out} = mRI + \delta.$$

Here δ is DAC nonlinearity given by

$$\delta := R(e_0 + e_1 + e_2 + \ldots + e_{m-1}).$$

In this case the mismatch effects of $e_0, e_1, \ldots, e_7$ (or equivalently DAC nonlinearity δ) to the ADC output cause almost flat power spectrum in the entire band.

2.2 Lowpass Element Rotation

This subsection explains a lowpass element rotation algorithm [12]. Let us consider a circuit in Fig. 3, which consists of a digital lowpass filter ($1/(1 - z^{-1})$), a DAC with nonlinearity of $\delta(z)$ and an analog high pass filter ($1 - z^{-1}$). Then we have the followings:

$$C_2(z) = \frac{1}{1 - z^{-1}}\, C_1(z) \tag{4}$$

$$C_4(z) = (1 - z^{-1})\, C_3(z) \tag{5}$$

$$C_3(z) = C_2(z) + \delta(z). \tag{6}$$

Thus the analog output of $C_4(z)$ is given by

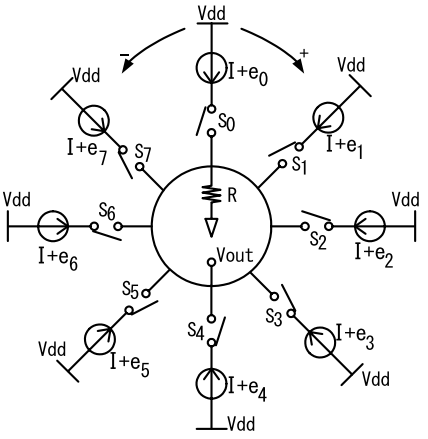

Fig. 4 A current-steering segmented DAC with 9-level resolution in a ring form.

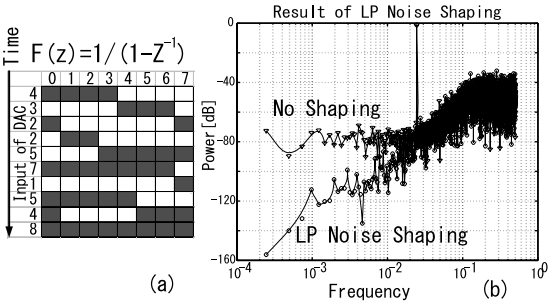

Fig. 5 DAC nonlinearity lowpass noise-shaping by an element rotation algorithm when a segmented current-steering internal DAC with 9-level resolution is used. (a) Current-cells in ON state which are filled in black, when input data are sequentially given by 4, 3, 2, 2, 5,.... (b) Simulation result for output spectrum. We see that the DAC nonlinearity power is noise-shaped ("LP Noise Shaping") with the element rotation algorithm while it is not noise-shaped ("No Shaping") without the algorithm.

$$C_4(z) = C_1(z) + (1 - z^{-1})\,\delta(z). \tag{7}$$

We see that the DAC nonlinearity $\delta(z)$ is first-order noise-shaped by $1 - z^{-1}$. Note that Eqs. (4), (5), (6) are equivalent to the following:

$$C_2(n+1) = C_2(n) + C_1(n+1) \tag{8}$$

$$C_4(n+1) = C_3(n+1) - C_3(n) \tag{9}$$

$$C_3(n) = C_2(n) + \delta(n). \tag{10}$$

If we replace a multi-bit DAC in a lowpass ΔΣAD modulator with the circuit in Fig. 3, its DAC nonlinearity is noise-shaped. However, in practice this structure cannot work properly; suppose that $C_1(n)$ is always a positive number, say 2, then the DAC input $C_2(n)$ becomes infinite (out-of-DAC-input-range) as n increases. Then the equivalent implementation (called an element rotation algorithm) has to be considered.

First we modify the segmented current-steering DAC as follows:

- Arrange unit-current-cells of the DAC in a ring form as shown in Fig. 4.
- Let the DAC have a pointer to show which unit-current-cell should be selected next sample time, and let the pointer be $P(n)$ at time n.

Suppose that we have infinite number of unit-current-cells, and $C_2(n) = a$, $C_1(n+1) = b$ (where $0 \le b \le 8$). Then the unit-current-cells of $0, 1, \ldots, a+b-1$ in the DAC are ON, and it follows from Eqs. (8) and (10) that

$$C_3(n+1) = (a+b)RI + R(e_0 + e_1 + e_2 + \ldots + e_{a+b-1}).$$

Since

$$C_3(n) = aRI + R(e_0 + e_1 + e_2 + \ldots + e_{a-1}),$$

the analog output $C_4(n+1)$ is given by

$$\begin{aligned} C_4(n+1) &= C_3(n+1) - C_3(n) \\ &= bRI + R(e_{a-1} + e_a + e_{a+1} + \ldots + e_{a+b-1}), \end{aligned}$$

which corresponds that the unit-current-cells of $a-1, a, a+1, \ldots, a+b-1$ in the DAC are ON. However, there are only 8 unit-current-cells in the actual DAC, and $a+b-1$ can be larger than 7. Then for the actual implementation of the above structure in the lowpass element rotation algorithm, the unit-current-cells are arranged in a ring form, and in this case the unit-current-cells of $\mathrm{mod}_8(a-1), \mathrm{mod}_8(a), \mathrm{mod}_8(a+1), \ldots, \mathrm{mod}_8(a+b-1)$ are ON. The rigorous description of the lowpass element rotation algorithm is as follows:

- Suppose that the input data $C_1(n) = c_n$ (where $n = 0, 1, 2, 3 \ldots$).
- Turn on c_n unit-current-cells of $\mathrm{mod}_8(P(n)+1)$, $\mathrm{mod}_8(P(n)+2)$, $\mathrm{mod}_8(P(n)+3)$, ..., $\mathrm{mod}_8(P(n)+c_n)$.
- Set the pointer at time $n+1$ to $P(n+1) = \mathrm{mod}_8(P(n)+c_n)$.

Figure 5(a) shows the unit-current-cells in ON state which are filled in black when input data are sequentially given by 4, 3, 2, 2, 5...When the input is 4 at time n, unit-current-cells of 0, 1, 2, 3 are ON. When it is 3 at time $n+1$, those of 4, 5, 6 are ON, and when it is 2 at time $n+2$, those of 7, ($\mathrm{mod}_8(8)$=)0 are ON. Also when it is 2 at time $n+3$, those of ($\mathrm{mod}_8(9)$=)1, ($\mathrm{mod}_8(10)$=)2 are ON. By selecting unit-current-cells in this way (i.e., always clockwise), mismatches among unit-current-cells are first-order lowpass noise-shaped [11]–[13]. Figure 5(b) shows the noise-shape effect by MATLAB simulation. The ADC output power spectrum contributed by DAC nonlinearities in the signal band is flat with a normal segmented current-steering DAC, however it is noise-shaped when this algorithm is incorporated.

2.3 Highpass Element Rotation

This subsection explains a highpass element rotation algorithm [9]. Let us consider a circuit in Fig. 6, which consists of a digital highpass filter ($1/(1+z^{-1})$), a DAC with nonlinearity of $\delta(z)$ and an analog lowpass filter ($1+z^{-1}$). Then we have the followings:

$$D_2(z) = \frac{1}{1+z^{-1}}\,D_1(z) \tag{11}$$

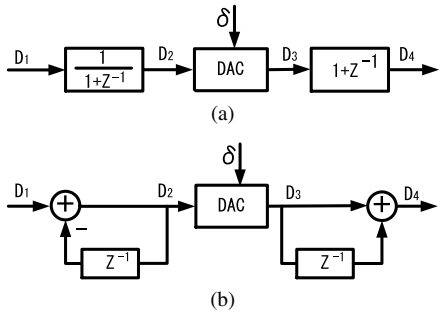

Fig. 6 (a) Highpass element rotation architecture. (b) Equivalent block diagram.

$$D_4(z) = (1 + z^{-1})\, D_3(z) \tag{12}$$

$$D_3(z) = D_2(z) + \delta(z). \tag{13}$$

Thus the analog output of $D_4(z)$ is given by

$$D_4(z) = D_1(z) + (1 + z^{-1})\delta(z). \tag{14}$$

We see that the DAC nonlinearity $\delta(z)$ is first-order noise-shaped by $1 + z^{-1}$. Note that Eqs. (11), (12), (13) are equivalent to the following:

$$D_2(n + 1) = D_2(n) - D_1(n + 1) \tag{15}$$

$$D_4(n + 1) = D_3(n + 1) + D_3(n) \tag{16}$$

$$D_3(n) = D_2(n) + \delta(n). \tag{17}$$

If we replace a multi-bit DAC in a highpass ΔΣAD modulator with the circuit in Fig. 6, its DAC nonlinearity is noise-shaped. However, similarly to the lowpass case, this structure cannot work properly and we have to consider its equivalent implementation (a highpass element rotation algorithm).

We modify the segmented current-steering DAC so that the unit-current-cells are in a ring form and the DAC have a pointer $P(n)$. The rigorous description of the highpass element rotation algorithm is as follows:

- At time $2n$:
  - Suppose that the input data $D_1(2n) = d_{2n}$.
  - Turn on d_{2n} unit-current-cells of $P(2n)$, $\mathrm{mod}_8(P(2n) + 1)$, $\mathrm{mod}_8(P(2n) + 2)$, …, $\mathrm{mod}_8(P(2n) + d_{2n} - 1)$. In other words, d_{2n} unit-current-cells are selected from $P(2n)$ *clockwise.*
  - Set the pointer at time $2n + 1$ to $P(2n + 1) = \mathrm{mod}_8(P(2n) + d_{2n} - 1)$.
- At time $2n + 1$:
  - Suppose that the input data $D_1(2n + 1) = d_{2n+1}$.
  - Turn on d_{2n+1} unit-current-cells of $P(2n + 1)$, $\mathrm{mod}_8(P(2n + 1) - 1)$, $\mathrm{mod}_8(P(2n + 1) - 2)$, …, $\mathrm{mod}_8(P(2n + 1) - d_{2n} + 1)$. In other words, d_{2n+1} unit-current-cells are selected from $P(2n+1)$ *counter clockwise.*
  - Set the pointer at time $2n + 2$ to $P(2n + 2) = \mathrm{mod}_8(P(2n + 1) - d_{2n+1} + 1)$.

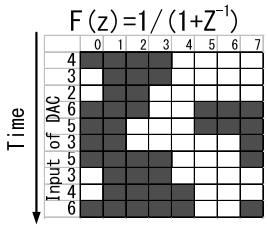

Fig. 7 Highpass noise-shaping of DAC nonlinearities by an element rotation algorithm when a segmented current-steering internal DAC with 9-level resolution is used. Current-cells in ON state which are filled in black, when input data are sequentially given by 4, 3, 2, 6, 5, ….

Figure 7(a) shows the unit-current-cells in ON state while input data are shifted by 4, 3, 2, 6, … for highpass noise-shaping in element rotation algorithm by $1 + z^{-1}$. When the input is 4 at time n, unit-current-cells of 0, 1, 2, 3 are ON. When it is 3 at time $n + 1$, those of 3, 2, 1 are ON, and when it is 2 at time $n + 2$, those of 1, 2 are ON. Also when it is 6 at time $n + 3$, those of 2, 1, 0, 7, 6, 5 are ON. In other words, unit-current-cells are selected clockwise or counter clockwise alternately at every sample time.

3. Complex Bandpass Noise-Shaping Algorithm of DAC Nonlinearities

In this section, we will derive an element rotation algorithm in complex bandpass modulators, based on the element rotation algorithms in lowpass and highpass modulators described in Sect. 2.

3.1 Complex Bandpass ΔΣAD Modulator

Figure 8 shows a complex bandpass ΔΣAD modulator, a first-order complex bandpass filter and its gain characteristics. We see that the complex filter has two inputs and outputs, and it consists of a complex bandpass filter, two internal ADCs and DACs. For example, the transfer function of the complex bandpass filter shown in Fig. 8(b) can be written as follows [6]:

$$H(z) = \frac{1}{z - (d + jc)}$$

where c and d are design parameters (appropriate constants of *real* values) which characterize the complex bandpass filter. We see in Fig. 8(c) that the gain of the complex bandpass filter is asymmetrical to the axis of $\omega = 0$.

3.2 Proposed Architecture for Complex Bandpass Noise-Shaping of DAC Nonlinearities

We consider here complex bandpass ΔΣAD modulators whose center of passband is at the normalized frequency of $\omega = \pi/2$ (1/4 of the sampling frequency) [1]–[6]. Figure 9 shows our proposed architecture for complex bandpass noise-shaping of DAC nonlinearities. It consists of a digital complex filter at front-end, two DACs, and an analog complex filter at back-end. I_1 is the digital output of the ADC in

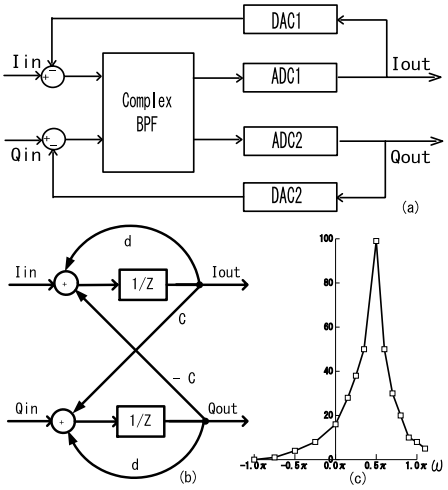

Fig. 8 (a) Complex bandpass ΔΣAD modulator block diagram. (b) An example of a complex bandpass filter. (c) Gain characteristics of Fig. 8(b).

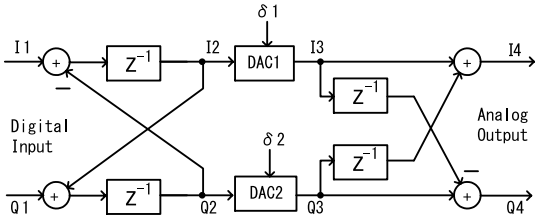

Fig. 9 Proposed architecture of DAC nonlinearity noise-shaping for a complex bandpass modulator, where two pointers and multiplexers are added to the feedback DACs. I_1 is the I-channel ADC output and Q_1 is the Q-channel ADC output, while I_4 is the I-channel DAC output and Q_4 is the Q-channel DAC output. δ_1 and δ_2 denote the nonlinearities of DAC1 and DAC2 respectively. However, note that this architecture cannot be implemented directly.

I-channel and Q_1 is that in Q-channel. Also I_4 is the analog output of the DAC in I-channel and Q_4 is that in Q-channel. The transfer function of the digiltal complex filter at front-end is written by

$$F(z) = \frac{1}{z - j}.$$

Then the transfer function of the analog complex filter at back-end is given by $1/F(z)$. Noting that the complex multi-bit output signal of 2-channel ADCs is given by

$$Y(z) := I_1(z) + jQ_1(z),$$

and the complex output signal of 2-channel DACs which is fedback to the complex filter is given by

$$M(z) := I_4(z) + jQ_4(z),$$

we obtain the followings in Fig. 9:

$$I_2(z) + jQ_2(z) = F(z) \cdot Y(z) \tag{18}$$

$$I_3(z) + jQ_3(z) = (I_2(z) + jQ_2(z)) + (\delta_1 + j\delta_2) \tag{19}$$

$$M(z) = \frac{1}{F(z)}(I_3 + jQ_3). \tag{20}$$

By substituting Eqs. (18) and (19) to Eq. (20), we have

$$M(z) = Y(z) + \frac{1}{F(z)}(\delta_1 + j\delta_2). \tag{21}$$

Note that Eqs. (1) and (2) hold also for the complex bandpass ΔΣAD modulator if we consider $H(z)$ is a complex filter and $X(z)$, $Y(z)$, $E(z)$ and $\delta(z)$ are complex signals. Then by substituting Eq. (21) to Eq. (1) and sorting it, we obtain

$$N(z) = \frac{H(z)}{1 + H(z)} \cdot \left[\frac{1}{H(z)}E(z) - \frac{1}{F(z)}(\delta_1(z) + j\delta_2(z))\right]. \tag{22}$$

We see that by comparing Eq. (22) with Eq. (3), not only the (complex) quantization noise $E(z)$ of 2-channel ADCs is noise-shaped by $1/H(z)$, but also the 2-channel DACs (complex) nonlinearities error $(\delta_1 + j\delta_2)$ is noise-shaped by $1/F(z)$.

3.3 Realization Algorithm for Proposed Architecture

We obtain the following equations in Fig. 9:

$$I_2(n+1) = I_1(n) - Q_2(n) \tag{23}$$

$$I_4(n+1) = I_3(n+1) + Q_3(n) \tag{24}$$

$$I_3(n) = I_2(n) + \delta_1(n) \tag{25}$$

$$Q_2(n+1) = I_2(n) + Q_1(n) \tag{26}$$

$$Q_4(n+1) = Q_3(n+1) - I_3(n) \tag{27}$$

$$Q_3(n) = Q_2(n) + \delta_2(n). \tag{28}$$

The direct realization of the proposed architecture in Fig. 9 is *not* possible because I_2, Q_2 can be out-of-input-range of the following I, Q-channel DACs. For example, suppose that

$$I_1(n) + jQ_1(n) = \exp(j\frac{\pi}{2}n) + 4.$$

This can happen because the center of the signal band in the modulator is at the normalized frequency of $\omega = \pi/2$, and I_1, Q_1 are integer values between 0 to 8. Then it follows from Eqs. (23) and (26) that

$$I_2(1) = 5 - Q_2(0), \quad I_2(2) = -I_2(0),$$
$$I_2(3) = -7 + Q_2(0), \quad I_2(4) = I_2(0)\ldots$$
$$Q_2(1) = 4 + I_2(0), \quad Q_2(2) = 10 - Q_2(0),$$
$$Q_2(3) = 4 - I_2(0), \quad Q_2(4) = -4 + Q_2(0)\ldots$$

We see that I_2 and Q_2 can be out of the DAC input rage (0, 1, 2, …,8).

Now we describe an equivalent realization of the proposed architecture; our implementation use only a digital filter at front-end of 2-channel DACs and does not require an analog filter at back-end.

[Proposed Algorithm]

We modify the two segmented current-steering DACs as follows (Fig. 10(a)):

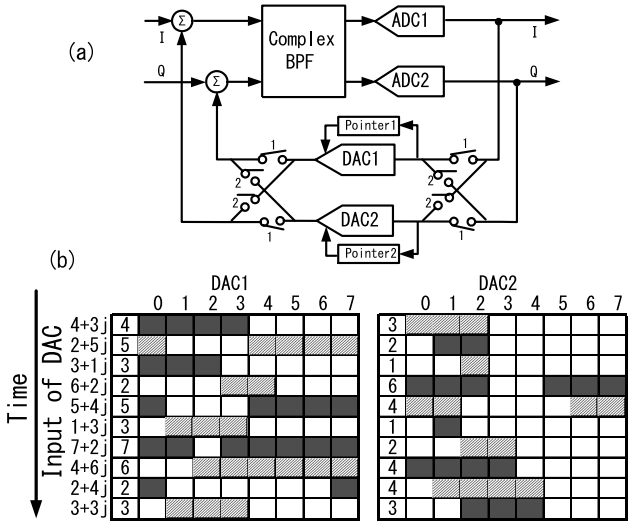

Fig. 10 (a) Proposed complex bandpass ΔΣAD modulator. (b) Explanation of the proposed algorithm. The unit-current-cells in ON state are filled in black for a real part (I-path) and in gray for an imaginary part (Q-path), when the complex input data are sequentially given by 4+3j, 2+5j, 3+j, 6+2j, ...

- Arrange unit-current-cells of each DAC in a ring form as shown in Fig. 4.
- Let each DAC have a pointer to show which unit-current-cell should be selected next sample time, and let the pointers for DAC1 and DAC2 be $P_1(n)$ and $P_2(n)$ at time n.

Then let their operation be as follows:

- At time $2n$:
  Suppose that the I-channel DAC input $I_1(2n) = i_{2n}$.
  - Turn on the following unit-current-cells of DAC1: $P_1(2n)$, $\mathrm{mod}_8(P_1(2n)+1), \ldots, \mathrm{mod}_8(P_1(2n)+i_{2n}-1)$. In other words, i_{2n} unit-current-cells are selected *clockwise* from $P_1(2n)$.
  - Make the output of DAC1 to be the I-channel DAC output, $I_4(2n)$.
  - Set the pointer of DAC1 at time $2n+1$ to $P_1(2n+1) = \mathrm{mod}_8(P_1(2n) + i_{2n} - 1)$.

  Assume that the Q-channel DAC input $Q_1(2n) = q_{2n}$.
  - Turn on the following unit-current-cells of DAC2: $\mathrm{mod}_8(P_2(2n) + 1)$, $\mathrm{mod}_8(P_2(2n) + 2)$, ..., $\mathrm{mod}_8(P_2(2n) + q_{2n})$. In other words, q_{2n} unit-current-cells are selected *clockwise* from $P_2(2n)+1$.
  - Make the output of DAC2 to be the Q-channel DAC output, $Q_4(2n)$.
  - Set the pointer of DAC2 at time $2n+1$ to $P_2(2n+1) = \mathrm{mod}_8(P_2(2n) + q_{2n})$.
- At time $2n+1$:
  Suppose that the I-channel DAC input $I_1(2n+1) = i_{2n+1}$.
  - Turn on the following unit-current-cells of DAC2: $P_2(2n+1)$, $\mathrm{mod}_8(P_2(2n+1)-1), \ldots, \mathrm{mod}_8(P_2(2n+1) - i_{2n+1} + 1)$. In other words, i_{2n+1} unit-current-cells are selected *counter clockwise* from $P_2(2n+1)$.
  - Make the output of DAC2 to be the I-channel DAC output, $I_4(2n+1)$.
  - Set the pointer of DAC2 at time $2n+2$ to $P_2(2n+2) = \mathrm{mod}_8(P_2(2n+1) - i_{2n+1} + 1)$.

  Assume that the Q-channel DAC input $Q_1(2n+1) = q_{2n+1}$.
  - Turn on the following unit-current-cells of DAC1: $\mathrm{mod}_8(P_1(2n+1)+1)$, $\mathrm{mod}_8(P_1(2n+1)+2)$, ..., $\mathrm{mod}_8(P_1(2n+1)+q_{2n+1})$ In other words, q_{2n+1} unit-current-cells are selected *clockwise* from $\mathrm{mod}_8(P_1(2n+1)+1)$.
  - Make the output of DAC1 to be the Q-channel DAC output, $Q_4(2n+1)$.
  - Set the pointer of DAC1 at time $n+2$ to $P_1(2n+2) = \mathrm{mod}_8(P_1(2n+1) + q_{2n+1})$.

Figure 10(b) explains their operation when the complex input data are sequentially given by 4+3j, 2+5j, 3+j, 6+2j, ...

Now we will explain how this algorithm was derived and why it is equivalent to the architecture in Fig. 9.

First, we consider the I-channel. The I-channel DAC (whose output is I_4 as shown in the upper part of Fig. 9) is equivalent to ⌈Highpass digital filter + DAC + Lowpass analog filter⌋; look at the left part of Fig. 6(b) and the upper-left part of Fig. 9, and also compare Eqs. (23) and (15). If $Q_2(n)$ in Eq. (23) is replaced with $I_2(n)$, Eq. (23) has the same form as Eq. (15). Similarly look at the right part of Fig. 6(b) and the upper-right part of Fig. 9, and also compare Eqs. (24) and (16). $Q_3(n)$ in Eq. (24) is replaced with $I_3(n)$, Eq. (24) has the same form as Eq. (16). Also Eq. (25) has the same form as Eq. (17). Thus we see the following:

- For the I-channel DAC output I_4, we apply a *highpass* element rotation algorithm with internal interaction between I, Q paths.

Next, we consider the Q-channel. The Q-channel DAC (whose output is Q_4 as shown in the lower part of Fig. 9) is equivalent to ⌈Lowpass digital filter + DAC + Highpass analog filter⌋; look at the left part of Fig. 3(b) and the lower-left part of Fig. 9, and also compare Eqs. (26) and (8). If $I_2(n)$ in Eq. (26) is replaced with $Q_2(n)$, Eq. (26) has the same form as Eq. (8). Similarly look at the right part of Fig. 3(b) and the lower-right part of Fig. 9, and also compare Eqs. (27) and (9). $I_3(n)$ in Eq. (27) is replaced with $Q_3(n)$, Eq. (27) has the same form as Eq. (9). Also Eq. (28) has the same form as Eq. (10). Thus we see the following:

- For the Q-channel DAC output Q_4, we apply a *lowpass* element rotation algorithm with internal interaction between I, Q paths.

Now we consider the interactions between I-path and Q-path

in Fig. 9 (or equivalently in Eqs. (23), (24), (26) and (27)). It follows from Eqs. (23) and (24) that the I-channel output I_4 at time $n+1$ is a function of the Q-channel internal states ($Q_2(n)$, $Q_3(n)$) at time n as well as the I-channel input I_1. Also we see from Eqs. (26) and (27) that the Q-channel output Q_4 at time $n+1$ is a function of the I-channel internal states ($I_2(n)$, $I_3(n)$) at time n as well as the Q-channel input Q_1. Noting that the pointers $P_1(n), P_2(n)$ keep some information of the I, Q channels internal states, we have the following observation:

- If DAC1 with a pointer P_1 is used for I-channel and DAC2 with a pointer P_2 is used for Q-channel at time $2n$, then DAC1 is used for Q-channel and DAC2 is used for I-channel at time $2n+1$.

Then the proposed algorithm is derived and the nonlinearities of 2-channel DACs, δ_1, δ_2, will be first-order complex bandpass noise-shaped.

4. Simulation of Proposed Algorithm

We have conducted MATLAB simulations to confirm the noise-shaping function on multi-bit DAC nonlinearities of the proposed algorithm. We used a fourth-order complex modulator [15] with internal ADCs/DACs of 9-level resolution in three cases. Figure 11 shows the complex bandpass filter used inside the modulator, where three poles are located at the normalized angular frequency of $\omega = \pi/2$ while one is at $\omega = 3\pi/2$; the reason that one pole is located at $\omega = 3\pi/2$ is that when this complex filter is incorporated in a modulator in Fig. 8, the quantization noise of the modulator is reduced by noise-shaping at $\omega = 3\pi/2$, which will appear at $\omega = \pi/2$ of the modulator output as image quantization noise caused by I, Q mismatches inside the modulator. For all three cases, the same analog complex bandpass filter and two ideal internal ADCs in a $\Delta\Sigma$ modulator were used. However two DACs in a modulator in three cases are different as follows:

- Case 1: Two identical and ideal (linear) DACs were used.
- Case 2: Two normal segmented current-steering DACs with mismatches among unit-current-cells were used.

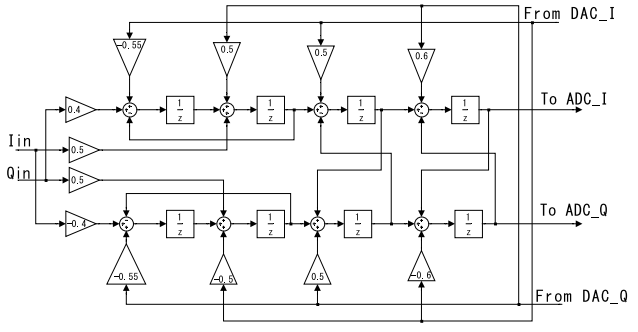

Fig. 11 A fourth-order complex bandpass filter used in a modulator in Fig. 8.

- Case 3: Two DACs whose mismatches are the same as case 2 and which employ the proposed element rotation algorithm were used.

Figures 12, 13 show the simulation result comparison for output spectrum and SNR of modulators in three cases, where the simulation conditions are as follows:

- In cases 2 and 3, $e_0, e_1, e_2, \ldots, e_7$ in DAC1 are 0.0023, −0.0015, −0.003, 0.0028, 0.0025, 0.0029, −0.001 and 0.0 (LSB) while those in DAC2 are −0.0017, 0.0015, −0.0025, 0.002, 0.0026, 0.0, −0.0019, and 0.0 (LSB).
- 16 K-point FFT is used to obtain the SNR.
- Input frequency (f_{in})/sampling frequency (f_s) = 4,095/16,384.

We see that in case 1, SNR of the ADC increases as OSR increases. However in case 2, SNR saturates as OSR increases; for small OSRs, quantization noise is dominant but it is noise-shaped and hence SNR improves as OSR in-

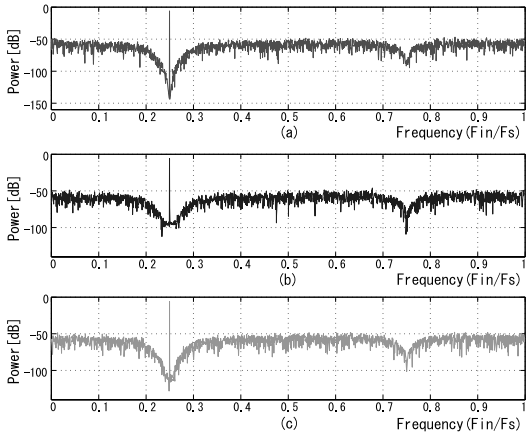

Fig. 12 The simulated results of the output power spectrum for complex bandpass $\Delta\Sigma$ modulators. (a) The simulated result with ideal DACs. (b) The simulated result with normal segmented current-steering DACs with mismatch among unit-current-cells. (c) The simulated result with proposed algorithm of DACs with the same mismatch among unit-current-cells. The reason that the output power is noise-shaped at $\omega = 3\pi/2$ (as well as at $\omega = \pi/2$ which is the center of the signal band) is that the complex filter in Fig. 11 has a pole at $\omega = 3\pi/2$ (as well as three poles at $\omega = \pi/2$).

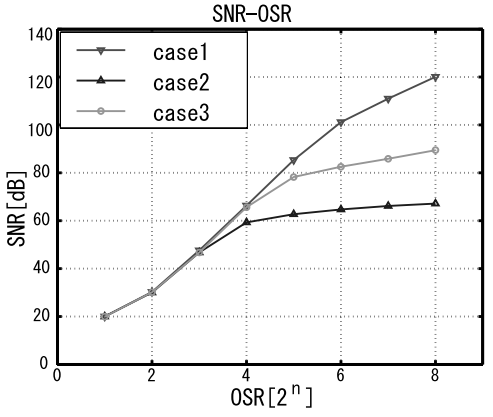

Fig. 13 The simulated results of SNR versus OSR in cases 1, 2 and 3.

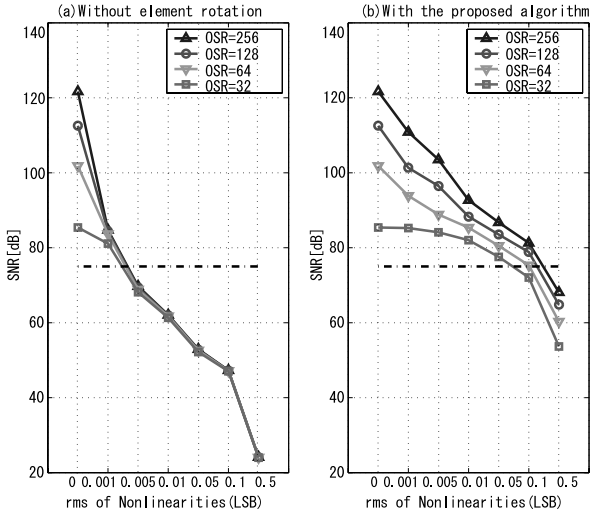

Fig. 14 Simulation results of the modulator SNR versus rms values of mismatches $e_0, e_1, e_2, \ldots, e_7$ for OSR = 32, 64, 128 and 256. The left graph shows in case that normal segmented DACs are used while the right graph shows in that case that our proposed algorithm is incorporated.

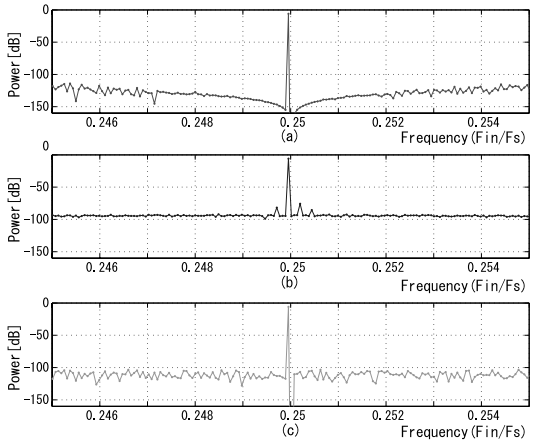

Fig. 15 The simulated results of the output power spectrum focused around the signal band in Fig. 12, where (4,095/16,384) f_s is the signal frequency component. (a) Case 1. (b) Case 2. (3) Case 3. We see that in case 2, there are spurious tones at (4,091/16,384) f_s and (4,099/16,384) f_s while they are removed in case 3.

creases. However for high OSRs the noise due to DAC nonlinearity becomes dominant, which is not noise-shaped and hence increasing OSR does not help much improve SNR. On the other hand, in case 3, the noise caused by nonlinearities of DAC is pushed out from the signal band, and their influence to the ADC accuracy is reduced which leads to the ADC SNR improvement.

Figure 14 shows simulation results of the modulator SNR versus root-mean-square (rms) values of mismatches $e_0, e_1, e_2, \ldots, e_7$ for OSR = 32, 64, 128 and 256. Here the value of the mismatches is defined by

$$\text{rms} := \sqrt{(e_0^2 + e_1^2 + e_2^2 + \ldots + e_7^2)/8}$$

and the ratios of $e_0, e_1, e_2, \ldots, e_7$ in DAC1 are 0.0023, −0.0015, −0.003, 0.0028, 0.0025, 0.0029, −0.001 and 0.0 (LSB) while those in DAC2 are −0.0017, 0.0015, −0.0025, 0.002, 0.0026, 0.0, −0.0019, and 0.0 (LSB). The left graph shows in case 2 while the right graph shows in case 3. We see that in case 2 SNR degrades rapidly as rms value increases while in case 3 SNR is improved.

We observe in Figs. 13, 14 that in case2 SNR does not improve even if OSR increases for relatively large DAC nonlinearities (if the spectrum of the DAC nonlinearities error is white, twice of OSR leads to at least 3 dB SNR improvement, even if it is not noise-shaped); this is because there are spurious tones at the frequencies of (4,091/16,384) f_s and (4,099/16,384) f_s due to large DAC nonlinearityies (Fig. 15), which are the main noise (distortion) components and are not removed with this range of OSRs.

5. Concluding Remarks

We have proposed a new noise-shaping algorithm of multi-bit DAC nonlinearities for a high resolution complex bandpass ΔΣAD modulator. The performance of the complex bandpass ΔΣADC can be improved by adding some simple digital circuits. The effectiveness of proposed algorithm is confirmed by MATLAB simulation. Finally we remark the followings:

- In the proposed algorithm, at time $2n$, DAC1 is used for I-channel and DAC2 is for Q-channel, while, at time $2n + 1$, DAC1 is for Q-channel and DAC2 is for I-channel; DAC1, DAC2 are used alternately for I, Q-channels, and hence the harmful influence by mismatches between 2-channel DACs is expected to be suppressed with this algorithm.
- The proposed algorithm is applicable to multi-bit complex bandpass ΔΣ DA modulators as well as AD modulators. The importance of the bandpass ΔΣ DA modulator is described in [16].
- Our approach here is to improve the accuracy of analog circuits using digital signal processing techniques. We believe that such an approach becomes more important, because as the VLSI technology progresses and the device size scales down, the supply voltage goes down, which makes it difficult to achieve the high accuracy of analog circuits with only circuit technique. On the other hand, the digital circuit becomes faster, cheaper and lower power, which makes rather complicated digital signal processing algorithm feasible to utilize for the analog circuit performance improvement.

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References

[1] K. Philips, "A 4.4mW 76 dB complex ΣΔ ADC for Bluetooth receivers," ISSCC Digest of Technical Papers, vol.46, pp.64–65, Feb. 2003.
[2] F. Henkel, U. Langmann, A. Hanke, S. Heinen, and E. Wanger, "A 1 MHz-bandwidth second-order continuous-time quadrature bandpass sigma-delta modulator for low-IF radio receivers," IEEE J. Solid-State Circuits, vol.37, pp.1628–1635, Dec. 2002.
[3] F. Esfahari, P. Basedau, P. Ryter, and R. Beker, "A fourth order continuous-time complex sigma-delta ADC for low-IF GSM and EDGE receivers," Symp. VLSI Circuits, Digest of Technical Papers, pp.75–78, June 2003.
[4] R. Schreier, J. Lloyd, L. Singer, D. Paterson, M. Timko, M. Hensley, G. Patterson, K. Behel, and J. Zhou, "A 10–300 MHz IF-digitizing IC with 90–105 dB dynamic range and 15–333 kHz bandwidth," IEEE J. Solid-State Circuits, vol.37, pp.1636–1644, Dec. 2002.
[5] T. Salo, T. Hollman, S. Lindfors, and K. Halonen, "A Dual-Mode 80MHz bandpass ΔΣ modulator for a GSM/WCDMA IF-receiver," ISSCC Digest of Technical Papers, vol.45, pp.218–219, Feb. 2002.
[6] S.A. Jantzi, K.W. Martin, and A.S. Sedra, "Quadrature bandpass ΣΔ modulator for digital radio," IEEE J. Solid-State Circuits, vol.32, pp.1935–1949, Dec. 1997.
[7] S.R. Norsworthy, R. Schreier, and G.C. Temes, eds., Deta-Sigma Data Converters, —Theory, Design and Simulation, IEEE Press, 1997.
[8] T. Ueno, A. Yasuda, T. Yamaji, and T. Itakura, "A fourth-order bandpass Δ-Σ modulator using second-order bandpass noise-shaping dynamic element matching," IEEE J. Solid-State Circuits, vol.37, pp.809–816, July 2002.
[9] T. Shui, R. Screier, and F. Hudson, "Mismatch shaping for a current-mode multibit delta-sigma DAC," IEEE J. Solid-State Circuits, vol.34, pp.331–338, March 1999.
[10] L.R. Carley, "A noise-shaping coder topology for 15 bit converters," IEEE J. Solid-State Circuits, vol.24, pp.267–273, April 1989.
[11] E. Fogleman, I. Galton, W. Huff, and H. Jensen, "A 3.3-V single-poly CMOS audio ADC delta-sigma modulator with 53.8-dB peak SINAD and 105-dB peak SFDR," IEEE J. Solid-State Circuits, vol.35, pp.297–307, March 2000.
[12] R. Shreier, J. Steensgaard, and G.C. Temes, "Speed vs. dynamic range trade-off in oversampling data converters," in Trade-Offs in Analog Circuit Design, The Designer's Companion, eds. C. Toumazou, G. Moschytz, and B. Gilbert, pp.644–653, Kluwer Academic Publishers, 2002.
[13] Y. Yang, A, Chokhawala, M. Alexander, J. Melanson, and D. Hester, "A 114 dB 68 mW chopper-stabilized stereo multi-bit audio A/D converter," ISSCC Digest of Technical Papers, vol.46, pp.56–57, Feb. 2003.
[14] B. Razavi, Principles of Data Converter Design, IEEE Press, 1995.
[15] A. Swaminathan, A single-IF receiver architecture using a complex SD modulator, M.Eng. Thesis, Carleton Univ. Ottawa, ON, Canada 1997.
[16] D.B. Barkin, A.C.Y. Yin, D.K. Su, and B.A. Wooley, "A CMOS oversampling bandpass cascaded D/A converter with digital FIR and current-mode semi-digital filtering," Symp. VLSI Circuits, Digest of Technical Papers, pp.79–82, June 2003.

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