LETTER *Special Section on Analog Circuit and Device Technologies*

Input-Dependent Sampling-Time Error Effects Due to Finite Clock Slope in MOS Samplers

Naoto HAYASAKA[†], ***Student Member and*** **Haruo KOBAYASHI**[†a)], ***Member***

SUMMARY This paper analyzes the input-dependent sample-time error in MOS sampling circuits caused by the finite slope of the sampling clock, and clarifies the following: (i) Input-dependent sampling jitter causes phase modulation in the sampled data. (ii) The formulas for SDR due to such sampling errors are explicitly derived. (iii) NMOS sampling circuits generate even-order harmonics, which are greatly reduced by using a differential topology. (iv) CMOS sampling circuits *without* clock skew between V_{clk} and $\overline{V_{clk}}$ generate odd-order harmonics which a differential topology cannot help cancel, whereas circuits *with* clock skew generate even-order as well as odd-order harmonics. (v) For single-ended sampling circuits, the SDR of CMOS circuits *without* clock skew is better than that of NMOS circuits. (vi) NMOS differential sampling circuits are relatively insensitive to input-dependent sampling-time error effects, which would be the best regarding to the input-dependent sampling-time error effects. (vii) Its effects in case of NMOS differential samplers with finite skew between plus and minus path clocks are discussed. (viii) Its effects in CMOS samplers with finite skew between PMOS and NMOS clocks are discussed.

key words: *sampling, jitter, MOS switch, track/hold circuit, ADC*

1. Introduction

Let us consider the NMOS sampling circuit in Fig. 1(a), whose topology is popular in high-speed, medium resolution (6–8 bit) CMOS ADCs [1], [2]. Suppose that the sampling clock V_{clk} has a finite slope (Fig. 2) and the ideal sampling time is defined to be the negative-going $(M + V_{thn})$-crossing of V_{clk}. (Here V_{thn} is the threshold voltage of the NMOS transistor.) Then the actual sampling time is that when V_{clk} passes through the value when it exceeds a threshold voltage of the NMOS transistor. In other words, the NMOS switch in Fig. 1(a) turns off when V_{clk} is above V_{in} by V_{thn}. Thus when V_{in} is above M, the actual sampling time is earlier than the ideal sampling time, whereas when V_{in} is less than M, it is later. Then we see that the finite slope of the sampling clock effectively causes input-dependent sampling time error (effective jitter) [2]–[4] even though the sampling clock does not have physical jitter [5], [6]. There are many nonidealities in MOS sampling circuits (such as clock jitter, charge injection, finite bandwidth), and in this letter we will focus on the effects of the sampling clock finite slope; we will analyze this effect rigorously for NMOS and CMOS sampling circuits (as shown in Fig. 1 and which are used for 6–8 bit high-speed CMOS ADCs) in order to estimate a required slope of the sampling clock for a specified Signal-to-

Manuscript received October 26, 2003.
Manuscript revised January 7, 2004.

[†]The authors are with the Department of Electronic Engineering, Faculty of Engineering, Gunma University, Kiryu-shi, 376-8515 Japan.
a) E-mail: k_haruo@el.gunma-u.ac.jp

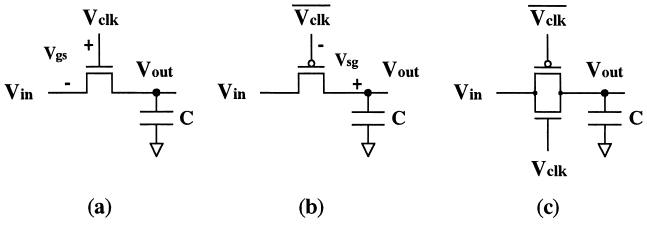

Fig. 1 NMOS, PMOS and CMOS sampling circuits.

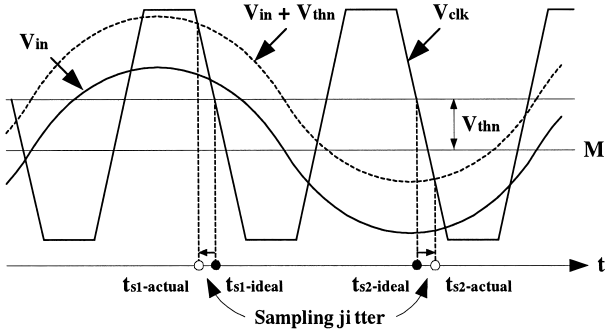

Fig. 2 Waveforms for V_{in} and V_{clk} to illustrate how a finite slope of V_{clk} introduces V_{in}-dependent sampling-time error (effective jitter).

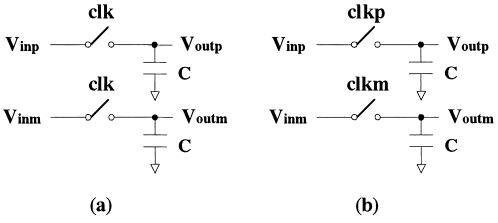

Fig. 3 Differential sampling circuits. (a) Without clock skew. (b) With clock skew of t_{skw} between *clkp* and *clkm*.

Distortion Ratio (SDR), as well as allowable clock skews in CMOS single-ended samplers, and NMOS, CMOS differential samplers. Since we focus on the effects of the sampling clock finite slope, we simplify the problem formulation as follows:

(i) We assume that the input for a single-ended sampling circuit (Fig. 1) is given by

$$V_{in}(t) = A\sin(\omega t) + M \tag{1}$$

and the inputs for a differential sampling circuit (Fig. 3) are

$$V_{inp}(t) = \frac{A}{2}\sin(\omega t) + M,$$

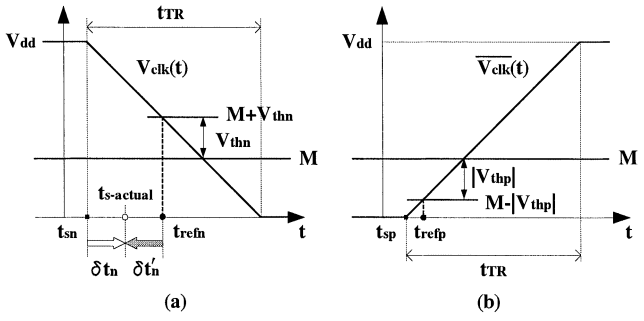

Fig. 4 Sampling clocks V_{clk}, $\overline{V_{clk}}$ and reference sampling timing t_{refn}, t_{refp}. (a) NMOS sampling circuit. (b) PMOS sampling circuit.

$$V_{inm}(t) = -\frac{A}{2}\sin(\omega t) + M.$$

(ii) We suppose that the sampling clock V_{clk} for NMOS switches starts to fall at time t_{sn} (Fig. 4(a)), and in the falling transient V_{clk} is expressed by

$$V_{clk}(t) = -(V_{dd}/t_{TR}) \cdot (t - t_{sn}) + V_{dd}. \tag{2}$$

Also the sampling clock $\overline{V_{clk}}$ for PMOS switches starts to rise at time t_{sp} (Fig. 4(b)), and in the rising transient it is expressed by

$$\overline{V_{clk}}(t) = (V_{dd}/t_{TR}) \cdot (t - t_{sp}). \tag{3}$$

(iii) The sampling clocks do not have (physical) jitter.
(iv) In the CMOS sampling circuit in Fig. 1(c), the sampling clocks for NMOS and PMOS switches can have a finite skew.
(v) The sampling clocks for the differential circuit in Fig. 3 can have a finite skew.
(vi) The effects of the MOS switch finite on-resistance, body effect (though we mention some comments on the MOS switch body effect in Sect. 2.1), finite drain-source voltage and charge injection are not taken into account. Also the device mismatch effects in differential sampling circuits in Fig. 3 are not considered. We assume that $V_{thn} = -V_{thp}$, where V_{thn}, V_{thp} are NMOS, PMOS threshold voltages respectively.

2. NMOS Sampling Circuit

2.1 NMOS Single-Ended Sampling Circuit

Let us consider the case when V_{clk} is in the falling transient state in an NMOS sampling circuit (Fig. 1(a)), and the NMOS switch turns off at time $t_{s\text{-}actual} := t_{sn} + \delta t_n$. Here, δt_n denotes the deviation of actual sampling time from t_{sn} (Fig. 4(a)). Then we have from OFF condition for NMOS switch

$$V_{clk}(t_{sn} + \delta t_n) = V_{in}(t_{sn} + \delta t_n) + V_{thn}. \tag{4}$$

It follows from Eqs. (2), (4) that

$$-\frac{V_{dd}}{t_{TR}}\delta t_n + V_{dd} = V_{in}(t_{sn} + \delta t_n) + V_{thn}. \tag{5}$$

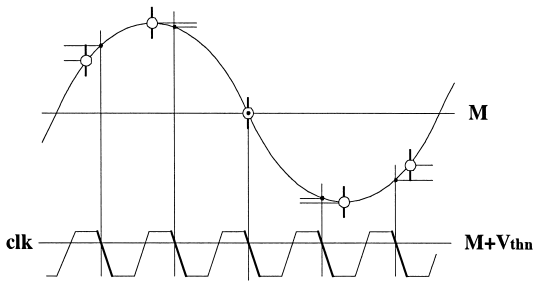

Fig. 5 Ideal (·) and actual (∘) sampling points in a single-ended NMOS sampling circuit.

Then Eq. (5) gives us the following:

$$\begin{aligned} t_{s\text{-}actual} &= t_{sn} + \delta t_n \\ &= t_{sn} + \frac{t_{TR}}{V_{dd}}(V_{dd} - V_{in}(t_{sn} + \delta t_n) - V_{thn}) \\ &= t_{sn} + \frac{t_{TR}}{V_{dd}}(V_{dd} - A\sin(\omega t_{s\text{-}actual}) - M - V_{thn}) \\ &= t_{\text{refn}} + \delta t'_n. \end{aligned} \tag{6}$$

Here, t_{refn} is the reference (ideal) sampling time (Fig. 4(a)) and $\delta t'_n$ denotes the deviation of the actual sampling time from t_{refn}, which are given by

$$t_{\text{refn}} := t_{sn} + \frac{t_{TR}}{V_{dd}}(V_{dd} - M - V_{thn}), \tag{7}$$

$$\delta t'_n := -\frac{t_{TR}A}{V_{dd}}\sin(\omega t_{s\text{-}actual}). \tag{8}$$

Let us denote t_{refn} as t, and we have the following sampled output from Eqs. (7), (8):

$$V_{out}(t) \approx A\sin(\omega t + \phi(t)) + M, \tag{9}$$

where

$$\phi(t) := -\frac{A\omega t_{TR}}{V_{dd}}\sin(\omega t). \tag{10}$$

We see from Eqs. (9), (10) that the input dependent sampling-time error causes *phase modulation*. Figure 5 illustrates ideal and actual sampling points.

$$\text{When} \quad \frac{A\omega t_{TR}}{V_{dd}} \ll 1, \quad \text{then } |\phi(t)| \ll 1,$$

and Eqs. (9), (10) give us the following sampled output:

$$\begin{aligned} &V_{out}(t) \\ &\quad\approx A\Big[\sin(\omega t)\cos(\phi(t) + \cos(\omega t)\sin(\phi(t))\Big] + M \\ &\quad\approx A\Big[\sin(\omega t)(1 - \frac{1}{2}\phi(t)^2) + \cos(\omega t)\cdot\phi(t)\Big] + M \\ &\quad= A\left(1 - \frac{3A^2\omega^2 t_{TR}^2}{8V_{dd}^2}\right)\sin(\omega t) - \frac{A^2\omega t_{TR}}{2V_{dd}}\sin(2\omega t) \\ &\qquad+\frac{A^3\omega^2 t_{TR}^2}{8V_{dd}^2}\sin(3\omega t) + M \\ &\quad\approx A\sin(\omega t) - \frac{A^2\omega t_{TR}}{2V_{dd}}\sin(2\omega t) + M. \end{aligned} \tag{11}$$

We see from Eq. (11) that when $A\omega t_{TR}/V_{dd} \ll 1$, the second harmonics is dominant rather than the third harmonics. In this case, Eq. (11) gives us the following:

$$\begin{aligned} SDR &= 20\log_{10}\frac{A}{A^2\omega t_{TR}/(2V_{dd})} \\ &= 20\log_{10}\frac{2V_{dd}}{A\omega t_{TR}}\ [\mathrm{dB}]. \end{aligned} \tag{12}$$

Remark: (i) Eq. (12) yields to

$$\begin{aligned} SDR &= 20\log_{10}\frac{2V_{dd}}{A(2\pi f)t_{TR}} \\ &= 20\log_{10}\frac{V_{dd}}{2Aft_{TR}} + 20\log_{10}\frac{2}{\pi} \\ &= 20\log_{10}\frac{V_{dd}}{A_{pp}ft_{TR}} - 4\ [\mathrm{dB}]. \end{aligned} \tag{13}$$

Equation (13) corresponds to the result in [4] which was derived empirically by simulation; but note that [4] does not discuss differential samplers or CMOS samplers including clock skew effects which we will discuss in the following sections.

(ii) Let us consider the body effect of the NMOS switch. Suppose that the body of the NMOS switch is connected to ground in Fig. 1(a), and then its threshold voltage V_{thn} increases as V_{in} (which is equal to its source-bulk voltage) increases. Note that as V_{in} is at *higher* level, the NMOS turns off *earlier* due to the finite clock slope, but the body effect (the increase of V_{thn}) makes the turn off time *later*. Thus the body effect makes the sampling time error (between the sampling timings for higher and lower levels of V_{in}) smaller, and hence it helps improve SDR given by Eq. (12). Since the amount of the body effect depends on MOS process (substrate doping density) and is nonlinear, we just point out this qualitatively.

2.2 NMOS Differential Sampling Circuit

Now consider a differential sampling circuit (Fig. 3(a)), and Fig. 6 illustrates ideal and actual sampling points. Similarly we have their sampled outputs:

$$V_{outp}(t) \approx \frac{A}{2}\sin\left(\omega t + \frac{\phi(t)}{2}\right) + M, \tag{14}$$

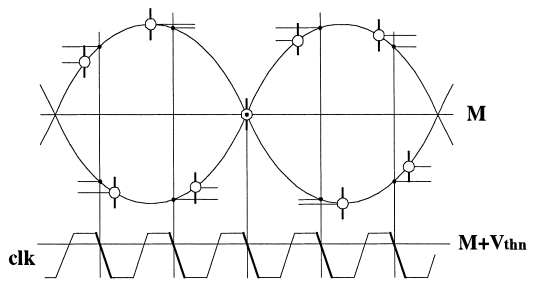

Fig. 6 Ideal (·) and actual (∘) sampling points in a differential NMOS sampling circuit.

$$V_{outm}(t) \approx -\frac{A}{2}\sin\left(\omega t - \frac{\phi(t)}{2}\right) + M. \tag{15}$$

Then Eqs. (14), (15) give us the differential output:

$$\begin{aligned} V_{out}(t) &:= V_{outp}(t) - V_{outm}(t) \\ &= \frac{A}{2}\left[\sin\left(\omega t - \frac{\phi(t)}{2}\right) + \sin\left(\omega t + \frac{\phi(t)}{2}\right)\right] \\ &= A\sin(\omega t)\cos\left(\frac{\phi(t)}{2}\right) \\ &\approx A\sin(\omega t)\cdot\left(1 - \frac{1}{8}\phi(t)^2\right) \\ &= A\left(1 - \frac{3A^2\omega^2 t_{TR}^2}{32V_{dd}^2}\right)\cdot\sin(\omega t) + \frac{A^3\omega^2 t_{TR}^2}{32V_{dd}^2}\sin(3\omega t) \\ &\approx A\sin(\omega t) + \frac{A^3\omega^2 t_{TR}^2}{32V_{dd}^2}\sin(3\omega t). \end{aligned} \tag{16}$$

We see from Eq. (16) that the second harmonics (which is the most dominant error in the NMOS single-ended sampler case) is cancelled, and we have

$$\begin{aligned} SDR &= 20\log_{10}\frac{32V_{dd}^2}{A^2\omega^2 t_{TR}^2} \\ &= 2\left[20\log_{10}\frac{2V_{dd}}{A\omega t_{TR}}\right] + 18\ [\mathrm{dB}]. \end{aligned} \tag{17}$$

Next we will consider the case that plus-path clock (*clkp*) and minus-path clock (*clkm*) in Fig. 3(b) has a finite skew of t_{skw}. We have

$$V_{outp}(t) \approx \frac{A}{2}\sin\left(\omega t + \frac{1}{2}(\phi(t) - \omega t_{skw})\right) + M, \tag{18}$$

$$V_{outm}(t) \approx -\frac{A}{2}\sin\left(\omega t - \frac{1}{2}(\phi(t - \omega t_{skw})\right) + M. \tag{19}$$

From Eqs. (18),(19), the differential output is given by

$$\begin{aligned} V_{out}(t) &:= V_{outp}(t) - V_{outm}(t) \\ &\approx a_0 + A\sin(\omega t) + a_2\cos(2\omega t) + b_3\sin(3\omega t) \end{aligned} \tag{20}$$

where $a_0 := -\alpha\beta$, $a_2 := \alpha\beta$, $b_3 := \alpha/8$,

$$\alpha := \frac{A^3\omega^2 t_{TR}^2}{4V_{dd}^2}, \qquad \beta := \frac{V_{dd}t_{skw}}{2At_{TR}}.$$

Also it follows from Eq. (20) that SDR is given by

$$\begin{aligned} SDR &= 10\log_{10}\frac{A^2/2}{a_0^2 + (a_2^2 + b_3^2)/2} \\ &= 2\left[20\log_{10}\frac{2V_{dd}}{A\omega t_{TR}}\right] + 18 \\ &\quad - 10\log_{10}(64\beta^2 + 1)\ [\mathrm{dB}]. \end{aligned} \tag{21}$$

Remark : Similar results described in Sect. 2 can be obtained for the PMOS sampling circuit in Fig. 1(b).

3. CMOS Sampling Circuit

Consider the CMOS sampling circuit in Fig. 1(c).

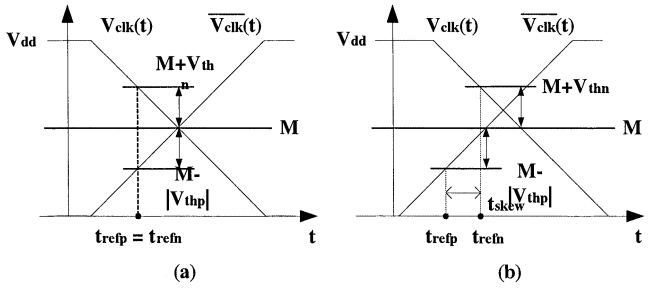

Fig. 7 Sampling clocks V_{clk}, $\overline{V_{clk}}$ in a CMOS sampling circuit. (a) Without skew. (b) With skew of t_{skew} between V_{clk} and $\overline{V_{clk}}$.

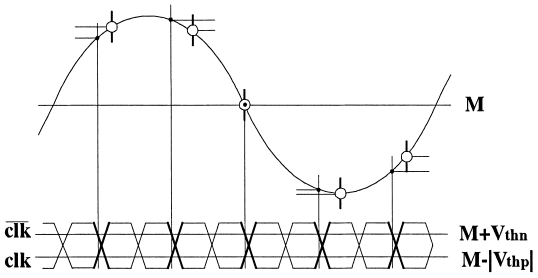

Fig. 8 Ideal (·) and actual (○) sampling points in a single-ended CMOS sampler without clock skew.

3.1 Zero Clock Skew Case

Suppose that there is no skew between NMOS clock (V_{clk}) and PMOS clock ($\overline{V_{clk}}$); in other words $t_{\rm refn} = t_{\rm refp}$ as shown in Fig. 7(a). The time when $V_{clk}(t) = M + V_{thn}$ and the one when $\overline{V_{clk}}(t) = M - |V_{thp}|$ are the same.

A. CMOS Single-Ended Sampling Circuit: Figure 8 illustrates ideal and actual sampling points. First, let us consider a CMOS single-ended sampler in Fig. 1(c). Noting that the CMOS switch is off when both NMOS and PMOS switches are off, we have the sampled output as follows:

$$\begin{aligned} V_{out}(t) &\approx A\sin(\omega t + |\phi(t)|) + M \\ &= A\left[\sin(\omega t)\cos(|\phi(t)|) + \cos(\omega t)\sin(|\phi(t)|)\right] + M \\ &\approx A\left[\sin(\omega t)(1 - \frac{1}{2}\phi(t)^2) + \cos(\omega t)\cdot|\phi(t)|\right] + M \\ &\approx A\left(1 - \frac{3A^2\omega^2 t_{TR}^2}{8V_{dd}^2}\right)\sin(\omega t) + \frac{A^3\omega^2 t_{TR}^2}{8V_{dd}^2}\sin(3\omega t) \\ &\quad + \frac{A^2\omega t_{TR}}{V_{dd}}\cos(\omega t)|\sin(\omega t)| + M. \end{aligned} \tag{22}$$

Noting that

$$|\sin(\omega t)| = \frac{2}{\pi}\left[1 - 2\sum_{n=1}^{\infty}\frac{\cos(2n\omega t)}{4n^2-1}\right],$$

Eq. (22) yields to the following:

$$\begin{aligned} V_{out}(t) &\approx A\sin(\omega t) \\ &\quad -\frac{4A^2\omega t_{TR}}{3\pi V_{dd}}\cos(\omega t)\cos(2\omega t) + M \end{aligned}$$

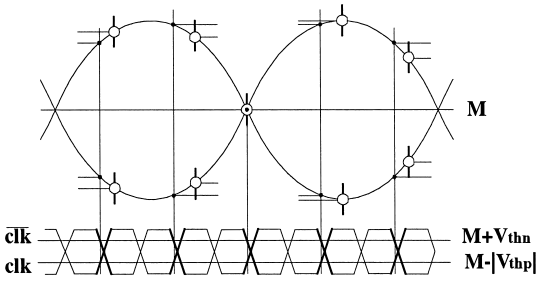

Fig. 9 Ideal (·) and actual (○) sampling points in a differential CMOS sampler without clock skew.

$$\approx A\sin(\omega t) - \frac{2A^2\omega t_{TR}}{3\pi V_{dd}}\cos(3\omega t) + M. \tag{23}$$

We see from Eq. (23) that the dominant harmonics of $V_{out}(t)$ is the third one, and even-order one is negligible. Also SDR is given by

$$\begin{aligned} SDR &= 20\log_{10}\frac{3\pi V_{dd}}{2A\omega t_{TR}} \\ &= 20\log_{10}\frac{2V_{dd}}{A\omega t_{TR}} + 7.44\ [\text{dB}]. \end{aligned} \tag{24}$$

B. CMOS Differential Sampling Circuit: For a differential circuit, the sampled outputs are given by

$$V_{outp}(t) \approx \frac{A}{2}\sin\left(\omega t + \frac{|\phi(t)|}{2}\right) + M,$$

$$V_{outm}(t) \approx -\frac{A}{2}\sin\left(\omega t + \frac{|\phi(t)|}{2}\right) + M,$$

$$\begin{aligned} V_{out}(t) &:= V_{outp}(t) - V_{outm}(t) \\ &= A\sin\left(\omega t + \frac{|\phi(t)|}{2}\right) \\ &\approx A\sin(\omega t) - \frac{A^2\omega t_{TR}}{3\pi V_{dd}}\cos(3\omega t). \end{aligned} \tag{25}$$

Then we have the following from Eq. (25):

$$\begin{aligned} SDR &= 20\log_{10}\frac{3\pi V_{dd}}{A\omega t_{TR}} \\ &= 20\log_{10}\frac{2V_{dd}}{A\omega t_{TR}} + 13.46\ [\text{dB}]. \end{aligned} \tag{26}$$

Figure 9 illustrates ideal and actual sampling points. We see that the phase modulation index (the intensity of the phase modulation) due to the input-dependent sampling-time error is reduced by a factor of 2. However, the harmonics caused by it are not cancelled because all of them are odd harmonics; using a differential circuit does not help reduce the harmonics caused by input-dependent sampling-time error in a CMOS sampling circuit without skew.

3.2 Finite Clock Skew Case

Suppose that there is a finite timing skew t_{skew} between V_{clk} and $\overline{V_{clk}}$ ($t_{skew} := t_{\rm refn} - t_{\rm refp} \neq 0$ as shown in Fig. 7(b)) and

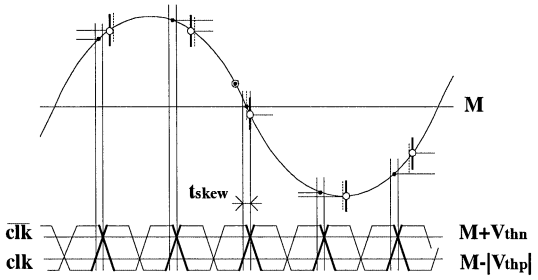

Fig. 10 Ideal (·) and actual (○) sampling points in a single-ended CMOS sampler with clock skew of t_{skew}.

$\omega t_{skew} \ll 1$. Note that the clocks for NMOS and PMOS switches are respectively given by

$$V_{clk}(t) = -\frac{V_{dd}}{t_{TR}}\left(t - t_{sn} - \frac{t_{skew}}{2}\right) + V_{dd}, \tag{27}$$

$$\overline{V_{clk}}(t) = \frac{V_{dd}}{t_{TR}}\left(t - t_{sp} + \frac{t_{skew}}{2}\right). \tag{28}$$

Then it follows from Eqs. (27), (28) that the turn-off timings of NMOS and PMOS switches are given by

$$t_{sn} + \delta t_n = t_{\mathrm{refn}} + \delta t'_n + \frac{t_{skew}}{2}, \tag{29}$$

$$t_{sp} + \delta t_p = t_{\mathrm{refp}} + \delta t'_p - \frac{t_{skew}}{2}. \tag{30}$$

A. CMOS Single-Ended Sampling Circuit: Figure 10 illustrates ideal and actual sampling points. It follows from Eqs. (10),(29) that we have the sampled output:

$$\begin{aligned} V_{out}(t) &\approx A\sin\left(\omega t + \left|\phi(t) + \frac{\omega t_{skew}}{2}\right|\right) + M \\ &= A\left[\sin(\omega t)\cos\left(\left|\phi(t) + \frac{\omega t_{skew}}{2}\right|\right)\right. \\ &\quad \left. + \cos(\omega t)\sin\left(\left|\phi(t) + \frac{\omega t_{skew}}{2}\right|\right)\right] + M \\ &\approx A\sin(\omega t)\left(1 - \frac{1}{2}\left(\phi(t) + \frac{\omega t_{skew}}{2}\right)^2\right) \\ &\quad + A\cos(\omega t)\left|\phi(t) + \frac{\omega t_{skew}}{2}\right| + M. \end{aligned} \tag{31}$$

Let

$$\epsilon := (V_{dd} t_{skew})/(2A t_{TR}),$$

and note that in case that $-1 \le \epsilon \le 1$,

$$\begin{aligned} &\left|\phi(t) + \frac{\omega t_{skew}}{2}\right| \\ &= \left|\frac{A\omega t_{TR}}{V_{dd}}\sin(\omega t) - \frac{\omega t_{skew}}{2}\right| \\ &= \frac{A\omega t_{TR}}{V_{dd}}|\sin(\omega t) - \epsilon| \\ &\approx \frac{2A\omega t_{TR}}{\pi V_{dd}}\left[\sqrt{1-\epsilon^2} + \epsilon\sin^{-1}(\epsilon)\right. \\ &\quad \left. - \left[\sin^{-1}(\epsilon) + 3\epsilon\sqrt{1-\epsilon^2}\right]\sin(\omega t)\right. \\ &\quad \left. - \frac{2}{3}(1+5\epsilon^2)\sqrt{1-\epsilon^2}\cos(2\omega t)\right], \end{aligned} \tag{32}$$

in case that $1 \le \epsilon$,

$$\left|\phi(t) + \frac{\omega t_{skew}}{2}\right| = -\frac{A\omega t_{TR}}{V_{dd}}(\sin(\omega t) - \epsilon), \tag{33}$$

and in case that $\epsilon \le -1$,

$$\left|\phi(t) + \frac{\omega t_{skew}}{2}\right| = \frac{A\omega t_{TR}}{V_{dd}}(\sin(\omega t) - \epsilon). \tag{34}$$

Then we have the following:
(i) In case that $-1 \le \epsilon \le 1$: Eqs. (10), (31), (32) give us

$$\begin{aligned} V_{out}(t) &\approx A\sin(\omega t) \\ &\quad + \frac{2A^2\omega t_{TR}}{\pi A}\left[\sqrt{1-\epsilon^2} + \epsilon\sin^{-1}(\epsilon)\right. \\ &\quad \left. - \frac{1}{3}(1+5\epsilon^2)\sqrt{1-\epsilon^2}\right]\cos(\omega t) \\ &\quad - \frac{A^2\omega t_{TR}}{\pi V_{dd}}\left[\sin^{-1}(\epsilon) + 3\epsilon\sqrt{1-\epsilon^2}\right]\sin(2\omega t) \\ &\quad - \frac{2A^2\omega t_{TR}}{3\pi V_{dd}}(1+5\epsilon^2)\sqrt{1-\epsilon^2}\cos(3\omega t) + M. \\ SDR &= 20\log_{10}\frac{2V_{dd}}{A\omega t_{TR}} + 7.44 - 10\log_{10}\gamma\ [\mathrm{dB}]. \end{aligned} \tag{35}$$

Here

$$\begin{aligned} \gamma :=\ & \frac{9}{4}\sin^{-2}(\epsilon) + \frac{27}{2}\sqrt{1-\epsilon^2}\sin^{-1}(\epsilon) \\ & + \left[(1+5\epsilon^2)^2 + \frac{81}{4}\epsilon^2\right](1-\epsilon^2). \end{aligned}$$

(ii) In case that $\epsilon \ge 1$: Eqs. (31), (33) give us

$$\begin{aligned} V_{out}(t) &\approx A\sin(\omega t) - \frac{A^2\omega t_{TR}}{2V_{dd}}\sin(2\omega t) + M. \\ SDR &= 20\log_{10}\frac{2V_{dd}}{A\omega t_{TR}}\ [\mathrm{dB}]. \end{aligned} \tag{36}$$

This corresponds to the NMOS sampling circuit case.

(iii) In case that $\epsilon \le -1$: Eqs. (31), (34) give us

$$\begin{aligned} V_{out}(t) &\approx A\sin(\omega t) + \frac{A^2\omega t_{TR}}{2V_{dd}}\sin(2\omega t) + M. \\ SDR &= 20\log_{10}\frac{2V_{dd}}{A\omega t_{TR}}\ [\mathrm{dB}]. \end{aligned} \tag{37}$$

This corresponds to the PMOS sampling circuit case.
This corresponds to the NMOS or PMOS sampling circuit case. Also we see from Eqs. (38),(40) that even-order harmonics are cancelled.

B. CMOS Differential Sampling Circuit: Figure 11 illustrates ideal and actual sampling points. It follows from Eqs. (10), (29), (30) that we have the sampled outputs

$$V_{outp}(t) \approx \frac{A}{2}\sin\left(\omega t + \frac{1}{2}|\phi(t) + \omega t_{skew}|\right) + M,$$

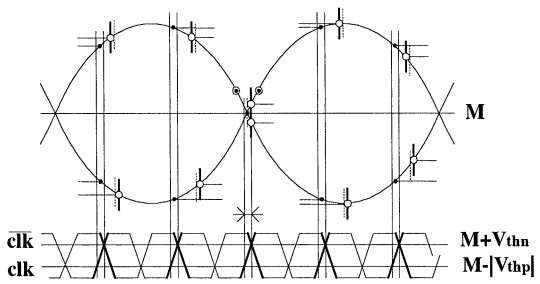

Fig. 11 Ideal (·) and actual (○) sampling points in a differential CMOS sampler with clock skew of t_{skew}.

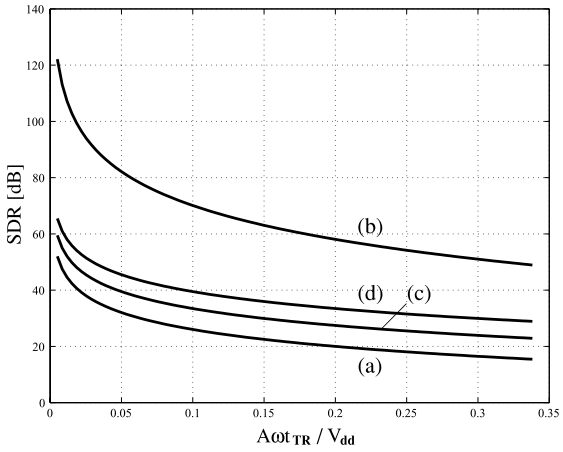

Fig. 12 Calculated SDR based on derived formulas versus $A\omega t_{TR}/V_{dd}$. (a) A single-ended NMOS sampler. (b) A differential NMOS sampler. (c) A single-ended CMOS sampler without clock skew. (d) A differential CMOS sampler without clock skew.

$$V_{outm}(t) \approx -\frac{A}{2}\sin\left(\omega t + \frac{1}{2}|\phi(t) - \omega t_{skew}|\right) + M,$$

$$V_{out}(t) := V_{outp}(t) - V_{outm}(t)$$

$$\approx A\sin\left(\omega t + \frac{1}{4}\{|\phi(t) + \omega t_{skew}| + |\phi(t) - \omega t_{skew}|\}\right)$$

$$\times\cos\left(\frac{1}{4}\{|\phi(t) + \omega t_{skew}| - |\phi(t) - \omega t_{skew}|\}\right).$$

(i) In case $-1/2 \le \epsilon \le 1/2$:

$$V_{out}(t) \approx A\sin(\omega t) + c_3\cos(3\omega t) + d_3\sin(3\omega t) \tag{38}$$

where

$$c_3 := -\frac{A^2\omega t_{TR}}{3\pi V_{dd}}(1 + 20\epsilon^2)\sqrt{1 - 4\epsilon^2},$$

$$d_3 := \frac{A^3\omega^2 t_{TR}^2}{8\pi^2 V_{dd}^2}\sin^{-2}(2\epsilon).$$

$$SDR = 10\log_{10}\frac{A^2}{c_3^2 + d_3^2}\ [\text{dB}]. \tag{39}$$

(ii) In case $\epsilon \le -1/2$ or $\epsilon \ge 1/2$:

$$V_{out}(t) \approx A\sin(\omega t) + \frac{A^3\omega^2 t_{TR}^2}{32V_{dd}^2}\sin(3\omega t). \tag{40}$$

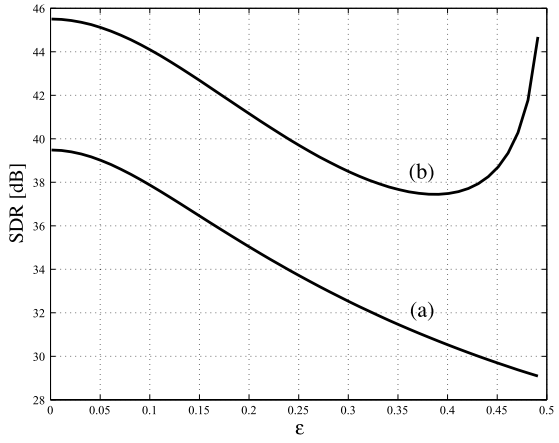

Fig. 13 Calculated SDR based on derived formulas versus clock skew in CMOS sampling circuits. The horizontal axis indicates $\epsilon := (V_{dd}t_{skew})/(2At_{TR})$, where $A\omega t_{TR}/V_{dd} = 0.05$. (a) A single-ended CMOS sampler with clock skew. (b) A differential CMOS sampler with clock skew. The SDR curve (b) increases for a large ϵ; this is because as ϵ increases the second-harmonics (which can be cancelled by a differential topology) increases while the third-harmonics decreases. Note that for a very large ϵ, the CMOS sampling circuit becomes equivalent to the NMOS (or PMOS) sampling circuit.

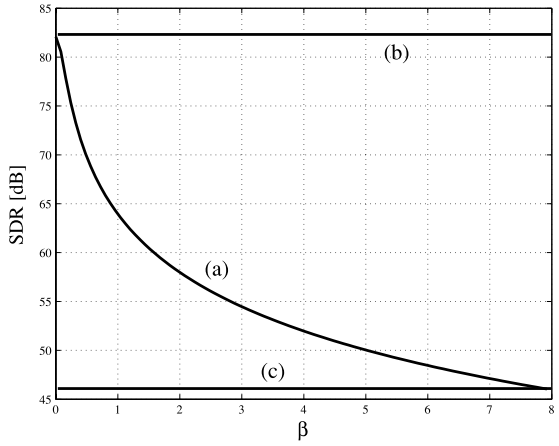

Fig. 14 Calculated SDR based on derived formulas versus clock skew in differential NMOS sampling circuits. The horizontal axis indicates $\beta := (V_{dd}t_{skw})/(2At_{TR})$, where $A\omega t_{TR}/V_{dd} = 0.05$. (a) A differential NMOS sampler with clock skew. (b) A differential NMOS sampler without clock skew. (c) A differential CMOS sampler without clock skew.

$$SDR = 20\log_{10}\frac{32V_{dd}^2}{A^2\omega^2 t_{TR}^2}\ [\text{dB}]. \tag{41}$$

Figures 12, 13 and 14 show numerical simulation results of SDR due to the input-dependent sampling time error; Fig. 12 is based on Eqs. (12), (17), (24), (26), and Fig. 13 uses Eqs. (35)–(37), (39), (41), while Fig. 14 is given by Eqs. (17), (21), (26).

4. Conclusion

We have analyzed the input-dependent sample-time error in MOS sampling circuits caused by the finite slope of the sampling clock and clarified the followings:

- Input-dependent sampling-time error causes phase modulation in the sampled data.
- The formulas for SDR due to such sampling errors are explicitly derived.
- NMOS sampling circuits generate even-order harmonics, which are greatly reduced by using a differential topology.
- CMOS sampling circuits *without* clock skew between V_{clk} and $\overline{V_{clk}}$ generate odd-order harmonics which a differential topology cannot help cancel, whereas circuits *with* clock skew generate even-order as well as odd-order harmonics.
- For single-ended sampling circuits, the SDR of CMOS circuits *without* clock skew is better than that of NMOS circuits.
- NMOS differential sampling circuits are relatively insensitive to input-dependent sampling-time error effects, which would be the best regarding to the input-dependent sampling-time error effects.
- Its effects in case of NMOS differential samplers with finite skew between plus and minus path clocks are discussed.
- Its effects in CMOS samplers with finite skew between PMOS and NMOS clocks are discussed.

These results can be used to estimate a required slope of the sampling clock for a specified SDR of MOS samplers, as well as allowable clock skews in CMOS single-ended samplers, and NMOS, CMOS differential samplers.

Acknowledgement

We would like to thank STARC which is supporting this research. Thanks are also due to K. Wilkinson for valuable discussions.

References

[1] K. Poulton, R. Neff, A. Muto, W. Liu, A. Burstein, and M. Heshami, "A 4 GS/s 8b ADC in 0.35 μm CMOS," ISSCC Tech. Digest, vol.45, pp.166–167, Feb. 2002.

[2] M. Choi and A.A. Abidi, "A 6-b 1.3 GS/s A/D converter in 0.35 μm CMOS," IEEE J. Solid-State Circuits, vol.36, no.12, pp.1847–1858, Dec. 2001.

[3] D. Johns and K. Martin, Analog Integrated Circuit Design, John Wiley & Sons, 1997.

[4] P.J. Lim and B.A. Wooley, "A high-speed sample-and-hold technique using a miller hold capacitance," IEEE J. Solid-State Circuits, vol.26, no.4, pp.643–651, April 1991.

[5] H. Kobayashi, K. Kobayashi, M. Morimura, Y. Onaya, Y. Takahashi, K. Enomoto, and H. Kogure, "Sampling jitter and finite aperture time effects in wideband data acquisition systems," IEICE Trans. Fundamentals, vol.E85-A, no.2, pp.335–346, Feb. 2002.

[6] N. Kurosawa, H. Kobayashi, H. Kogure, T. Komuro, and H. Sakayori, "Sampling clock jitter effects in digital-to-analog converters," Measurement, vol.31, no.3, pp.187–199, March 2002.