IEICE TRANS. ELECTRON., VOL.E88–C, NO.6 JUNE 2005

LETTER *Special Section on Analog Circuit and Device Technologies*

Reducing Spurious Output of Balanced Modulators by Dynamic Matching of I, Q Quadrature Paths

Jun OTSUKI[†], *Nonmember*, **Hao SAN**[†], *Student Member*, **Haruo KOBAYASHI**[†a)], *Member*, **Takanori KOMURO**[†], **Yoshihisa YAMADA**[†], *and* **Aiyan LIU**[†], *Nonmembers*

SUMMARY This paper presents a technique for reducing spurious output of balanced modulators used in transmitters and arbitrary waveform generators. Two-step upconversion is a convenient way to produce a desired single-sideband (SSB) radio-frequency (RF) signal—baseband quadrature I and Q signals (which are analog outputs of direct digital frequency synthesizers) are upconverted by mixers and local oscillators (LOs)—but mismatches between the DACs in I and Q paths cause spurious output. We propose a method of dynamically matching the I and Q paths by multiplexing two DACs between I and Q paths in a pseudo-random manner. MATLAB simulation shows that multiplexing the two DACs spreads the spurious output, caused by mismatches between the two DACs, in the frequency domain, and reduces the peak level of spurious signals.

key words: *Cartesian transmitter, arbitrary waveform generator, IQ mismatch, SFDR, spread spectrum*

1. Introduction

The ratio of maximum output signal level to the peak level of spurious output (Spurious Free Dynamic Range: SFDR, or Maximum Distortion-Free Dynamic Range [1]) is an important measure of the performance of transmitter circuits (Fig. 1). Pure sinusoidal signals with a low level of spurious output are also required from measuring instruments such as signal generators and arbitrary waveform generators. The two-step upconversion transmitter architecture is widely used for mobile SSB transmitter circuits and for SSB signal generators. In the two step upconversion architecture (and in general, for Cartesian upconversion transmitters), I, Q direct digital frequency synthesizers perform digital modulation, and two DACs generate baseband I and Q analog signals. The two analog signals are then phase shifted by mixers and LOs, and upconvered to produce the desired SSB RF signal. Fig. 2 shows a two-step transmitter architecture for quadrature upconversion [2]. Here the frequency of the baseband DAC output signals is ω_0, and the I, Q signals $\cos(\omega_0 t)$ and $\sin(\omega_0 t)$ are in quadrature phase. By using two LO frequencies ω_1 and ω_2, and either adding or subtracting the phases, a desired SSB output signal of frequency $\omega_0 + \omega_1 + \omega_2$ can be generated. The two-step upconversion architecture is an effective way to generate SSB if perfect quadrature phase and perfect gain matching are assumed. However, in practice there are mismatches between I and Q paths which result in spurious output [3], [4]. For example, there are mismatches such as gain mismatch and timing skew between the two DACs, gain mismatches of mixers, phase errors from LOs whose phases should be ideally 90^o apart for quadrature sine and cosine signals. Therefore, as well as the desired signal, image signals also appear at the signal generator output. In transmitters, such image signals may interfere with other transmitter channels; in arbitrary waveform generators, they represent spurious output. Complicated analog bandpass filters may be required to remove such image signals; filter complexity, size, and power dissipation may result in a larger and more expensive product.

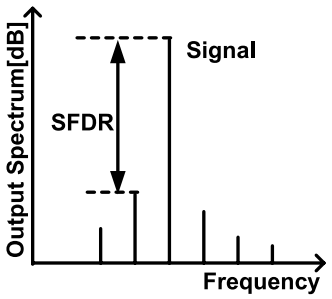

Fig. 1 Spurious Free Dynamic Range (SFDR): the ratio of maximum signal power to maximum spurious output power. In the graph this is shown as the difference of two powers, because the Y-axis scale is in decibels.

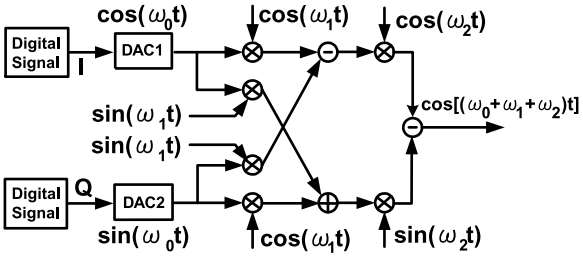

Fig. 2 Two-step upconversion SSB generator architecture.

In receiver circuits, also, mismatches between I and Q paths adversely affect performance [3], [4]. However, I and Q paths mismatches in receivers can be partially compensated for by digital signal processing techniques, thus some degree of mismatch is tolerable. In transmitter circuits, on the other hand, because the output of the signal generator is an analog signal, the use of direct digital calibration techniques for compensation of mismatch may not be feasible.

This paper describes a digital dynamic matching tech-

Manuscript received October 27, 2004.
Manuscript revised January 17, 2005.

[†]The authors are with the Department of Electronic Engineering, Faculty of Engineering, Gunma University, Kiryu-shi, 376-8515 Japan.
a) E-mail: k_haruo@el.gunma-u.ac.jp

DOI: 10.1093/ietele/e88–c.6.1290

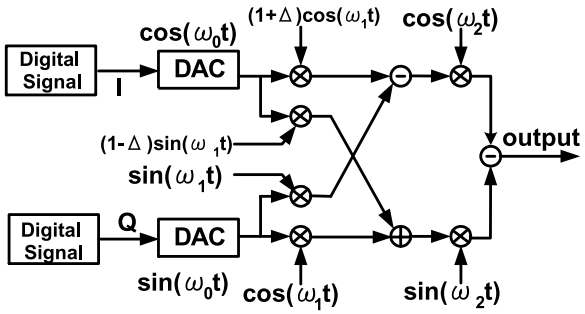

Fig. 3 A two-step upconversion transmitter based on Fig. 2 with 2Δ gain mismatches between the mixer pairs.

nique for improving SFDR (Fig. 1) in high-frequency signal generators. Our proposed method suppresses the spurious output caused by mismatches between two DACs and hence enables simpler analog filters to be used in the signal generator. In this paper, we mainly consider the two-step transmitter architecture in Fig. 2, however the proposed technique is also applicable to one-step transmitter architectures.

Throughout this paper,we used the parameters of $\omega_0/(2\pi) = 15\,MHz$, $\omega_1/(2\pi) = 1\,GHz$, $\omega_2/(2\pi) = 4\,GHz$ in our MATLAB simulation.

2. Spurious Output Caused by Mismatches in I, Q-Paths

Consider the two-step transmitter architecture in Fig. 2. In a practical implementation, mismatches between I and Q paths cannot be avoided, which results in spurious output. We confirmed this effect by the following simulation:

1. Figure 3 shows a two-step upconverter transmitter with a gain mismatch for in mixer pairs (or amplitude error between sine and cosine waveforms in LO). Figure 4 shows its output power spectrum, where Δ in Fig. 3 is 0.01. We see that spurious output is −52 dB, 46 dB below the signal level.
2. Figure 5 shows a transmitter with mismatches in gain, offset, 2nd-order harmonics, 3rd-order harmonics and timing skew between the two DACs. The simulation was performed with the condition that $a_0 = 0.0045$, $a_1 = 0.995$, $a_2 = 0.0045$, $a_3 = 0.0046$, $b_0 = 0.0055$, $b_1 = 1.005$, $b_2 = 0.0055$, $b_3 = 0.0054$ and $dt = 100\,ps$. Figure 6 shows its output power spectrum, and we see that several spurious spikes appear in the spectrum, and the highest is only 24 dB below the signal.

3. Proposed Technique for Suppressing Spurious Outputs

In the two-step upconversion transmitter architecture, the two DAC circuits are larger than other circuits, so it is more difficult to get perfect matching between the two DACs. Also their analog output signals are at relatively low frequencies. So we propose the new configuration shown in Fig. 7 to reduce the effect of mismatches between two DACs. At some timing, DAC1 is used for the I path (upper path) while DAC2 is used for the Q path (lower path). At other timing, DAC1 is used for the Q path, while DAC2 is used for the I path. In our proposed configuration, we

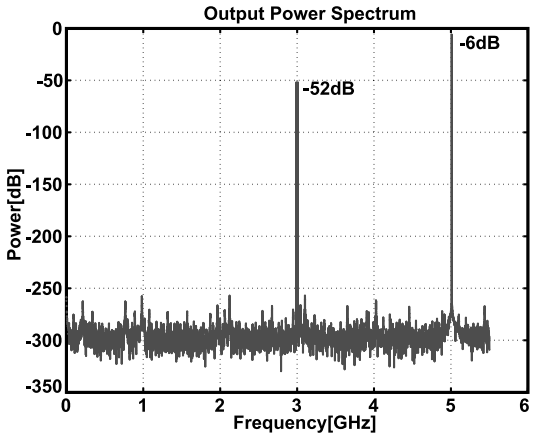

Fig. 4 Output power spectrum of Fig. 3 with 2Δ = 0.02 gain mismatches between mixer pairs. Output signal power is −6 dB@5.015 GHz, and spurious peak is −52 dB@3 GHz, 46 dB below signal level.

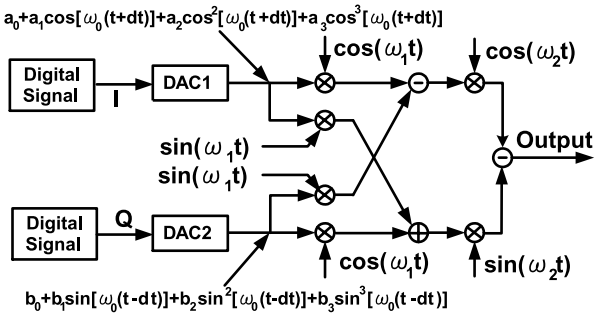

Fig. 5 A two-step upconversion transmitter with gain, offset, 2nd-order harmonics, 3rd-order harmonics mismatches and timing skew between two DACs.

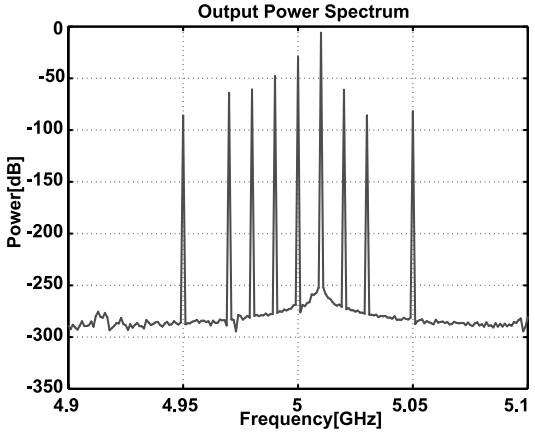

Fig. 6 Output spectrum of Fig. 5 with gain, offset, 2nd-order harmonics, 3rd-order harmonics mismatches and timing skew between two DACs. Several spurious outputs appear, with a peak at 24 dB below the signal.

alternate between the above two configurations of DAC1 and DAC2 in a pseudo-random manner. To implement this mechanism, two digital multiplexer (MUX) circuits are added between the two digital signal generators and the two DAC inputs, while two analog MUXs are added between the two DAC outputs and the following I and Q paths. The select signals of the two digital and analog MUXs are generated by a digital pseudo-random signal generator (such as an M-sequence generator), and synchronized; the digital pseudo-random signal generator could be relatively low power and easy to implement because it operates with the same clock rate of the DAC sampling clock, which would be a few hundreds of MHz in actual implementation. This results in spurious output caused by mismatches between DAC1 and DAC2 being spread in the frequency domain, and the peak spurious signal is reduced relative to the signal level.

Figure 8 shows an example of gain and timing mismatches between the two DACs.

Note that such spectrum spreading techniques have been used in other circuits:

1. In [1] and [7], selection of unit cells in a segmented DAC is dynamically changed to reduce the effect of DAC nonlinearity by spreading spurious output, caused by mismatches among the unit cells, in the frequency domain.
2. In [8], the effects of DC offset in a direct conversion mixer are reduced by a chopping technique.
3. In [9], a random-interleaved method is proposed for interleaved ADC systems; an extra ADC was added and the spurious output caused by mismatches among different channels is spread in the frequency domain.
4. In [10], pseudo-random dithering of switch timing for switching regulators is used to spread the spurious output spectrum.
5. In [11], random dithering of clock timing for digital LSIs is used to spread the clock spectrum.

However, to the best of our knowledge, our paper is the first proposal for using I, Q-path multiplexing (dynamic matching) in Cartesian signal generators to reduce spurious output.

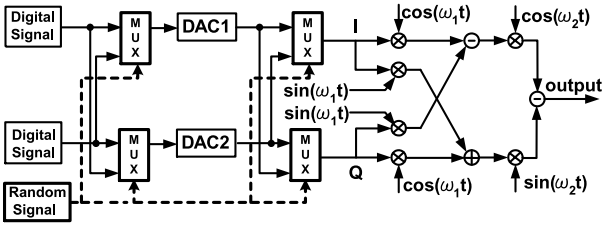

Fig. 7 Proposed dynamic matching technique configuration.

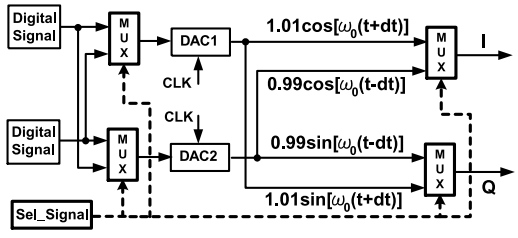

Fig. 8 Internal signals when the proposed method is employed. Here gain (1.01, 0.99) and timing (dt, $-dt$) mismatches between two DACs are considered.

4. Simulation Results

We have conducted MATLAB simulations to confirm the effectiveness of the proposed dynamic matching technique. We assume x_1, x_2 as inputs, y_1, y_2 as outputs of DAC1 and DAC2, and then we can approximate their input-output characteristics as follows:

$$y_1 = a_0 + a_1 x_1 + a_2 x_1^2 + a_3 x_1^3 \quad (1)$$

$$y_2 = b_0 + b_1 x_2 + b_2 x_2^2 + b_3 x_2^3. \quad (2)$$

Here, we consider mismatches as follows:

$$\begin{aligned} \text{offset error} \quad & a_0 \neq b_0, \\ \text{gain error} \quad & a_1 \neq b_1, \\ \text{2nd-order harmonic} \quad & a_2 \neq b_2, \\ \text{3rd-order harmonic} \quad & a_3 \neq b_3. \end{aligned}$$

We also consider timing skew between DAC1 and DAC2 sampling clocks as dt. In our simulation, we also take care of the quantization noise; we assume DACs of 10-bit resolution.

Figures 9 and 10 show output spectrum simulation results where gain and timing mismatches between two DACs are considered; we used the condition that $a_1 = 1.01$ and $b_1 = 0.99$ in Eqs. (1), (2) while the sampling clock timing skew dt between the two DACs is 100 ps. Also the MUX select frequency is 256 MHz in Fig. 7. We see that spurious output caused by mismatches between the two DACs are spectrum spread, and the spurious output peak is reduced

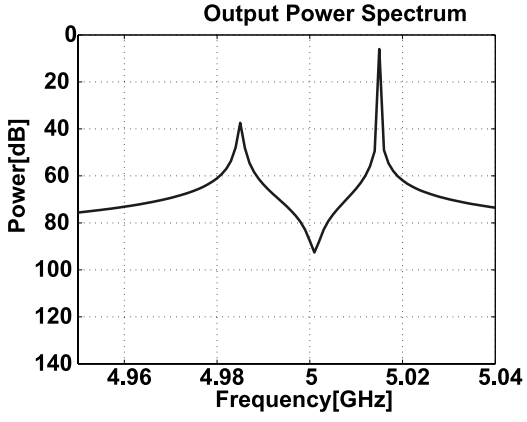

Fig. 9 Output spectrum for Fig. 2 with gain, timing mismatches between DACs, but without quantization noise. Signal power is −6.0 dB@5.015 GHz, peak spurious power is −37.4 dB@4.985 GHz, 31.4 dB below signal level.

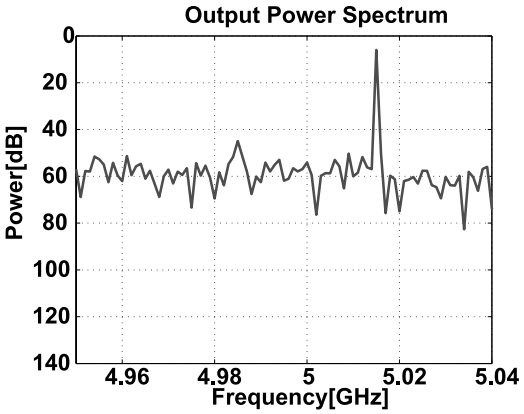

Fig. 10 Output spectrum with gain, timing mismatches between DACs, but *without* quantization noise, when the proposed dynamic matching shown in Fig. 8 is used. Signal power is −6.0 dB@5.015 GHz, peak spurious power is −44.9.3 dB@4.985 GHz and SFDR is 38.9 dB. Compared with Fig. 9, spurious peak output is reduced by 7.5 dB.

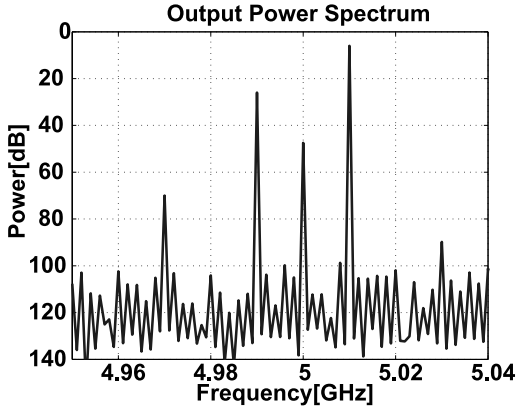

Fig. 11 Output spectrum for Fig. 2 with offset, gain, timing, 3rd-order harmonic mismatches between DACs as well as *with* quantization noise. Signal power is −6.0 dB@5.015 GHz, peak spurious power is −26.0 dB@4.985 GHz, 2nd spurious is −47.4 dB@5.0 GHz, and spurious peak is 20.0 dB below signal.

by 7.5 dB with our dynamic matching method. We use 10 bit resolution DACs in our simulation to evaluate effects of quantization noise, and found that finite DAC resolution (quantization noise) causes the noise floor to be raised but there is no direct connection between spurious output and quantization noise; we can consider the quantization noise of the DAC as white noise, and it does not have any effect on spurious output of the two-step upconversion transmitter when the proposed dynamic matching is applied.

We have also performed simulations with different parameter values for the offset, gain, timing, 3rd-order harmonic mismatches between two DACs: $a_0 = 0.045$, $a_1 = 0.9$, $a_2 = 0.0$, $a_3 = 0.000225$ in Eq. (1) and $b_0 = 0.055$, $b_1 = 1.1$, $b_2 = 0.0$, $b_3 = 0.00275$ in Eq. (2), while dt is 100 ps. Also the MUX select frequency is 256 MHz in Fig. 7. Then similar results are obtained; the proposed method spreads the spurious spectrum and reduces spurious peak levels as shown in Fig. 11 and Fig. 12.

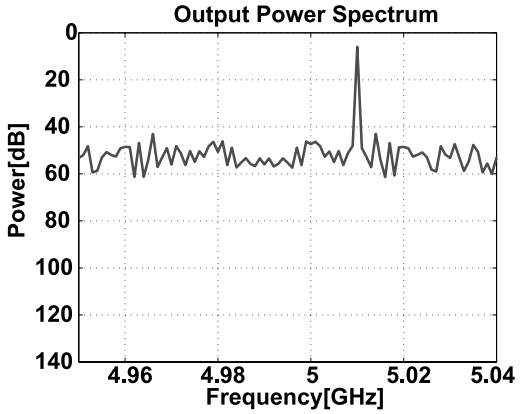

Fig. 12 Output spectrum for Fig. 7 with dynamic matching method, when offset, gain, timing and 3rd-order harmonic mismatches between DACs as well as quantization noise are considered. Signal power is −6.0 dB@5.015 GHz, peak spurious power is 43.0 dB@4.966 GHz, 37.0 dB below signal. Compared with Fig. 11, spectrum of 3rd-order harmonics is spread, and spurious signals reduced by 17.0 dB.

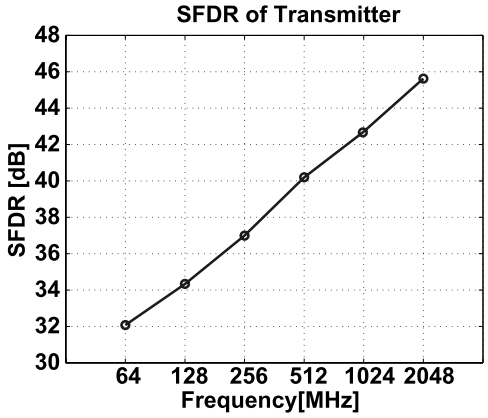

Fig. 13 Transmitter SFDR vs. MUX select signal frequency. We see that SFDR improves by 3 dB when the MUX select signal frequency doubles.

Remark

(i) Our simulations show that the spurious output caused by 2nd-order harmonics is *not* reduced by our proposed method. However in practical DAC implementation, differential circuits are used in most cases, so 2nd-order harmonics are small and 3rd-order harmonics are dominant. Therefore this does not affect the effectiveness of our method.

(ii) We have also performed simulations to know the effects of the MUX select signal freqquency with the same mismatch conditions as Figs. 11, 12; we found that the SFDR of the transmitter improves by 3 dB when the select frequency doubles (Fig. 13).

5. Conclusion

We have proposed a dynamic matching technique for reducing spurious output of modulators in signal generators used for transmitters and arbitrary waveform generators. We proposed a dynamic matching technique which alternates the two DACs in I and Q paths in a pseudo-random manner. The

validity of the proposed technique was confirmed by MATLAB simulation. The transmitter spurious output power spectrum caused by mismatches between the two DACs is spread in the frequency domain and spurious peak level is reduced by our proposed technique. The performance of signal generators can be improved simply by adding some digital circuitry and low frequency analog circuitry, which would be relatively easy to implement.

Next steps are as follows:

- Transistor level circuit design of a signal generator including the proposed dynamic matching technique.
- Confirmation of effectiveness of the proposed technique by SPICE simulation for the signal generator design.
- Consideration of the effect of mismatches between two analog MUXs; this may depend on the DAC implementation.
- Consideration of the effect of beat effects between input signals and sampling clocks of two DACs.
- Development of spurious suppression techniques to compensate for gain mismatches between mixers and phase errors between LOs.

Our approach here is to improve the performance of analog circuits using digital signal processing technique. We believe that such approaches are becoming more important as VLSI technology progresses and device sizes are scaled down, supply voltage is decreased (it will be below 1V in few years), which make it increasingly difficult to realize analog circuits with high dynamic range using only analog circuit techniques. On the other hand, digital circuits are becoming faster, cheaper and lower power, which makes it feasible to use rather complicated digital signal processing algorithms for improving analog circuit performance.

Acknowledgements

We would like to thank K. Wilkinson and K. Miyamoto for valuable discussions.

References

[1] R. van de Plassche, CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters, 2nd ed., Kluwer Academic Publishers, 2003.
[2] B. Razavi, "A 900-MHz/1.8-GHz CMOS transmitter for dual-band application," IEEE J. Solid-State Circuits, vol.34, no.5, pp.573–579, May 1999.
[3] B. Razavi, RF Microelectronics, Prentice Hall, 1998.
[4] T.H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press, 1998.
[5] A. Torosyan, D. Fu, and A.N. Willson, Jr., "A 300 MHz quadrature direct digital synthesizer/mixer in 0.25 μm CMOS," IEEE J. Solid-State Circuits, vol.38, no.6, pp.875–887, June 2003.
[6] L.K. Tan and H. Samueli, "A 200 MHz quadrature frequency synthesizer/mixer in 0.8 μm CMOS," IEEE J. Solid-State Circuits, vol.30, no.3, pp.193–200, March 1995.
[7] H. San, H. Kobayashi, S. Kawakami, and N. Kuroiwa, "A noise-shaping algorithm of multi-bit DAC nonlinearities in complex band-pass $\Delta\Sigma$AD modulators," IEICE Trans. Fundamentals, vol.E87-A, no.4, pp.792–800, April 2004.
[8] B. Bautista, B. Bastani, and J. Heck, "A high IIP2 down conversion mixer using dynamic matching," IEEE J. Solid-State Circuits, vol.35, no.12, pp.1934–1941, Dec. 2000.
[9] M. Tamba, A. Shimizu, H. Munakata, and T. Komuro, "A method to improve SFDR with random interleaved sampling method," Proc. International Test Conference, pp.512–520, 2001.
[10] T. Daimon, H. Sadamura, T. Shindou, H. Kobayashi, M. Kono, T. Myono, T. Suzuki, S. Kawai, and T. Iijima, "Spread-spectrum clocking in switching regulators for EMI reduction," IEICE Trans. Fundamentals, vol.E86-A, no.2, pp.381–386, Feb. 2003.
[11] C.D. Hoekstra, "Frequency modulation of system clocks for EMI reduction," Hewlett-Packard J., article 13, pp.101–107, Aug. 1997.