PAPER   *Special Section on Analog Circuits and Related SoC Integration Technologies*

A Second-Order Multibit Complex Bandpass ΔΣAD Modulator with I, Q Dynamic Matching and DWA Algorithm

Hao SAN[†a)], *Member*, Yoshitaka JINGU[†], Hiroki WADA[†], Hiroyuki HAGIWARA[†],
Akira HAYAKAWA[†], *Nonmembers*, Haruo KOBAYASHI[†b)], Tatsuji MATSUURA[††], *Members*,
Kouichi YAHAGI[††], Junya KUDOH[††], *Nonmembers*, Hideo NAKANE[††], Masao HOTTA[†††],
Toshiro TSUKADA[††††], Koichiro MASHIKO[††††], *and* Atsushi WADA[†††††], *Members*

SUMMARY   We have designed, fabricated and measured a second-order multibit switched-capacitor complex bandpass ΔΣAD modulator to evaluate our new algorithms and architecture. We propose a new structure of a complex bandpass filter in the forward path with I, Q dynamic matching, that is equivalent to the conventional one but can be divided into two separate parts. As a result, the ΔΣ modulator, which employs our proposed complex filter can also be divided into two separate parts, and there are no signal lines crossing between the upper and lower paths formed by complex filters and feedback DACs. Therefore, the layout design of the modulator can be simplified. The two sets of signal paths and circuits in the modulator are changed between I and Q while CLK is changed between high and low by adding multiplexers. Symmetric circuits are used for I and Q paths at a certain period of time, and they are switched by multiplexers to those used for Q and I paths at another period of time. In this manner, the effect of mismatches between I and Q paths is reduced. Two nine-level quantizers and four DACs are used in the modulator for low-power implementations and higher signal-to-noise-and-distortion (SNDR), but the nonlinearities of DACs are not noise-shaped and the SNDR of the ΔΣAD modulator degrades. We have also employed a new complex bandpass data-weighted averaging (DWA) algorithm to suppress nonlinearity effects of multibit DACs in complex form to achieve high accuracy; it can be realized by just adding simple digital circuitry. To evaluate these algorithms and architecture, we have implemented a modulator using $0.18\,\mu$m CMOS technology for operation at 2.8 V power supply; it achieves a measured peak SNDR of 64.5 dB at 20 MS/s with a signal bandwidth of 78 kHz while dissipating 28.4 mW and occupying a chip area of $1.82\,\text{mm}^2$. These experimental results demonstrate the effectiveness of the above two algorithms, and the algorithms may be extended to other complex bandpass ΔΣAD modulators for application to low-IF receivers in wireless communication systems.
key words: *complex bandpass ΔΣAD modulator, I, Q path mismatches, dynamic matching, miltibit, data-weighted averaging*

1. Introduction

In the RF receiver of communication systems, low-IF receiver architecture is frequently used so that more receiver functions, such as multi standard and automatic gain control, can be moved to the digital part to provide more programmability. In conventional low-IF receiver architectures, two real (one input and one output) ΔΣAD modulators are used for in-phase (I) and quadrature (Q) paths. Its disadvantage is that not only input signals but also image signals are converted by ADCs. On the other hand, a complex bandpass ΔΣAD modulator can provide superior performance to a pair of real bandpass ΔΣAD modulators of the same order. It processes just input I and Q signals, not image signals, and AD conversion can be realized with low power dissipation. Thus, they are desirable for such low-IF receiver applications [1]–[5].

The use of a low-order multibit ΔΣAD modulator makes higher resolution possible with a low oversampling ratio (OSR), and the stability problem is alleviated. It is attractive for low-power implementations because it alleviates the slew-rate requirements of operational amplifiers with a high dynamic range in the modulator. However, multibit DACs cannot be made perfectly linear and their nonlinearity in the feedback paths are equivalent to errors added directly to the input signals; hence, they may degrade the SNDR of the ΔΣAD modulator. Then we developed a data-weighted averaging (DWA) algorithm for complex bandpass modulators [6], [7], which is implemented by just adding simple digital circuitry to suppress nonlinearity effects of multibit DACs in a complex form.

The performance of the complex bandpass ΔΣAD modulator is degraded by mismatches between I and Q paths, which cause both signal and quantization noise in the mirror image band and aliasing in the design signal band, thereby decreasing the SNDR of the complex modulator.

On the basis of the above consideration, we proposed new algorithms and a new architecture. We propose a new switched-capacitor topology architecture, that is suitable for complex bandpass ΔΣAD modulators and compensates for mismatches between I and Q paths. The new architecture reduces the amount of mirror image band quantization noise aliased into the signal band. Moreover, this technique can be extended to multibit modulators suitable for complex band-

Fig. 1 Block diagram of the complex bandpass ΔΣAD modulator.

Fig. 2 Conventional complex bandpass ΔΣAD modulator.

Fig. 3 (a) Basic complex bandpass filter. (b) Proposed equivalent implementation of a complex bandpass filter. (c) Operation of the proposed complex bandpass filter (state 1). (d) Operation of the proposed complex bandpass filter (state 2).

pass DWA algorithm [8], [9]. Furthermore, in the realization of complex ΔΣAD modulators, their layout design becomes complicated because of signal lines made to cross by complex filters and feedback from DACs for I and Q paths in the modulator, and this increases the required chip area. We propose a new structure for a complex bandpass ΔΣAD modulator, which has a symmetrical configuration that can be divided into two separate paths without crossing signal lines between the upper and lower circuit parts; thus, the required chip area is reduced and its layout design can be simplified.

In this paper, we present the chip implementation of a complex bandpass ΔΣAD modulator with switched-capacitor circuits, in order to evaluate the effectiveness of the above-mentioned two algorithms using a real chip.

2. Complex Bandpass ΔΣAD Modulator Architecture

A complex bandpass ΔΣAD modulator gains its advantage by implementing the poles and zeros of its loop filter without their conjugates, which are leaked in the image band for a complex single-side band signal. Figure 1 shows a simplified block diagram of the proposed complex bandpass ΔΣAD modulator (whose topology is derived from modifying that of a real lowpass ΔΣAD modulator in [10] by replacing z^{-1} with jz^{-1}); it is a second-order structure with two discrete-time complex integrators (or complex bandpass filters) and two nine-level quantizers surrounded by two feedback loops. The input and output of the complex bandpass ΔΣAD modulator can be expressed as

$$Y(z) = 0.5z^{-2}X(z) + (z - j)^2 z^{-2} E(z). \tag{1}$$

Then the signal transfer function (STF) and noise transfer function (NTF) of the complex modulator can be given by

$$STF(z) = 0.5z^{-2} \tag{2}$$

$$NTF(z) = (z - j)^2 z^{-2}. \tag{3}$$

Here, the passband center of the modulator is at $f_s/4$ (f_s is the sampling frequency of the modulator). Complex poles of the filter ($z = j$) can be implemented either with real integrators [4], or with a cascade of unit delay-cell architecture [13] (Fig. 2). In our modulator design, we choose the delay-cell architecture since it operates fast and has simple coefficient values. DWA logic circuits are used to realize our proposed complex DWA algorithm, which will be described in Sect. 4.
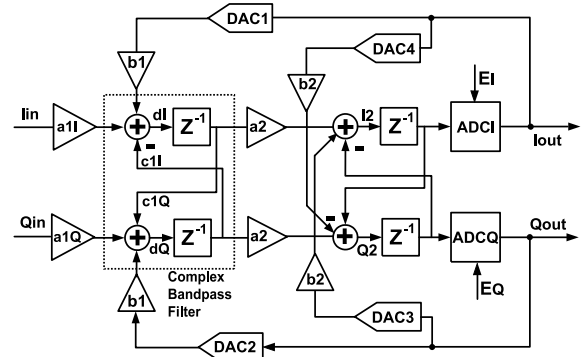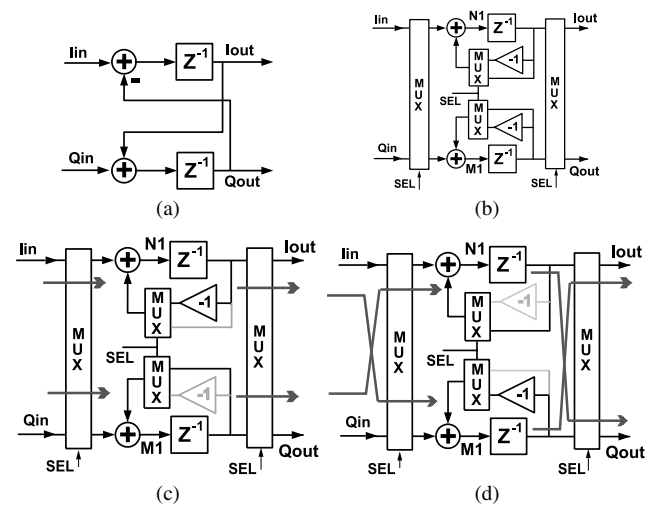
3. New Structure of Complex Bandpass Filter

Figure 2 shows a conventional structure of a second-order complex bandpass ΔΣAD modulator, which is composed of a second-order complex bandpass filter, two ADCs and four DACs. The modulator has I and Q signal crossing lines inside as shown in Fig. 2; it has not only signal crossings between the I and Q paths of the complex filter, but also signal crossings between the feedback paths through two DACs to the second stage of the complex filter in I and Q paths.

Figure 3(a) shows a basic complex bandpass filter in the modulator (Fig. 2) in the case of c1I = c1Q = 1, while Fig. 3(b) shows its proposed equivalent implementation, where four multiplexers (MUXs) are added and their select signal (SEL) toggles at half the rate of CLK in the z^{-1} block, after which they are synchronized. The proposed complex filter is divided into two separate parts without any crossing of signal lines.

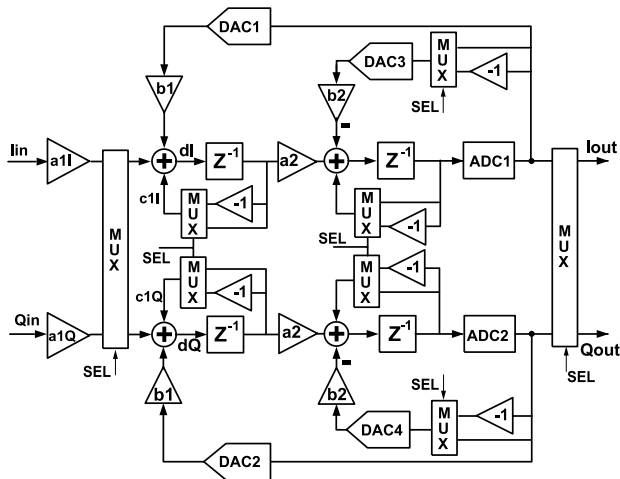The proposed complex filter operates with two states; in state 1 (in Fig. 3(c)), the upper part of the circuit is used

Fig. 4 Complex bandpass ΔΣAD modulator with proposed complex filter.

Table 1 Parameters for mismatches between I and Q paths.

a1I=$1 \times (1 - 0.03)$	a1Q=$1 \times (1 + 0.03)$
c1I=$3 \times (1 + 0.014)$	c1Q=$3 \times (1 - 0.03)$
dI=$1/3 \times (1 - 0.03)$	dQ=$1/3 \times (1 + 0.02)$

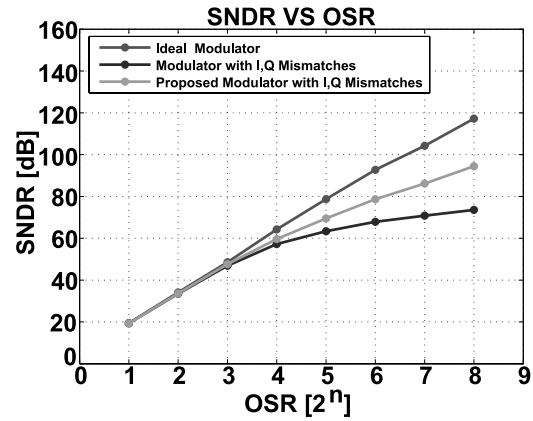**Fig. 5** Comparison of SNDRs of modulators with ideal DACs in three cases (parameters are those in Table 1).

for the I path, while the lower part is for the Q path. In state 2 (in Fig. 3(d)), the upper part of the circuit is used for the Q path, while the lower part is for the I path. In our proposed configuration, the input I and Q signals are alternated between the upper and lower parts of the complex filter by the SEL signal, so that it is equivalent to the conventional configuration when the circuits in both configurations are ideal with the same transfer function given by

$$H(z) = \frac{1}{z - j}. \tag{4}$$

Figure 4 shows the complex bandpass ΔΣAD modulator with two proposed complex filters. We have eliminated two MUXs from the back end of the first-stage filter and the front end of the second-stage filter, so that there are no signal crossing lines from DACs at the second-stage filter. We have also added MUXs to change the sign for inputs of DAC3 and DAC4 to keep the signal flow the same as that of the conventional modulator. As a result, only two MUXs are used to change the I and Q signals at the inputs and outputs of the modulator. The complex filter in the modulator can be divided into two separate parts without signal line crossing between the upper and lower paths, and its layout design can be simplified. Furthermore, the two sets of signal paths and circuits in the modulator are changed between I and Q when CLK is changed. Symmetric circuits are used for I and Q paths at a certain period of time, and they are switched by multiplexers to those used for Q and I paths at another period of time. Therefore, the effect of mismatches between I and Q paths is reduced by dynamic matching.

We have conducted MATLAB simulations to evaluate the effectiveness of the proposed architecture. Second-order complex bandpass modulators with internal ADCs/DACs of 9-level resolution (in Figs. 2 and 4) were used for the simulation with the following three cases:

1. An ideal modulator (in Figs. 2 or 4) without mismatches and nonlinearities.

2. A modulator in Fig. 2 with I and Q path mismatches whose parameters are shown in Table 1. Since the effect of mismatches in the second-stage filter is smaller, we form mismatches only for the first-stage filter in our simulation.

3. A modulator that employs the proposed architecture (in Fig. 4) and whose mismatches and nonlinearities are the same as those in case 2.

Figure 5 shows the simulation result comparison for the SNDRs of the modulators in these three cases. In case 1, the SNDR of the ADC increases as OSR increases. However, in case 2 (where mismatch parameters between I and Q paths are shown in Table 1), SNDR saturates as OSR increases. On the other hand, in case 3, SNDR improves because the mismatch effects are taken out of the signal band by dynamic matching.

4. Complex Bandpass DWA Algorithm

In ΔΣAD modulators, oversampling and noise shaping techniques are used to achieve high accuracy. When a single-bit modulator (i.e., internal ADC and DAC are 1-bit) is used to achieve a high SNDR, a higher OSR is needed, which demands a higher sampling rate, and/or a high-order filter inside a modulator (as well as a high-order digital filter following the ΔΣAD modulator) is required, which may cause modulator stability problems. On the other hand, when multibit ADCs/DACs are used inside the modulator, it can obtain a high SNDR with a low-order loop filter and improve the stability problem. Smaller steps of the quantizer result in a lower quantization error, and relax the required performance for opamps with a larger overload level.

A multibit DAC cannot be made perfectly linear, while a 1-bit DAC is inherently linear. Multibit DAC nonlinearity

is equivalent to errors added directly to the input signal - it is not reduced by noise shaping, and hence they may degrade the SNDR of the ΔΣADC. In our implementation, multibit ADCs/DACs are used. Each DAC in our modulator has a nine-level resolution with the segmented switched-capacitor architecture. Nonlinearities of the DAC due to mismatches of capacitors introduce errors in the feedback loop and appear directly at output; this results in an almost flat power spectrum in the entire band, and the SNDR of the modulator degrades.

We proposed a new noise shaping algorithm to reduce the effects of nonlinearities in multibit DACs of complex bandpass ΔΣAD modulators. Figure 6 shows our proposed architecture for complex bandpass noise shaping of DAC nonlinearities. It consists of a digital complex bandpass filter at the front end, two DACs, and an analog complex band elimination filter at the back end. The transfer function of the digital complex bandpass filter at the front end is the same as Eq. (4), whereas the transfer function of the analog complex band elimination filter at the back end is given by

$$H(z) = 1 - jz^{-1}. \tag{5}$$

Therefore, the nonlinearity errors of the two DACs $e1 + je2$ can be noise-shaped in a complex form at $f_s/4$, the notch of Eq. (5). In practice, however, this structure cannot be real-
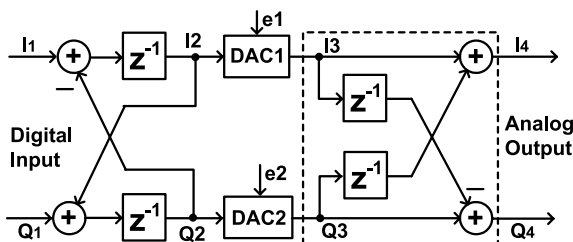
ized because the input signals may be infinite (out of DAC input range). Thus, the equivalent implementation called the complex DWA algorithm is proposed to realize the architecture of DACs shown in Fig. 6.

Our implementation uses only a digital filter at the front end of 2-channel DACs and does not require an analog filter at the back end. Element selection logic circuits (DWA1 and DWA2) are added between the two ADC outputs and DAC inputs to select the DAC unit elements in a rotational manner [7] as shown in Fig. 7. For the I-channel DAC output I_4, we apply a *highpass* DWA algorithm [11] with internal interaction between I and Q modulator outputs. For the Q-channel DAC output Q_4, we apply a *lowpass* DWA algorithm [12] with internal interaction between I and Q modulator outputs. DAC1 and DAC2 are used alternately for I and Q-channels; hence, mismatch effects between two DACs $e1 + je2$ are first-order complex bandpass noise-shaped at $f_s/4$. Our algorithm can be implemented using simple circuitry; analog and digital multiplexers, barrel shifters and adders/subtractors.

5. Circuit Implementation

Figure 8 shows the entire proposed complex bandpass ΔΣAD modulator. We see that the proposed second-order complex bandpass filter, which shares several MUXs, is used so that the proposed modulator has no crossing signal lines for either the forward paths of the z^{-1} block or the feedback paths from DACs. Hence, the proposed modulator can be completely divided into two separate parts and its layout design can be greatly simplified. Then its internal signal lines can be shorter, which leads to a smaller chip area.

For the proposed architecture, we note that MUXs can be easily realized using MOS switches. We add MUXs that alternate the polarity of the feedback signals between +1 and −1 at every sampling time to the feedback paths of filters and DACs. This maintains the polarity of internal complex

Fig. 6 Proposed architecture of DAC nonlinearity noise shaping for a complex bandpass modulator. I1 is the I-channel ADC output and Q1 is the Q-channel ADC output, while I4 is the I-channel DAC output and Q4 is the Qchannel DAC output. e1 and e2 denote the nonlinearities of DAC1 and DAC2, respectively. Note that this architecture cannot be implemented directly.
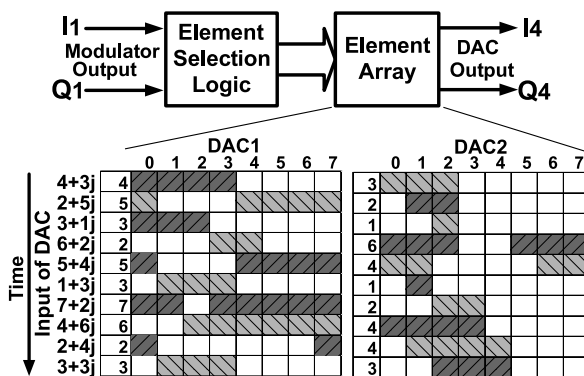

Fig. 7 Explanation of our complex bandpass DWA algorithm. The unit current cells in the ON state are filled in black for a real part (I-path) and in gray for an imaginary part (Q-path), when the complex input data are sequentially given by 4+3j, 2+5j, 3+j, 6+2j, ...

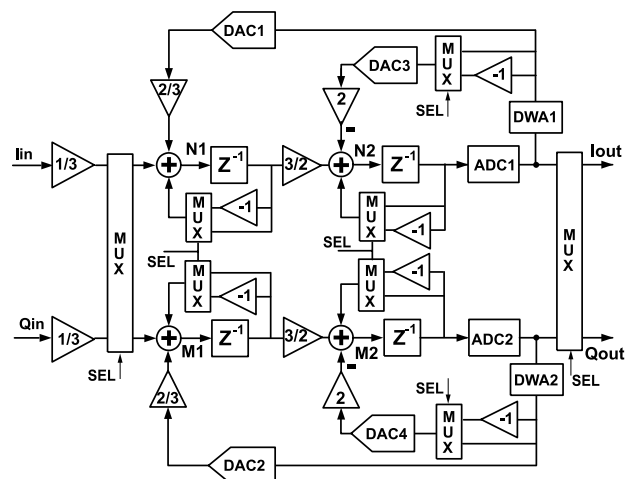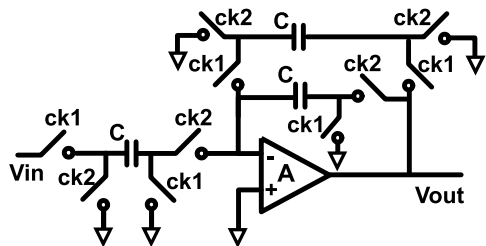**Fig. 8** Architecture of our complex bandpass ΔΣAD modulator.

Fig. 9 z^{-1} block realization using a switched-capacitor delay cell.

signals so that they are processed as a complex signal form [14]. In fact, we can realize this by simply chopping the two differential outputs at every sampling time.

The proposed modulator was designed with fully differential switched capacitor circuits. z^{-1} block realization using a switched-capacitor delay cell [13] is shown in Fig. 9 in its single-ended form, but the actual implementation is in its fully differential form in the modulator. Gate-boosted NMOS switches and dummy switches are used at the input sampling parts to cancel the effect of charge injection and clock feedthrough, while the rest of the elements are CMOS switches. $ck1$ and $ck2$ are nonoverlapping clocks to minimize the charge injection caused by sampling switches. Latched comparators with input offset storage are used in the flash-type nine-level ADCs, where offset cancellation is applied to both the preamplifier and the latch.

6. Experimental Results

The proposed complex bandpass ΔΣAD modulator was fabricated using 1P6M $0.18\,\mu$m CMOS technology without any option for precision capacitors and low threshold voltages. Figure 10 shows its chip microphotograph; the core size is $1.4 \times 1.3\,\text{mm}^2$. The capacitors were realized using multiple unit-capacitor cells for accurate ratio matching of coefficients. Unit-capacitor cells were realized using the MIM structure for high capacitance density in a small chip area.

Figure 11 shows a comparison of the output power spectrum results of the modulator for zero input between ON and OFF states of DWA logic. We see that while DWA logic is in the ON state, the noise floor at the band of interest is about 3 dB lower than that when DWA logic is in the OFF state; this validates the effectiveness of the proposed algorithm.

Figure 12 shows the measured output power spectrum for a 4.92 MHz sinusoidal input, where the sampling frequency of CLK was 20 MHz, and the reference voltages of the modulator were fixed at $V_{ref+} = 1.9$ V and $V_{ref-} = 0.9$ V. The degree of the mirror image signal suppression in the modulator was evaluated by demodulating the complex IF signal down to the baseband with quadrature carriers in the digital domain and performing an FFT on the resulting complex-valued signal. The spectrum of the demodulated, complex-valued baseband signal is shown in Fig. 13 which just shifts the center of the signal band from fs/4 to DC in the frequency domain; the scale of the frequency axis is ex-
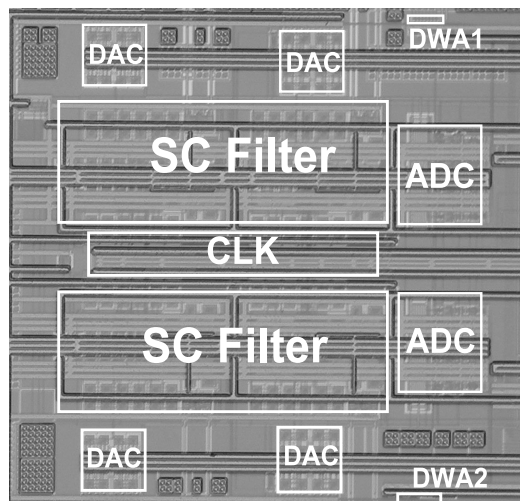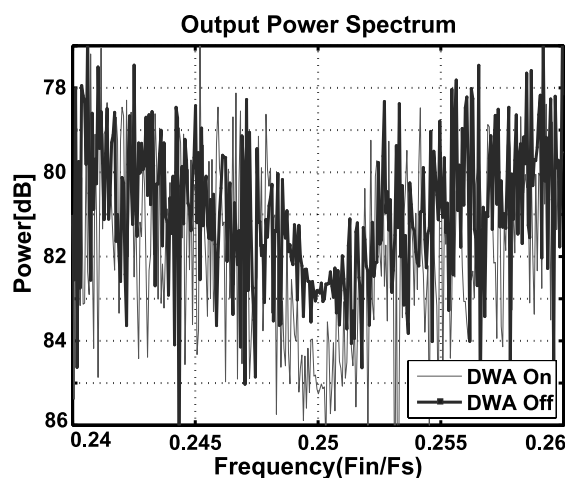

Fig. 10 Chip photopragh.

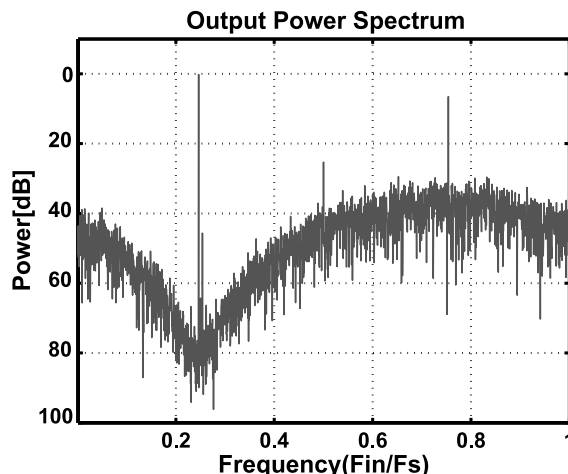**Fig. 11** Comparison of power spectrum bwtween DWA on and off.

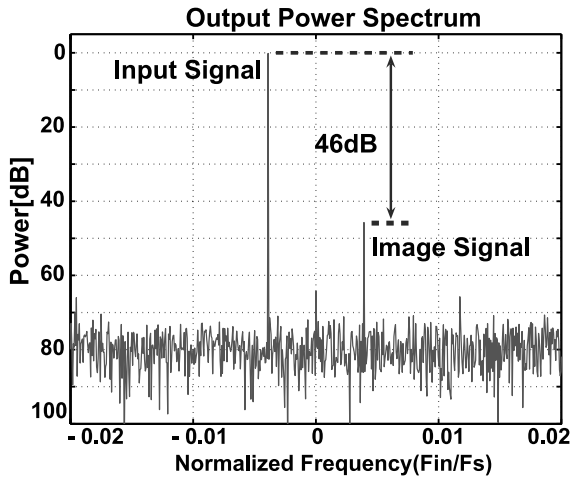**Fig. 12** Measured output power spectrum of the proposed modulator.

Output Power Spectrum

Fig. 13   Measured output power spectrum of the proposed modulator.
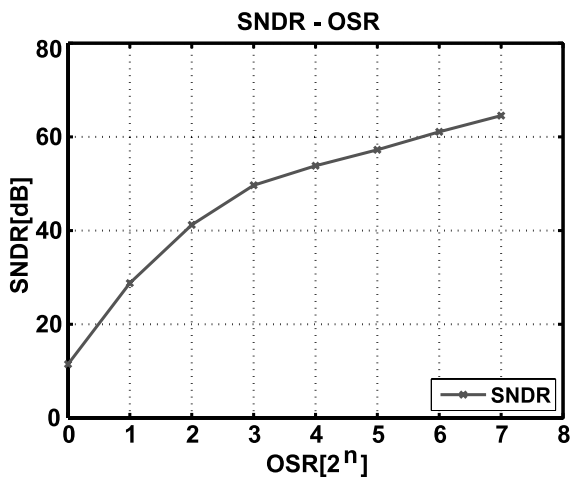
SNDR - OSR

Fig. 14   Measured SNDR vs. OSR of the proposed modulator.

panded around DC and the value of the power spectrum is the same as that in Fig. 12. It is observed that the image signal is suppressed by 46 dB with respect to the desired signal. Figure 14 shows SNDR vs. OSR; the peak SNDR is 64.5 dB. Clocked at 20 MHz, the modulator consumes 28.4 mW at a power supply voltage of 2.8 V.

7. Conclusion

We have designed, fabricated and tested a second-order multibit switched-capacitor complex bandpass $\Delta\Sigma$AD modulator to demonstrate the effectiveness of two new algorithms:

1. A complex bandpass filter with I, Q dynamic matching to reduce the effect of mismatch between I and Q paths. The complex filter in the modulator can be divided into two separate parts without requiring sensitive signal lines of the upper and lower paths to cross.
2. A new complex bandpass DWA algorithm is implemented to suppress nonlinearity effects of multibit

DACs in complex form.

The effectiveness of the proposed architecture and circuit technique has been demonstrated by measured results.

References

[1] J. Crols and M. Steyeart, "Low-IF topologies for high-performance analog front ends of fully integrated receivers," IEEE Trans. Circuits Syst. II, vol.45, no.3, pp.269–282, March 1998.

[2] L. Breems, R. Rutten, R. Veldhoven, G. Weide, and H. Termeer "A 56 mW CT quadrature cascaded $\Sigma\Delta$ modulator with 77 dB DR in a near zero-IF 20 MHz band," ISSCC Digest of Technical Papers, pp.238–239, Feb. 2007.

[3] N. Yaghini and D. Johns, "A 43 mW CT complex $\Delta\Sigma$ ADC with 23 MHz of signal bandwidth and 68.8 dB SNDR," ISSCC Digest of Technical Papers, pp.502–503, Feb. 2005.

[4] S.A. Jantzi, K.W. Martin, and A.S. Sedra, "Quadrature bandpass $\Sigma\Delta$ modulator for digital radio," IEEE J. Solid-State Circuits, vol.32, no.12, pp.1935–1949, Dec. 1997.

[5] H. San, Y. Jingu, H. Wada, H. Hagiwara, A. Hayasaka, J. Kudoh, K. Yahagi, T. Matsuura, H. Nakane, H. Kobayashi, M. Hotta, T. Tsukada, K. Mashiko, and A. Wada, "A multibit complex bandpass $\Delta\Sigma$AD modulator with I, Q dynamic matching and DWA algorithm," 2006 Asian Solid-State Circuits Conference (A-SSCC 2006), pp.55–58, Hangzhou, China, Nov. 2006.

[6] H. San, H. Kobayashi, S. Kawakami, N. Kuroiwa, and H. Wada, "An element rotation algorithm for multibit DAC nonlinearities in complex bandpass $\Delta\Sigma$AD modulators," IEEE 17th International Conference on VLSI Design, pp.151–156, Mumbai, India, Jan. 2004.

[7] H. San, H. Kobayashi, S. Kawakami, and N. Kuroiwa, "A noise-shaping algorithm of multi-bit DAC nonlinearities in complex bandpass $\Delta\Sigma$AD modulators," IEICE Trans. Fundamentals, vol.E87-A, no.4, pp.792–800, April 2004.

[8] H. San, A. Hayasaka, Y. Jingu, H. Wada, H. Hagiwara, K. Kobayashi, H. Kobayashi, T. Matsuura, K. Yahagi, J. Kudoh, H. Nakane, M. Hotta, T. Tsukada, K. Mashiko, and A. Wada, "Complex bandpass $\Delta\Sigma$AD modulator architecture with dynamic matching of I,Q paths," 2005 IEEJ International Analog VLSI Workshop, Bordeaux, France, Oct. 2005.

[9] H. San, A. Hayakawa, Y. Jingu, H. Wada, H. Hagiwara, K. Kobayashi, H. Kobayashi, T. Matasuura, K. Yahagi, J. Kudoh, H. Nakane, M. Hotta, T. Tsukada, K. Mashiko, and A. Wada, "Complex bandpass $\Delta\Sigma$AD modulator architecture without I, Q-path crossing layout," IEICE Trans. Fundamentals, vol.E89-A, no.4, pp.908–915, April 2006.

[10] J. Grilo, I. Galton, K Wang, and R. Montemayor "A 12-mW ADC Delta-Sigma modulator with 80 dB of dynamic range integrated in a single-chip Bluetooth transceiver," IEEE J. Solid-State Circuits, vol.37, no.3, pp.271–278, March 2002.

[11] T. Shui, R. Screier, and F. Hudson, "Mismatch shaping for a current-mode multibit delta-sigma DAC," IEEE J. Solid-State Circuits, vol.34, no.3, pp.331–338, March 1999.

[12] R.T. Baird and T.S. Fiez, "Linearity enhancement of multibit $\Delta\Sigma$ A/D and D/A converters using data weighted averaging," IEEE Trans. Circuits Syst. II, vol.42, no.12, pp.753–762, Dec. 1995.

[13] L. Longo and B. Horng, "A 15b 30 kHz bandpass sigma-delta modulator," ISSCC Digest of Technical Papers, pp.226–227, Feb. 1993.

[14] K.W. Martin, "Complex signal processing is not complex," IEEE Trans. Circuits Syst. I, vol.51, pp.1823–1836, Sept. 2004.

Hao San received the B.S. degree in automation engineering from Liaoning Institute of Technology, China in 1993, and the M.S. and Dr. Eng. degrees in electronic engineering from Gunma University, Japan in 2000 and 2004, respectively. From 2000 to 2002, he worked for Kawasaki Microelectronics Inc. In 2004 he joined Gunma University and currently he is an assistant professor in Electronic Engineering Department there. He has been engaged in research of analog and mixed-signal integrated circuits. He is a member of the IEEE.

Yoshitaka Jingu received the B.S. and M.S. degrees in electrical engineering from Gunma University in 2004 and 2006, respectively. In 2006, he joined Renesas Technology Corp., where he is engaged in analog integrated circuit design.

Hiroki Wada received the B.S. and M.S. degrees in electrical engineering from Gunma University in 2004 and 2006, respectively. In 2006, he joined SANYO Electric Co., Ltd. His research interests include analog circuits.

Hiroyuki Hagiwara was born in Gunma, Japan on Oct. 5, 1981, and received the B.S. and M.S. degrees in electrical engineering from Gunma University in 2004 and 2006, respectively. In 2006, he joined CMK Corporation. His research interests include analog circuits.

Akira Hayakawa received the B.S. and M.S. degrees in electrical engineering from Gunma University in 2004 and 2006, respectively. In 2006, he joined Mitsuba Corporation. His research interests include analog circuits.

Haruo Kobayashi received the B.S. and M.S. degrees in information physics from University of Tokyo in 1980 and 1982 respectively, the M.S. degree in electrical engineering from University of California at Los Angeles (UCLA) in 1989, and the Dr.Eng. degree in electrical engineering from Waseda University in 1995. He joined Yokogawa Electric Corp. Tokyo, Japan in 1982, where he was engaged in the research and development related to measuring instruments and mini-supercomputers. From 1994 to 1997, he was involved in research and development of ultra-high-speed ADCs/DACs at Teratec Corp. In 1997 he joined Gunma University and presently is a Professor in Electronic Engineering Department there. He was also an adjunct lecturer at Waseda University from 1994 to 1997. His research interests include analog & digital integrated circuits design and signal processing algorithms. He received Yokoyama Award in Science and Technology in 2003, and the Best Paper Award from the Japanese Neural Network Society in 1994.

Tatsuji Matsuura received the B.E. and M.E. degrees in mathematical engineering and instrumentation physics from the University of Tokyo, Tokyo, Japan, in 1976 and 1978 respectively. He joined the Central Research Lab. Hitachi, Ltd., in 1978 where he has been engaged in the research and development of picture-processing LSIs and high-speed A/D and D/A converters. Since 1995, he has been with the Semiconductor & Integrated Circuit Group, Hitachi, Ltd. Since 2003, he is in Renesas Technology, where he is a senior chief engineer. He is a member of the IEEE. He served as a technical program committee member of CICC (Custom Integrated Circuit Conference) for analog sub-committee since 1996 to 2003. Since 2005, he serves as a technical program committee member of ISSCC(International Solid-State Circuit Conference).

Kouichi Yahagi received the B.E. degree in electronic engineering from Tokyo University of Agriculture and Technology, Tokyo, Japan in 1988. Since he joined Hitachi, Ltd. in 1988, he has involved in the development of various analog and analog-digital mixed ICs. Currently he is in Renesas Technology Corp. where he leads a RF transceiver design team for wireless communications.

Junya Kudoh received the B.E. degree in electrical engineering from Waseda University, Tokyo Japan in 1991. He joined Device Development Center of Hitachi, Ltd. in 1991. Currently he is in Advanced Analog Development Div. of Renesas Technology Corp. and engaged in development of analog circuits. His interests include the design of analog-to-digital conversion circuits and architectures.

Hideo Nakane received the B.E. and M.E. degrees in Electrical Engineering and Computer Science, Kumamoto University, Kumamoto, Japan in 1997 and 1999, respectively. And he received D.Eng. in Graduate School of Science and Technology, Kumamoto University in 2002. He joined Semiconductor & Integrated Circuit Group, Hitachi, Ltd. in 2002. Since 2003, he is in Renesas Technology Corp., and engaged in A/D converter design for radio communications. He is a member of the IEEE and IEE of Japan.

Masao Hotta received the Ph.D. degree in electronics from Hokkaido University, Sapporo, Japan, in 1976. In 1976 he was with the central research laboratory, Hitachi Ltd., Tokyo, Japan. He engaged in research and development of high-precision D/A converters, ultra-high-speed D/A converters and high-speed A/D converters. From 1996 to 2003, he was a manager of advanced device development department and also a senior chief engineer & senior manager of advanced analog technology center, semiconductor & integrated circuits division of Hitachi Ltd. He has worked on the development of mixed-signal LSIs, RF devices, and DA/CAD systems. From 2003 to 2005, he was a general manager of advanced analog technology division, Renesas Technology Corp. He conducted development on RF power amplifier modules, RF transceiver LSIs, mixed-signal LSIs and advanced analog cores for SoC. Since 2005, he has been a Professor at Musashi Institute of Technology, Tokyo, Japan, working on high performance ADCs, mixed-signal LSI design and wireless systems. Dr. Hotta has served as a chair of IEEE Circuits and Systems Society Japan Chapter, technical program committee members of CICC, BCTM and ASIC/SOC Conference and a chair of Technical Committee on Circuits and Systems, IEICE. He is a fellow of IEEE.

Toshiro Tsukada received the B.E., M.E. and D.Eng. degrees in electrical engineering from the University of Tokyo, in 1971, 1973, and 1995 respectively. Since joining the Central Research Laboratory, Hitachi, Ltd. in 1973, he has been involved in the research and development of MOS analog and mixed-signal integrated circuits. From 1980 to 1981 he worked on MOS analog circuits as a research associate in the Electronics Research Laboratory, University of California, Berkeley, and worked on integrated communication circuits at the Telecommunications Division of Hitachi (1988–1993). Since 1995, he has been in Semiconductor & Integrated Circuits of Hitachi and in the Advanced Analog Development Department, Renesas Technology Corporation. He is currently working as a senior manager in the Low Power Technology Group of Semiconductor Technology Academic Research Center (STARC), Yokohama.

Koichiro Mashiko received the B.S. and M.S. degrees in physics from the University of Tokyo, Tokyo, Japan, in 1975 and 1977, respectively. He received the Ph.D. degree in electrical engineering from Osaka University, Osaka, Japan, in 1988. He joined the LSI Laboratory, Mitsubishi Electric Corporation, Itami, Hyogo, Japan, in 1977, where he was engaged in the R&D of DRAM's from 64 kbit to 4 Mbit, 256 kbit dual-port video RAM, and so on. From 1990 to 1993, he was with Mitsubishi Electric Research Laboratories, Inc. or MERL, Cambridge, MA. U.S.A., where he was engaged in the establishment of the new laboratory and collaboration with U.S. universities. In 1993, he transferred to the System LSI Laboratory, Mitsubishi Electric Corporation, Itami, Japan, where he was engaged in the R&D of high-speed logic circuits and low-voltage/low-power circuit and device technologies. In 2002, he joined STARC (Semiconductor Technology Academic Research Center), Yokohama, Japan, where he has been promoting the collaboration between universities and industry in SoC design area with focus on mixed-signal and heterogeneous integration. He was Guest Professor at the University of Tokyo, VLSI Design and Education Center, or VDEC from 2003–2005. He is a member of IEEE. He served as a Technical Program Committee member for IEEE VLSI Circuit Symposium from 1994 to 1997 and for IEEE CICC from 1998 to 2001. He also served as Chair and Vice Chair of Analog and RF Subcommittee for ASP-DAC2004 and 2005, respectively. He is now a member of TPC of A-SSCC and VLSI-DAT.

Atsushi Wada received the B.S. degree in physics from Kyoto University, Kyoto, Japan, in 1987. In 1987, he joined R&D headquarters, SANYO Electric Co., Ltd., Osaka, Japan. Since then, he has been engaged in research and development of CMOS analog circuits and mixed signal systems such as dynamic-RAM's, low-power pipelined A/D converters, analog front-end LSIs and image sensing systems. He is currently conducting development on RF/Mixed signal circuits and low power LSI's as a senior manager of Mixed Signal Department in Devices Development Center, SANYO Electric Co., Ltd., Gifu, Japan. He is a member of IEEE. He served as a member of Technical Program Committee for IEEE VLSI Circuit Symposium from 1998 to 2002.