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Novel Architecture of Feedforward Second-Order Multibit ΔΣAD Modulator

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SUMMARY This paper proposes novel feedforward architecture of the second-order multibit ΔΣAD modulator with single DAC-feedback topology. The ΔΣAD modulator realizes high resolution by oversampling and noise shaping techniques. However, its SNDR (Signal to Noise and Distortion Ratio) is limited by the dynamic range of the input signal and non-idealities of circuit building blocks, particularly by the harmonic distortion in amplifier circuits. A full feedforward ΔΣAD modulator structure has the signal transfer function of unity under ideal circumstances, which means that the signal swings through the loop filter become smaller compared with a feedbacked ΔΣAD modulator. Therefore, the harmonic distortion generated inside the loop filter can be significantly reduced in the feedforward structure because the effect of non-idealities in amplifiers can be suppressed when signal swing is small. Moreover, the reduction of the internal signal swings also relaxes output swing requirements for amplifiers with low supply voltage. However, in conventional feedforward ΔΣAD modulator, an analog adder is needed before quantizer, and especially in a multibit modulator, an additional amplifier is necessary to realize the summation of feedforward signals, which leads to extra chip area and power dissipation. In this paper, we propose a novel architecture of a feedforward ΔΣAD modulator which realizes the summation of feedforward signals without additional amplifier. The proposed architecture is functionally equivalent to the conventional one but with smaller chip area and lower power dissipation. We conducted MATLAB and SPICE simulations to validate the proposed architecture and modulator circuits.

key words: *ΔΣAD modulator, switched-capacitor, feedforward, multibit*

1. Introduction

As an interface between the analog world and the digital domain, the Analog-to-Digital Converter (ADC) is widely used in mixed-signal circuits. However, in nano-meter CMOS technology, the device characteristics degradation (such as matching and drain resistance r_{ds}) and the low supply voltage evidently reduce the accuracy of ADC. ΔΣAD modulators realize high resolution by oversampling and noise shaping techniques, which are suitable for high resolution application in the nano-meter CMOS technology. The performance of ΔΣAD modulators is limited by dynamic range of input signal and non-idealities of circuit building blocks. In nano-meter CMOS technology, the performance of analog circuits is significantly degraded and non-idealities of circuit building blocks, especially non-linearities of amplifiers generate more harmonic distortion. Furthermore, since signal swings are reduced due to lower supply voltage, the dynamic range will be decreased and the performance of the modulator would be degraded. Circuit level challenge for high resolution with low-voltage operation is limited in the nano-meter CMOS technology. The best solution for the problems would be at system level.

In this paper we propose novel feedforward architecture of the ΔΣAD modulator which would be suitable with nano-meter CMOS technology implementation. Section 2 describes feedforward and feedback modulator architectures. Section 3 explains the proposed architecture and Sect. 4 shows its simulation results. Section 5 describes conclusion.

2. Feedback & Feedforward ΔΣAD Modulators

This section describes second-order feedback (Fig. 1) and feedforward (Fig. 2) ΔΣAD modulators. They have similar structure with two integrators, one ADC and one or two DACs, but their signal paths are different.

2.1 Feedback ΔΣAD Modulator

The feedback structure shown in Fig. 1 is a commonly used in a ΔΣAD modulator, and its input and output can be expressed as

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^2 E(z). \quad (1)$$

Here $X(z)$ is the input signal, $Y(z)$ is the output signal and $E(z)$ is the quantization noise of the modulator. Then the signal transfer function (STF) and noise transfer function (NTF) are given by

$$STF(z) = z^{-2} \quad (2)$$

$$NTF(z) = (1 - z^{-1})^2. \quad (3)$$

NTF provides a second-order noise-shaping function for the

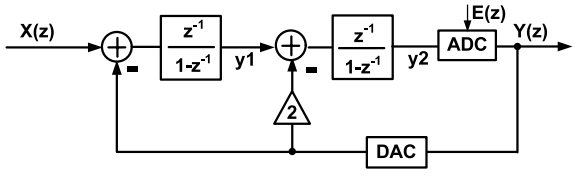

Fig. 1 Second-order feedback ΔΣAD modulator.

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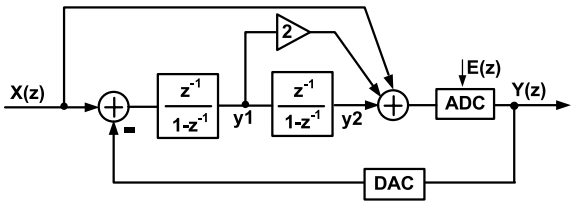

Fig. 2 Conventional second-order feedforward ΔΣAD modulator.

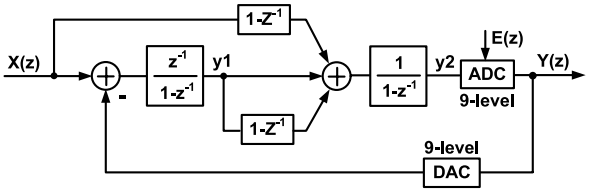

Fig. 3 Proposed second-order feedforward ΔΣAD modulator.

quantization noise $E(z)$. The output signals of the first and second integrators (y_1 and y_2) are given as follows:

$$y_1 = z^{-1}(1+z^{-1})X(z) - z^{-1}(1-z^{-1})E(z) \quad (4)$$

$$y_2 = z^{-2}X(z) - z^{-1}(2-z^{-1})E(z). \quad (5)$$

From Eqs. (4) and (5), we see that the output signals of two integrators (y_1 and y_2) are the functions of the input signal ($X(z)$). Then the signal swings at the amplifier outputs become large which makes their implementation with the low supply voltage difficult. The harmonics generated by the amplifier non-linearities also depends on the signal swing of integrator, which would reduce SNDR of the modulator with feedback topology.

2.2 Feedforward ΔΣAD Modulator

The input and output of the feedforward ΔΣAD modulator (Fig. 2) can be expressed as

$$Y(z) = X(z) + (1-z^{-1})^2 E(z) \quad (6)$$

$$STF(z) = 1 \quad (7)$$

$$NTF(z) = (1-z^{-1})^2. \quad (8)$$

Compared with feedbacked ΔΣAD modulator (Fig. 1), NTF given by Eq. (8) is the same as Eq. (3). However note that STF is unity and not delayed under ideal circumstances. The output signals of the first and second integrators (y_1 and y_2) are given as follows:

$$y_1 = -z^{-1}(1-z^{-1})E(z) \quad (9)$$

$$y_2 = -z^{-2}E(z). \quad (10)$$

From Eqs. (9) and (10), we can see that the output signals of two integrators (y_1 and y_2) are free of the input signal $X(z)$, which means that the first and second integrators of the feedforward ΔΣAD modulator process quantization error only [1], [2]. Therefore, the signal swings passing through the integrators are smaller and the distortion generated by the amplifiers would be input-signal-independent and reduced. Furthermore, in this topology, the signal amplitudes of the amplifiers are reduced, which eases implementation of amplifier design with low power supply.

3. Proposed Novel Architecture of Feedforward ΔΣAD Modulator

Note the summation point of feedforward paths in front of the quantizer in Fig. 2, a signal addition circuit is necessary to realize all the feedforward signals summed together; this creates complexity for full feedforward ΔΣAD modulators. In some implementations [3], [4], this adder is realized by passive switched-capacitor network. However, this approach reduces the signal level into the quantizer and is only suitable for single-bit implementation. In a multibit implementation of the full feedforward ΔΣAD modulators, the switched-capacitor adder has to be used and a weighted summation amplifier is required before the quantizer [5], that leads to extra chip area and power dissipation. Some ideas have been proposed to solve this problem in [6], [7]. However, they require a distributed DAC-feedback [6] or a high-order (≥3rd-order) loop filter [6], [7] which would increase complexity of modulator circuits.

We propose here a novel architecture of feedforward ΔΣAD modulators [8]. It is a single DAC-feedback, second-order ΔΣAD modulator without an additional amplifier and its circuit implementation with low supply voltage would be simple. Figure 3 shows the proposed architecture of the feedforward ΔΣAD modulator in 3-bit ADC and DAC case, and it has the following features:

- **One-amplifier saving**
  In our proposed novel architecture, we moved the summation point of feedforward path from input node of the quantizer to the input node of the second-stage loop filter. (See the conventional feedforward modulator (Fig. 2) for comparison.) The feedforward signals are merged into the output of the first-stage integrator, and then are fed to the second stage. By this way, the amplifier in the second stage can be shared to realize signal summation and integration. As such, circuit complexity is reduced by not requiring an additional weighted summation amplifier before the quantizer. In the modulator implementation of [5], the summation amplifier in front of the quantizer consumes 8% of total power, and we estimate that this amount of power reduction would be possible in the modulator topology of [5] with our proposed amplifier-saving technique.
- **Lower-order loop filter and multibit architecture**
  Higher SNDR can be realized by a higher-order modulator which, however, needs more hardware and consumes more power. A second-order loop filter can be implemented simply rather than a high-order one, which reduces analog circuit complexity and power dissipation. Multibit quantizer not only reduces quantization noise, but also relaxes the required slew rate

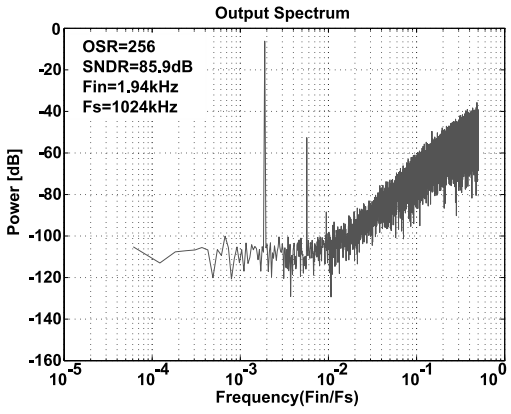

Fig. 4 Simulated output power spectrum of the second-order feedback ΔΣAD modulator in Fig. 1 with harmonic distortions.

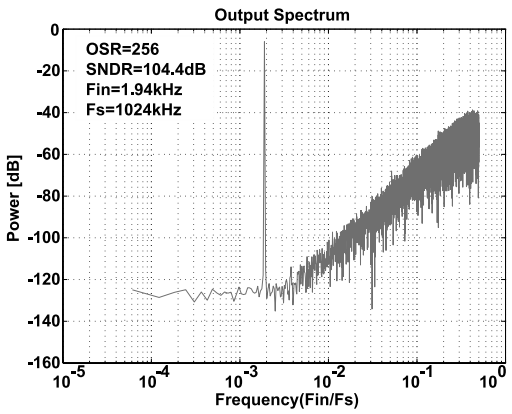

Fig. 5 Simulated output power spectrum of the conventional second-order feedforward ΔΣAD modulator in Fig. 2 with harmonic distortions.

of input amplifier of the filter. Therefore, the modulator becomes more linear, its stability is improved and power dissipation is lower [9].

- **Single DAC-feedback and single-loop topology** Furthermore, with a single DAC-feedback and a single-loop topology, (rather than a distributed DAC-feedback [10] or a cascaded architecture [11]), requirements for analog circuit and DAC linearization in the ΔΣ modulator are reduced, because the modulator circuits can be much insensitive to the finite dc gains of the amplifiers. Normally DAC circuits are realized by switched-capacitor circuits, and simple DAC implementation can reduce the power dissipation for charge and discharge of capacitors, which are more suitable for low-power dissipation.

The input and output transfer functions (STF, NTF) of the proposed modulator are the same as Eqs. (6), (7) and (8). The output signals of the first and second integrators in proposed modulator, (y_1, y_2) are as follows:

$$y_1 = -z^{-1}(1 - z^{-1})E(z) \tag{11}$$

$$y_2 = X(z) - z^{-1}(1 - z^{-1})E(z). \tag{12}$$

From Eqs. (11) and (12), we see that the output signal of the first integrator y_1 is free of the input signal, but the output signal of the second integrator y_2 contains a input signal component. However, non-idealities of the second integrator can be noise-shaped by the feedback loop in the modulator, and their effects are not dominant for second order modulator [12]. It should also be noted that the $(1 - z^{-1})$ term in the feedforward path of the proposed modulator can be implemented just by a simple capacitor.

We have made the performance comparison of feedback ΔΣAD modulator with our proposed ΔΣAD modulator, including a finite gain amplifier model and a nonlinear amplifier model with harmonic distortion. We assumed that all amplifiers in the modulators have DC gain of 40 dB and third-order distortion corresponding to 1% for a full scale signal.

Figure 4 shows the output spectrum of a feedback ΔΣAD modulator in Fig. 1 including a finite gain and a nonlinear amplifier model. We observe that the gain nonlinearities of amplifiers cause large harmonic distortion and it appears at the output of the feedback ΔΣAD modulator. When this modulator samples a sinusoidal input signal of $F_{in} = 1.94$ kHz at $F_s = 1024$ kHz sampling rate, its SNDR reaches 85.9 dB in case of $OSR = 256$.

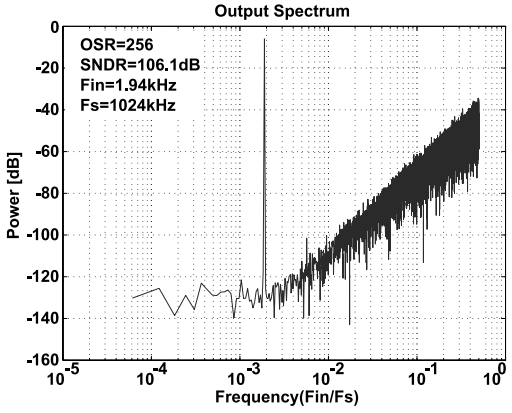

Fig. 6 Simulated output power spectrum of the proposed second-order feedforward ΔΣAD modulator in Fig. 3 with harmonic distortions.

Figure 5 shows the output spectrum of the conventional feedforward ΔΣAD modulator (Fig. 2) and Fig. 6 shows the output spectrum of the feedforward ΔΣAD modulator (Fig. 3), both of which include a finite gain and nonlinear amplifier models that are the same as feedback modulator ones. The same nonlinear gain coefficients are used as the case of Fig. 4, but it is clear that in feedforward modulator, the harmonic distortion is greatly suppressed. Our proposed feedforward modulator has harmonic suppression effect which is the same as the conventional one. SNDR can reach $SNDR = 106.1$ dB in the case of $OSR = 256$ with the same input signal frequency and sampling rate.

From the above discussion we can see that the proposed modulator can realize equivalent noise shaping function to the conventional one and is more insensitive to non-idealities of amplifier.

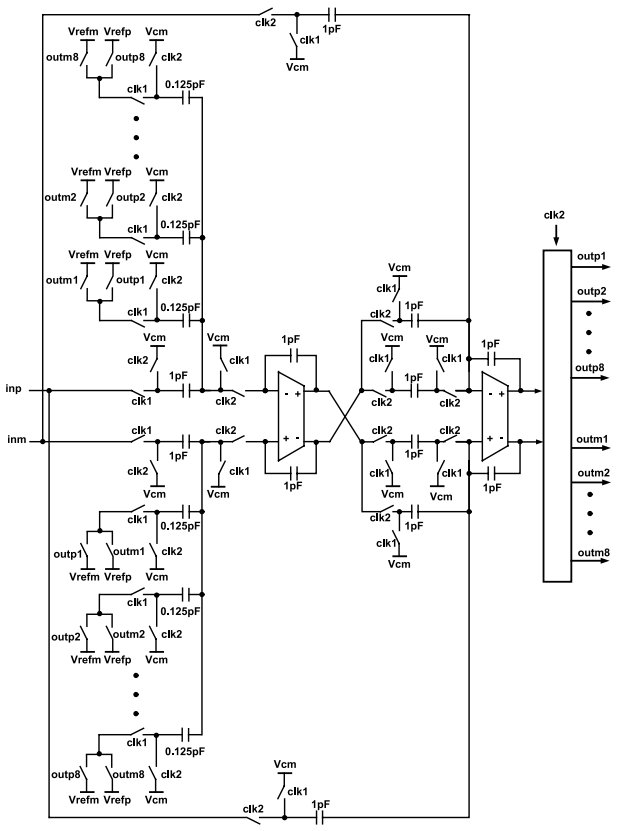

Fig. 7 Switched-capacitor implementation of the proposed feedforward ΔΣAD modulator.

Figure 7 shows the fully differential switched-capacitor circuit implementation of the proposed feedforward ΔΣAD modulator with loop filters and feedback DACs. Parasitic-insensitive switched-capacitors structures are used for integrators [13]. Negative capacitors in the modulator are easily implemented by changing the polarity of input signals in the fully differential circuit. Feedforward signals are summed at input node of the second stage integrator, and no more additional summation amplifier is necessary. The coefficients in Fig. 3 are realized by the ratios of capacitors around the amplifiers. In our proposed modulator, all coefficients are 1 which is easily implemented with the same capacitor size. Nine-level DAC are designed by 8 capacitors whose unit size is 1/8 of the input sampling capacitor. Therefore, the size of all capacitors can match well.

4. Simulation Results

We have conducted MATLAB and SPICE simulations to validate the proposed architecture and the modulator circuits. Matlab behavioral model is shown in Fig. 3 and SPICE behavioral circuit is shown in Fig. 7.

In SPICE simulation, ideal amplifiers and switches are used, and the values of capacitors are shown in Fig. 7. We assume that supply voltage is $V_{dd} = 1.8\,\mathrm{V}$, reference voltages are $V_{refp} = 1.8\,\mathrm{V}$, $V_{cm} = 0.9\,\mathrm{V}$ and $V_{refm} = 0\,\mathrm{V}$, input signals are differential sine waves with $V_{pp} = 1.0\,\mathrm{V}$ and common mode voltage of 0.9 V. Figure 8 shows SPICE simulation results of two integrators output waveforms; the output voltages of both integrators are within a range of 0 to V_{dd} (which means that the two amplifiers work well without saturation). We can see that the output voltage swing of the

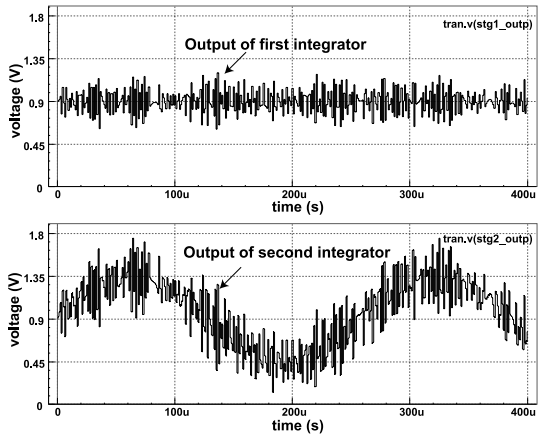

Fig. 8 SPICE simulation results of two-integrator outputs in the proposed ΔΣAD modulator.

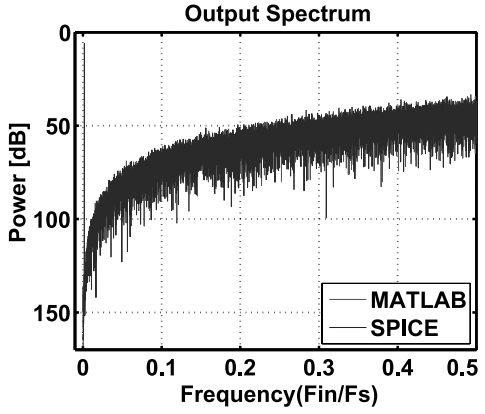

Fig. 9 MATLAB and SPICE simulated output power spectrum comparison of the proposed multibit ΔΣAD modulator.

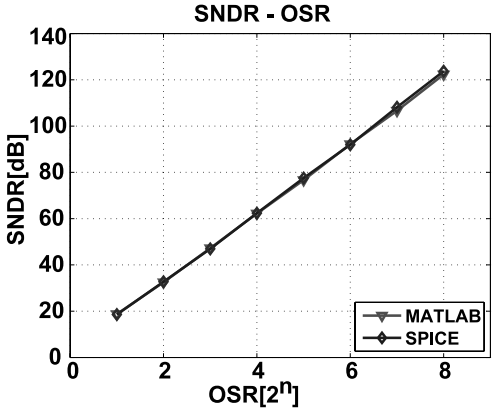

Fig. 10 MATLAB and SPICE simulated SNDR-OSR comparison of the proposed multibit ΔΣAD modulator.

first integrator is very small; it eventually reduces the power consumption and eases the amplifier design with low supply voltage. We have also compared the MATLAB and SPICE simulation results. Figure 9 shows the output spectrum simulation result comparison, and Fig. 10 shows SNDR-OSR result comparison. We can see that the SPICE behavioral simulation results are similar to MATLAB simulated results, and hence the proposed circuit realizes the noise shaping as well as at system level.

5. Conclusion

We have proposed novel feedforward architecture of the second-order ΔΣAD modulator and its implementation circuits. In the proposed architecture, one amplifier is shared between the signal adder and the second-integrator so that the circuit complexity, chip area and power dissipation would be reduced. MATLAB and SPICE simulations results validate the effectiveness of the proposed architecture and modulator circuits.

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