A Time-to-Digital Converter with Small Circuitry

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I. Introduction

A Time-to-Digital-Converter (TDC) is to measure the interval time between two signals, and its time resolution of several pico seconds is achieved when it is implemented with advanced CMOS process [1-5]. Its applications are gradually expanding such as a phase comparator of all-digital-PLL, a sensor interface circuit, modulation circuit and demodulation circuit as well as a TDC-based ADC [1-6]. The TDC will play more important role in nano-CMOS era because it is well-matched to implement with fine digital CMOS process; it consists of mostly digital circuits, and as the switching speed increases, its performance is improved.

This paper reports on a new TDC architecture with small circuitry (hence low power and low cost), fine time resolution and high linearity.

II. Conventional TDC Architecture

Basic TDC : Fig.1(a) shows configuration of a basic TDC, where the reference CLK passes through a buffer line which consists of an inverter chain, and the delayed reference CLK signals are fed into Flip-Flops as their data input. Also the measured signal is fed into Flip-Flops as their clock signal. We obtain the outputs of the Flip-Flops as a thermometer code, according to the rise-edge-timing interval between the reference CLK and the measured signal, and the encoder transforms it into a binary code. Its time resolution is given as the gate delay τ.

Vernier Delay Line TDC : Fig.1(b) shows a vernier delay line TDC which uses two delay lines: one is for the reference CLK with the buffer delay of τ_1. and the other is for the measured signal with the buffer delay of τ_2. Its time resolution is given by $\tau_1 - \tau_2$ (gate delay difference) which can be smaller than the basic TDC, but note that it uses 2N buffers (N buffers of τ_1 and N buffers of τ_2) for the input range from 0 to N $(\tau_1 - \tau_2)$.

III. Proposed TDC Architecture

Fig.2 shows the proposed TDC which consists of two kind of buffers with their delays of τ_1, τ_2. Its time resolution is given by $\tau_1 - \tau_2$ which is the same as the vernier delay line TDC in Fig.1(b), but the number of the total buffers is N which is half of the vernier delay line TDC.

Fig.3 shows an example of the proposed TDC with τ_1=30ps, τ_2=20ps and time resolution of 10ps $(= \tau_1 - \tau_2)$; Figs.3(a), (b) and (c) show the path when the reference CLK is delayed by 20ps, 30ps, and 40ps respectively. These delayed signals from the reference CLK are fed into Flip-Flops (or latched comparators) as data inputs, and the measured signal is fed into all Flip-Flops (or latched comparators) as clock inputs.

Note that Nose et. al. proposed the similar TDC as a hierarchical structure TDC [4], but its time resolution is τ_2 which is the gate delay itself and depends on CMOS process. Since the time resolution of our proposed TDC is the difference of the two gate delays $(\tau_1 - \tau_2)$, it can be finer than the gate delay itself τ_2.

IV. Linearity Consideration for the Proposed TDC

The average delay value among, for example, τ_1 buffers can be adjusted by the DLL system. However there can be relative delay mismatches among τ_1 buffers; the delay of one buffer may be $\tau_1 + e_0$, another buffer delay may be $\tau_1 + e_1$, and another one may be $\tau_1 + e_2$, etc. These relative delay mismatches e_0, e_1, e_2, ... cause the nonlinearity of the TDC.

We compare their effects between the conventional vernia delay line TDC and the proposed TDC using MATLAB simulation and show that the linearity of the proposed TDC is better. We consider the case that both TDCs use τ_1=30ps and τ_2=20ps and can measure the time interval from 0 to 1,000ps. We assume that the relative mismatches among τ_1 buffers are the same for both TDCs and also those among τ_2 buffers are the same.

Fig.4 shows the histgrams of the input range variation for the conventional vernia delay line TDC and the proposed TDC. We see that the variation (which corresponds to integral nonlinearity due to the buffer delay relative mismatches) is smaller for the proposed TDC; this is due to the fact that the number of total buffers used in the proposed TDC is only half of that in the conventional TDC.

V. Design and Measurements of the Proposed TDC

We have designed and laid out the proposed TDC using TSMC 0.18um CMOS process (Figs.5,6), and Fig.7 shows its chip photo. Fig.8 shows measured waveforms of the TDC in Fig.5 which demonstrates that the principle of our proposed TDC architecture functions.

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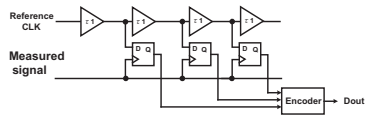
References

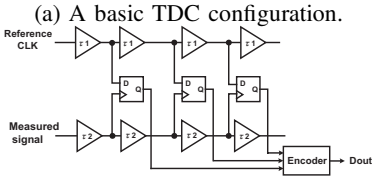
[1] S.Henzler, et.al., "90nm 4.7ps-Resolution 0.7-LSB Single-Shot Precision and 19pJ-per-Shot Local Passive Interpolation Time-to-Digital Converter with On-Chip Characterization", *ISSCC* (Feb. 2008).
[2] R.B.Staszewski, et.al., "1.3V 20p Time-to-Digital Converter for Frequency Synthesis in 90-nm CMOS", *IEEE Trans. CAS II* (Mar.2006).

978-1-4244-2749-9/09/$25.00 ©2009 IEEE

[3] M. Lee, A. A. Abidi, "A 9b,1.25ps Resolution Coarse-Fine Time-to-Digital Converter in 90nm CMOS that Amplifies a Time Residue", *Symposium on VLSI Circuits* (June 2007).
[4] K. Nose, et. al., "A 1-ps Resolution Jitter Measurement Macro Using Interpolated Jitter Oversampling", *IEEE JSSC* (Dec.2006).
[5] C. Hsu, et.al., "A Low-Noise,Wide-BW 3.6GHz Digital ΔΣ Fractional-N Frequency Synthesizer with a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation," *ISSCC* (Feb. 2008).
[6] T. Komuro, et.al., "ADC Architecture Using Time-to-Digital Converter", *IEICE* vol. J90-C (April 2007).



(a) A basic TDC configuration.



(b) A vernier delay line TDC.

Fig. 1. Conventional TDC architectures.

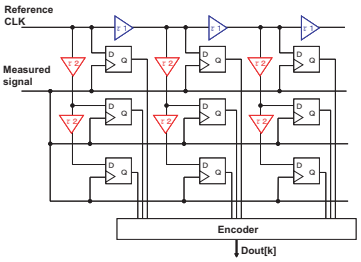
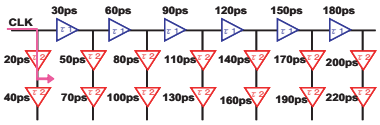
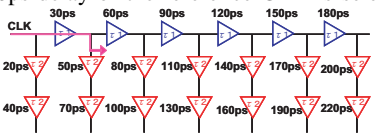


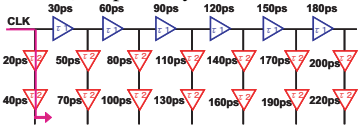
Fig. 2. Proposed TDC configuration.



(a) 20ps delay of the reference CLK is selected.



(b) 30ps delay is selected.



(c) 40ps delay is selected.

Fig. 3. A delay line in the proposed TDC with τ_1=30ps, τ_2=20ps.

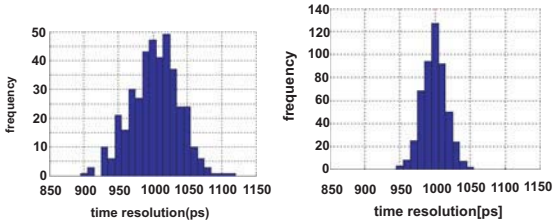


Fig. 4. Simulated TDC nonlinearity results due to buffer delay mismatches for the conventional vernier delay line TDC (left) and the proposed TDC (right).

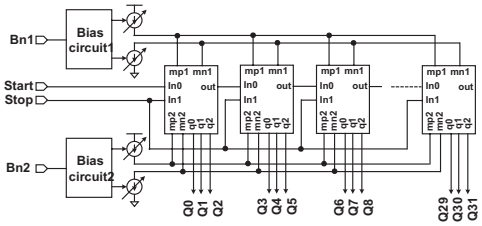


Fig. 5. The prototype TDC with the proposed architecture.

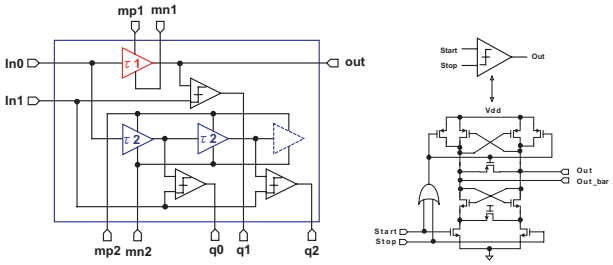


Fig. 6. Unit cell circuit in the prototype TDC (left), and a latched comparator circuit used there (right).

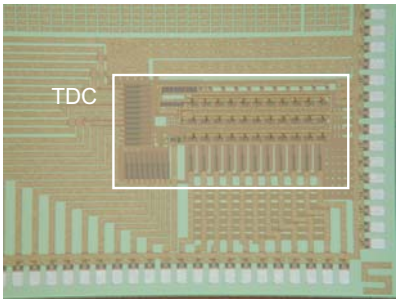


Fig. 7. Prototype TDC chip photo ($500\mu m \times 1,000\mu m$).

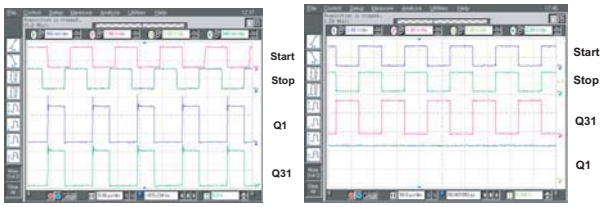


Fig. 8. Measured waveforms of the TDC in Fig.5.