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Input-Dependent Sampling-Time Error Effects in MOS Sampling Circuits

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Abstract - This paper analyzes the input-dependent sample-time error in MOS sampling circuits caused by the finite slope of the sampling clock, and clarifies the following: (i) Input-dependent sampling jitter causes phase modulation in the sampled data. (ii) The formulas for SDR due to such sampling errors are explicitly derived. (iii) NMOS sampling circuits generate even-order harmonics, which are greatly reduced by using a differential topology. (iv) CMOS sampling circuits *without* clock skew between V_{clk} and $\overline{V_{clk}}$ generate odd-order harmonics which a differential topology cannot help cancel, whereas circuits *with* clock skew generate even-order as well as odd-order harmonics. (v) For single-ended sampling circuits, the SDR of CMOS circuits *without* clock skew is better than that of NMOS circuits. (vi) NMOS differential sampling circuits are relatively insensitive to input-dependent sampling jitter effects, which would be the best regarding to the input-dependent sampling jitter effects.

Keywords: Sampling, Jitter, MOS Switch, Track/Hold Circuit, ADC

I. Introduction

Let us consider the NMOS sampling circuit in Fig.1 (a). Suppose that the sampling clock V_{clk} has a finite slope (Fig.2) and the ideal sampling time is defined to be the negative-going $(M + V_{thn})$-crossing of V_{clk}. (Here V_{thn} is the threshold voltage of the NMOS transistor.) Then the actual sampling time is that when V_{clk} passes through the value when it exceeds a threshold voltage of the NMOS transistor. In other words, the NMOS switch in Fig.1 (a) turns off when V_{clk} is above V_{in} by V_{thn}. Thus when V_{in} is above M, the actual sampling time is earlier than the ideal sampling time, whereas when V_{in} is less than M, it is later. Then we see that the finite slope of the sampling clock effectively causes input-dependent sampling time error (effective jitter) [1, 2, 3] even though the sampling clock does not have physical jitter [4, 5]. In this paper we analyze this effect rigorously for NMOS, PMOS and CMOS sampling circuits.

Throughout this paper, we assume that the input for a single-ended sampling circuit (Fig.1) is given by

$$V_{in}(t) = A\sin(\omega t) + M.$$

Also the inputs for a differential sampling circuit (Fig.3) are

$$V_{inp}(t) = \frac{A}{2}\sin(\omega t) + M,\ V_{inm}(t) = -\frac{A}{2}\sin(\omega t) + M.$$

We also suppose that the sampling clock V_{clk} for NMOS switches starts to fall at time t_{sn} (Fig.4 (a)), and in the falling transient V_{clk} is expressed by

$$V_{clk}(t) = -(V_{dd}/t_{TR}) \cdot (t - t_{sn}) + V_{dd}. \qquad (1)$$

Also the sampling clock $\overline{V_{clk}}$ for PMOS switches starts to fall at time t_{sp} (Fig.4 (b)), and in the rising transient it is expressed by

$$\overline{V_{clk}}(t) = (V_{dd}/t_{TR}) \cdot (t - t_{sp}). \qquad (2)$$

II. NMOS Sampling Circuit

2.1 Single-Ended Sampling Circuit

Let us consider the case when V_{clk} is in the falling transient state in an NMOS sampling circuit (Fig.1 (a)), and the NMOS switch turns off at time $t_{sn}+\delta t_n$. Then we have

$$V_{clk}(t_{sn} + \delta t_n) = V_{in}(t_{sn} + \delta t_n) + V_{thn}$$

and it follows from eq.(1) that

$$-\frac{V_{dd}}{t_{TR}}\delta t_n + V_{dd} = V_{in}(t_{sn} + \delta t_n) + V_{thn}.$$

Then we have

$$\begin{aligned} & t_{sn} + \delta t_n \\ &= t_{sn} + \frac{t_{TR}}{V_{dd}}(V_{dd} - V_{in}(t_{sn} + \delta t_n) - V_{thn}) \\ &\approx t_{sn} + \frac{t_{TR}}{V_{dd}}(V_{dd} - A\sin(\omega t) - M - V_{thn}) \\ &= t_{\rm refn} + \delta t'_n. \end{aligned}$$

Here, $t_{\rm refn}$ is the reference (ideal) sampling time (Fig.4 (a)) and $\delta t'_n$ denotes the deviation of the actual sampling time from $t_{\rm refn}$, which are given by

$$t_{\rm refn} := t_{sn} + \frac{t_{TR}}{V_{dd}}(V_{dd} - M - V_{thn})$$

$$\delta t'_n := -\frac{t_{TR}A}{V_{dd}}\sin(\omega t).$$

Since

$$V_{in}(t_{\rm refn} + \delta t'_n) \approx V_{in}(t_{\rm refn}) + \big[\frac{d}{dt}V_{in}(t)\big]_{t=t_{\rm refn}} \delta t'_n,$$

the sampled output is given by

$$V_{out}(t) \approx A\sin(\omega t + \phi(t)) + M$$

$$\text{where} \qquad \phi(t) := \frac{A\omega t_{TR}}{V_{dd}}\sin(\omega t).$$

We see that the input dependent sampling jitter causes *phase modulation*. Fig.5 (a) illustrates ideal and actual sampling points.

$$\text{When} \quad \frac{A\omega t_{TR}}{V_{dd}} << 1, \quad \text{then } |\phi(t)| << 1,$$

and we have the following sampled output:

$$\begin{aligned} V_{out}(t) &\approx A\big[\sin(\omega t)\cos(\phi(t)) + \cos(\omega t)\sin(\phi(t))\big] + M \\ &\approx A\big[\sin(\omega t)(1 - \frac{1}{2}\phi(t)^2) + \cos(\omega t)\cdot\phi(t)\big] + M \\ &= A\big(1 - \frac{3A^2\omega^2 t_{TR}^2}{8V_{dd}^2}\big)\sin(\omega t) + \frac{A^2\omega t_{TR}}{2V_{dd}}\sin(2\omega t) \\ &\quad + \frac{A^3\omega^2 t_{TR}^2}{8V_{dd}^2}\sin(3\omega t) + M \\ &\approx A\sin(\omega t) + \frac{A^2\omega t_{TR}}{2V_{dd}}\sin(2\omega t) + M. \end{aligned}$$

We see that when $A\omega t_{TR}/V_{dd} << 1$, the second harmonic is dominant rather than the third harmonic. In this case, Signal-to-Distortion Ratio (SDR) is given by

$$SDR = 20\log_{10}\frac{A}{A^2\omega t_{TR}/(2V_{dd})} = 20\log_{10}\frac{2V_{dd}}{A\omega t_{TR}}\ [\text{dB}].$$

Remark The above equation yields to

$$\begin{aligned} SDR &= 20\log_{10}\frac{2V_{dd}}{A(2\pi f)t_{TR}} = 20\log_{10}\frac{V_{dd}}{2Aft_{TR}} \\ &\quad + 20\log_{10}\frac{2}{\pi} = 20\log_{10}\frac{V_{dd}}{A_{pp}ft_{TR}} - 4\ [\text{dB}]. \end{aligned}$$

This corresponds to the result in [3] which was derived empirically by simulation.

2.2 Differential Sampling Circuit

Now consider a differential sampling circuit (Fig.3 (a)), and Fig.5 (b) illustrates ideal and actual sampling points. Similarly we have their sampled outputs:

$$V_{outp}(t) \approx \frac{A}{2}\sin(\omega t + \frac{\phi(t)}{2}) + M,$$

$$V_{outm}(t) \approx -\frac{A}{2}\sin(\omega t - \frac{\phi(t)}{2}) + M.$$

Then the differential output is given by

$$\begin{aligned} V_{out}(t) &:= V_{outp}(t) - V_{outm}(t) \\ &= \frac{A}{2}\big[\sin(\omega t - \frac{\phi(t)}{2}) + \sin(\omega t + \frac{\phi(t)}{2})\big] \\ &= A\sin(\omega t)\cos(\frac{\phi(t)}{2}) \approx A\sin(\omega t)\cdot(1 - \frac{1}{8}\phi(t)^2) \\ &= A(1 - \frac{3A^2\omega^2 t_{TR}^2}{32V_{dd}^2})\cdot\sin(\omega t) + \frac{A^3\omega^2 t_{TR}^2}{32V_{dd}^2}\sin(3\omega t) \\ &\approx A\sin(\omega t) + \frac{A^3\omega^2 t_{TR}^2}{32V_{dd}^2}\sin(3\omega t). \end{aligned}$$

We see that the second harmonic (which is the most dominant error) is cancelled, and SDR is given by

$$SDR = 20\log_{10}\frac{32V_{dd}^2}{A^2\omega^2 t_{TR}^2} = 2\left[20\log_{10}\frac{2V_{dd}}{A\omega t_{TR}}\right] + 18\ [\text{dB}].$$

Next we will consider the case that *clkp* and *clkm* in Fig.3 (b) has a skew of t_{skw}. We have

$$V_{outp}(t) \approx \frac{A}{2}\sin(\omega t + \frac{1}{2}(\phi(t) - \omega t_{skw})) + M,$$

$$V_{outm}(t) \approx -\frac{A}{2}\sin(\omega t - \frac{1}{2}(\phi(t) - \omega t_{skw})) + M.$$

Then the differential output is given by

$$\begin{aligned} V_{out}(t) &:= V_{outp}(t) - V_{outm}(t) \\ &\approx a_0 + A\sin(\omega t) + a_2\cos(2\omega t) + b_3\sin(3\omega t), \\ \text{where } & a_0 := \alpha\beta, \quad a_2 := -\alpha\beta, \quad b_3 := \alpha/8 \end{aligned}$$

$$\alpha := \frac{A^3\omega^2 t_{TR}^2}{4V_{dd}^2}, \qquad \beta := \frac{V_{dd}t_{skw}}{2At_{TR}}.$$

Also SDR is given by

$$\begin{aligned} SDR &= 10log_{10}\frac{a_0^2 + (a_2^2 + b_3^2)/2}{A^2/2} \\ &= 2\Big[20\log_{10}\frac{2V_{dd}}{A\omega t_{TR}}\Big] \\ &\quad +18 - 10\log_{10}(64\beta^2 + 1) \quad \text{[dB]}. \end{aligned}$$

3. PMOS Sampling Circuit

The reader can refer to [6] in PMOS sampling circuit case (Fig.1 (b)).

4. CMOS Sampling Circuit

Consider the CMOS sampling circuit in Fig.1 (c).

4.1 Zero Clock Skew Case

Suppose that there is no skew between V_{clk} and $\overline{V_{clk}}$; in other words $t_{\rm refn} = t_{\rm refp}$ as shown in Fig.6 (a).

A. Single-Ended Sampling Circuit: Fig.7 (a) illustrates ideal and actual sampling points. Noting that the CMOS switch is off when both NMOS and PMOS switches are off, we have the sampled output as follows:

$$\begin{aligned} V_{out}(t) &\approx A\sin(\omega t - |\phi(t)|) + M \\ &= A\big[\sin(\omega t)\cos(|\phi(t)|) - \cos(\omega t)\sin(|\phi(t)|)\big] + M \\ &\approx A\big[\sin(\omega t)(1 - \frac{1}{2}\phi(t)^2) - \cos(\omega t)\cdot|\phi(t)|\big] + M \\ &= A\big(1 - \frac{3A^2\omega^2 t_{TR}^2}{8V_{dd}^2}\big)\sin(\omega t) + \frac{A^3\omega^2 t_{TR}^2}{8V_{dd}^2}\sin(3\omega t) \\ &\quad -\frac{A^2\omega t_{TR}}{V_{dd}}\cos(\omega t)|\sin(\omega t)| + M. \end{aligned}$$

Noting that $|\sin(\omega t)| = \frac{2}{\pi}\Big[1 - 2\sum_{n=1}^{\infty}\frac{\cos(2n\omega t)}{4n^2-1}\Big]$,

we see that $V_{out}(t)$ has odd harmonics but does not have even harmonics.

$$\begin{aligned} V_{out}(t) &\approx A\sin(\omega t) + \frac{4A^2\omega t_{TR}}{3\pi V_{dd}}\cos(\omega t)\cos(2\omega t) + M \\ &\approx A\sin(\omega t) + \frac{2A^2\omega t_{TR}}{3\pi V_{dd}}\cos(3\omega t) + M. \end{aligned}$$

Then SDR is given by

$$SDR = 20\log_{10}\frac{3\pi V_{dd}}{2A\omega t_{TR}} = 20\log_{10}\frac{2V_{dd}}{A\omega t_{TR}} + 7.44 \text{ [dB]}.$$

B. Differential Sampling Circuit : For a differential circuit, the sampled outputs are given by

$$\begin{aligned} V_{outp}(t) &\approx \frac{A}{2}\sin(\omega t - \frac{|\phi(t)|}{2}) + M, \\ V_{outm}(t) &\approx -\frac{A}{2}\sin(\omega t - \frac{|\phi(t)|}{2}) + M, \end{aligned}$$

$V_{out}(t) := V_{outp}(t) - V_{outm}(t) = A\sin(\omega t - \frac{|\phi(t)|}{2})$.

Fig.7 (b) illustrates ideal and actual sampling points. We see that the phase modulation index (the intensity of the phase modulation) due to the input-dependent sampling jitter is reduced by a factor of 2. However, the harmonics caused by it are not cancelled because all of them are odd harmonics; using a differential circuit does not help reduce harmonics caused by input-dependent sampling jitter in a CMOS sampling circuit without clock skew.

4.2 Finite Clock Skew Case

Suppose that there is a finite timing skew t_{skew} between V_{clk} and $\overline{V_{clk}}$ ($t_{skew} := t_{\rm refn} - t_{\rm refp} \neq 0$ as shown in Fig.6 (b)) and $\omega t_{skew} << 1$. Note that the clocks for NMOS and PMOS switches are respectively given by

$$\begin{aligned} V_{clk}(t) &= -\frac{V_{dd}}{t_{TR}}(t - t_{sn} - \frac{t_{skew}}{2}) + V_{dd} \\ \overline{V_{clk}}(t) &= \frac{V_{dd}}{t_{TR}}(t - t_{sp} + \frac{t_{skew}}{2}). \end{aligned}$$

A. Single-Ended Sampling Circuit : We have the sampled output

$$\begin{aligned} V_{out}(t) &\approx A\sin(\omega t - |\phi(t) - \frac{\omega t_{skew}}{2}|) + M \\ &= A\Big[\sin(\omega t)\cos(|\phi(t) - \frac{\omega t_{skew}}{2}|) \\ &\quad - \cos(\omega t)\sin(|\phi(t) - \frac{\omega t_{skew}}{2}|)\Big] + M \\ &\approx A\sin(\omega t)\cdot\Big(1 - \frac{1}{2}(\phi(t) - \frac{\omega t_{skew}}{2})^2\Big) \\ &\quad - A\cos(\omega t)\cdot|\phi(t) - \frac{\omega t_{skew}}{2}| + M. \end{aligned}$$

$$\text{Let} \quad \epsilon := (V_{dd}t_{skew})/(2At_{TR})$$

and note that in case that $-1 \le \epsilon \le 1$,

$$\begin{aligned}
&|\phi(t) - \frac{\omega t_{skew}}{2}| \\
&= |\frac{A\omega t_{TR}}{V_{dd}}\sin(\omega t) - \frac{\omega t_{skew}}{2}| \\
&= \frac{A\omega t_{TR}}{V_{dd}}|\sin(\omega t) - \epsilon| \\
&\approx \frac{2A\omega t_{TR}}{\pi V_{dd}}\Big[\sqrt{1-\epsilon^2} + \epsilon\sin^{-1}(\epsilon) \\
&\quad - [\sin^{-1}(\epsilon) + 3\epsilon\sqrt{1-\epsilon^2}]\sin(\omega t) \\
&\quad - \frac{2}{3}(1+5\epsilon^2)\sqrt{1-\epsilon^2}\cos(2\omega t)\Big],
\end{aligned}$$

in case that $1 \le \epsilon$,

$$|\phi(t) - \frac{\omega t_{skew}}{2}| = -\frac{A\omega t_{TR}}{V_{dd}}(\sin(\omega t) - \epsilon),$$

and in case that $\epsilon \le -1$,

$$|\phi(t) - \frac{\omega t_{skew}}{2}| = \frac{A\omega t_{TR}}{V_{dd}}(\sin(\omega t) - \epsilon).$$

Then we have the following:
(i) In case that $-1 \le \epsilon \le 1$:

$$\begin{aligned}
V_{out}(t) &\approx A\sin(\omega t) \\
&+ \frac{A^2\omega t_{TR}}{\pi V_{dd}}\Big[\sin^{-1}(\epsilon) + 3\epsilon\sqrt{1-\epsilon^2}\Big]\sin(2\omega t) \\
&+ \frac{2A^2\omega t_{TR}}{3\pi V_{dd}}(1+5\epsilon^2)\sqrt{1-\epsilon^2}\cos(3\omega t) + M.
\end{aligned}$$

$$SDR = 20\log_{10}\frac{2V_{dd}}{A\omega t_{TR}} + 7.44 - 10\log_{10}\gamma \text{ [dB]}.$$

$$\begin{aligned}
\text{Here} \quad \gamma &:= \frac{9}{4}\sin^{-2}(\epsilon) + \frac{27}{2}\sqrt{1-\epsilon^2}\sin^{-1}(\epsilon) \\
&\quad + [(1+5\epsilon^2)^2 + \frac{81}{4}\epsilon^2](1-\epsilon^2).
\end{aligned}$$

(ii) In case that $\epsilon \ge 1$:

$$V_{out}(t) \approx A\sin(\omega t) + \frac{A^2\omega t_{TR}}{2V_{dd}}\sin(2\omega t) + M.$$

$$SDR = 20\log_{10}\frac{2V_{dd}}{A\omega t_{TR}} \text{ [dB]}.$$

This corresponds to an NMOS sampling circuit case.
(iii) In case that $\epsilon \le -1$:

$$V_{out}(t) \approx A\sin(\omega t) - \frac{A^2\omega t_{TR}}{2V_{dd}}\sin(2\omega t) + M.$$

$$SDR = 20\log_{10}\frac{2V_{dd}}{A\omega t_{TR}} \text{ [dB]}.$$

This corresponds to a PMOS sampling circuit case.

B. Differential Sampling Circuit: We have the sampled outputs

$$V_{outp}(t) \approx \frac{A}{2}\sin\big(\omega t - \frac{1}{2}|\phi(t) - wt_{skew}|\big) + M,$$

$$V_{outm}(t) \approx -\frac{A}{2}\sin\big(\omega t - \frac{1}{2}|\phi(t) + wt_{skew}|\big) + M,$$

$$\begin{aligned}
V_{out}(t) &= V_{outp}(t) - V_{outm}(t) \\
&\approx A\sin\big(\omega t - \frac{1}{4}\{|\phi(t) - \omega t_{skew}| + |\phi(t) + \omega t_{skew}|\}\big) \\
&\times \cos\big(\frac{1}{4}\{|\phi(t) - \omega t_{skew}| - |\phi(t) + \omega t_{skew}|\}\big).
\end{aligned}$$

(i) In case $-1/2 \le \epsilon \le 1/2$:

$$V_{out}(t) \approx A\sin(\omega t) + c_3\cos(3\omega t) + d_3\sin(3\omega t),$$

$$\text{where} \quad c_3 := \frac{A^2\omega t_{TR}}{3\pi V_{dd}}(1+20\epsilon^2)\sqrt{1-4\epsilon^2},$$
$$d_3 := \frac{A^3\omega^2 t_{TR}^2}{8\pi^2 V_{dd}^2}\sin^{-2}(2\epsilon).$$

We see that even-order harmonics are cancelled.

$$SDR = 10\log_{10}\frac{A^2}{c_3^2 + d_3^2} \text{ [dB]}.$$

(ii) In case $\epsilon \le -1/2$ or $\epsilon \ge 1/2$:

$$V_{out}(t) \approx A\sin(\omega t) + \frac{A^3\omega^2 t_{TR}^2}{32V_{dd}^2}\sin(3\omega t).$$

$$SDR = 20\log_{10}\frac{32V_{dd}^2}{A^2\omega^2 t_{TR}^2} \text{ [dB]}.$$

This corresponds to an NMOS or PMOS sampling circuit case.

Figs.9 and 10 show numerical simulation results of SDR due to the input-dependent sampling jitter.

5. Conclusion

We have analyzed the input-dependent sample-time error in MOS sampling circuits caused by the finite slope of the sampling clock, and the results would be useful for designing high-speed CMOS sampling circuits.

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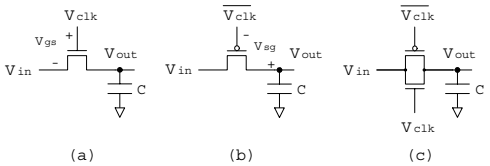

Fig.1: NMOS, PMOS and CMOS sampling circuits.

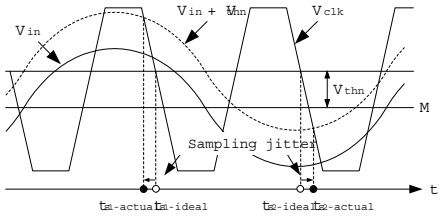

Fig.2: Waveforms for V_{in} and V_{clk} to illustrate how a finite slope of V_{clk} introduces V_{in}-dependent sampling time error (effective jitter).

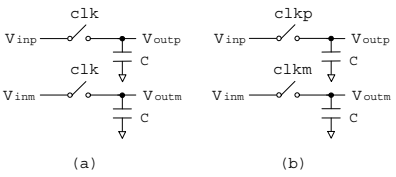

Fig.3: Differential sampling circuits. (a) Without clock skew. (b) With clock skew of t_{skw} between *clkp* and *clkm*.

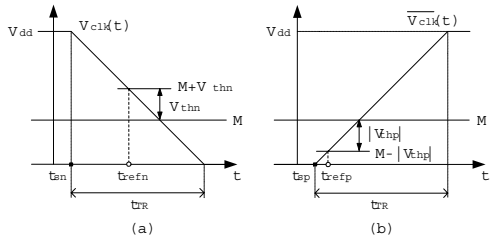

Fig.4: Sampling clocks V_{clk}, $\overline{V_{clk}}$ and reference sampling timing t_{refn}, t_{refp}. (a) NMOS sampling circuit. (b) PMOS sampling circuit.

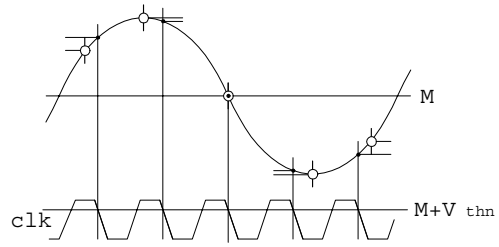

Fig.5: (a) Ideal (·) and actual (○) sampling points in a single-ended NMOS sampling circuit.

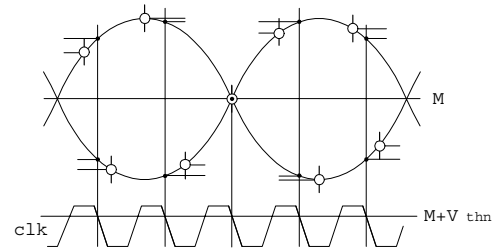

Fig.5: (b) Ideal (·) and actual (○) sampling points in a differential NMOS sampling circuit.

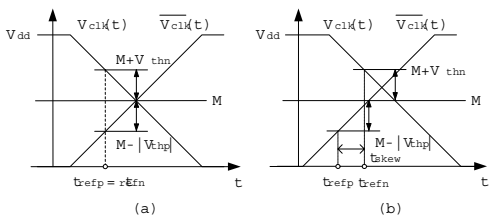

Fig.6: Sampling clocks V_{clk}, $\overline{V_{clk}}$ in a CMOS sampling circuit. (a) Without skew. (b) With skew of

t_{skew} between V_{clk} and $\overline{V_{clk}}$.

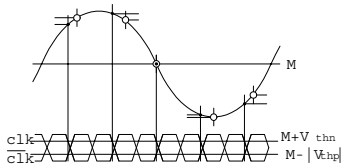

Fig.7 (a): Ideal (·) and actual (○) sampling points in a single-ended CMOS sampler without clock skew.

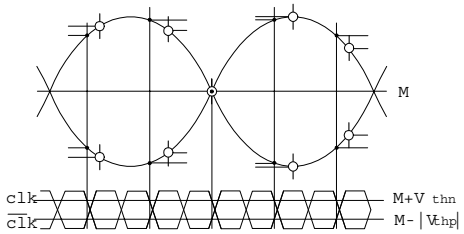

Fig.7 (b): Ideal (·) and actual (○) sampling points in a differential CMOS sampler without clock skew.

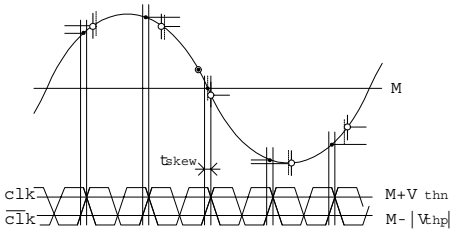

Fig.8 (a): Ideal (·) and actual (○) sampling points in a single-ended CMOS sampler with clock skew of t_{skew}.

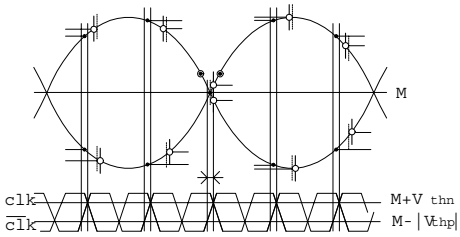

Fig.8 (b): Ideal (·) and actual (○) sampling points in a differential CMOS sampler with clock skew of t_{skew}.

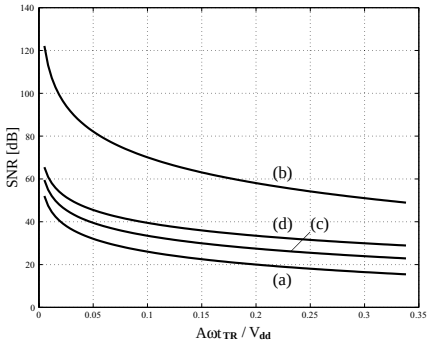

Fig.9: Calculated SDR based on derived formulas versus $A\omega t_{TR}/V_{dd}$. (a) A single-ended NMOS sampler. (b) A differential NMOS sampler. (c) A single-ended CMOS sampler without clock skew. (d) A differential CMOS sampler without clock skew.

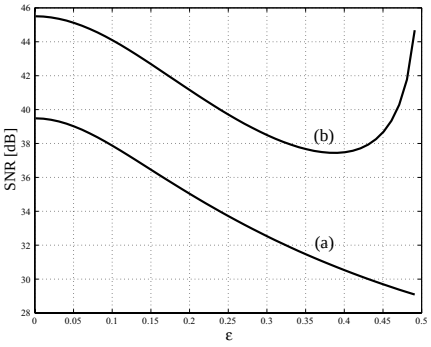

Fig.10: Calculated SDR based on derived formulas versus clock skew in CMOS sampling circuits. The horizontal axis indicates $\epsilon := (A\omega^2 t_{TR} t_{skew})/(2V_{dd})$, where $A\omega t_{TR}/V_{dd} = 0.05$. (a) A single-ended CMOS sampler with clock skew. (b) A differential CMOS sampler with clock skew. The SDR curve (b) in Fig.10 increases for a large ϵ; this is because as ϵ increases the second-harmonics (which can be cancelled by a differential topology) increases while the third-harmonics decreases. Note that for a very large ϵ, the CMOS sampling circuit becomes equivalent to the NMOS (or PMOS) sampling circuit.