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Sampling clock jitter effects in digital-to-analog converters

Naoki Kurosawa[a], Haruo Kobayashi[a,*], Hideyuki Kogure[a], Takanori Komuro[b], Hiroshi Sakayori[b]

[a]*Department of Electronic Engineering, Gunma University, 1-5-1 Tenjin-cho, Kiryu 376-8515, Japan*
[b]*Agilent Technologies Japan Ltd., 9-1 Takakura-cho Hachioji, Tokyo 192-8510, Japan*

Abstract

This paper describes sampling clock jitter effects in digital-to-analog converters. A formula for the output error power due to sampling clock jitter for a sinusoidal input is derived and verified by numerical simulations, and its spectrum characteristics is shown. Also its effects on DAC SNR is clarified by numerical simulation as follows: (i) When the total noise power outside as well as inside the signal band is taken into account, the DAC SNR remains almost constant regardless of the sampling jitter. (ii) However, when an analog lowpass filter follows the DAC and only the noise power inside the signal band is considered, the DAC SNR degrades as the jitter increases and the input signal frequency becomes higher. Thus the sampling clock jitter is serious for the high speed DAC.

Keywords: Jitter; Sampling; DAC; Analog circuit; Spread spectrum

1. Introduction

Digital-to-analog converters (DACs) are essential components for measuring instruments (such as arbitrary waveform signal generators) and communication systems (such as transceivers), and higher sampling speed is being demanded for them [1–3]. For such high sampling speed DACs, their sampling clock jitter effects may be crucial; the clock jitter effects of DACs have not been well investigated, even though those of analog-to-digital converters (ADCs) and sampling circuits have been [4–8]. In this paper we analyze their effects theoretically and verify them by numerical simulations. In Section 2, the formula for the DAC output error power due to the sampling jitter is derived, and in Section 3, numerical simulation verifies the derived formula. In Section 4, the power spectrum characteristics of the DAC output error due to the sampling jitter is discussed, and in Section 5 we clarify by numerical simulations that sampling clock jitter degrades signal-to-noise ratio (SNR, one of the important performance metrics of the DAC [3]) significantly. Finally Section 6 provides conclusion.

2. DAC output error power due to sampling clock jitter

2.1. Problem formulation

Fig. 1 shows a DAC where a digital input $V_{in}(n)$ is applied with a sampling clock of *CLK*. Ideally the sampling clock *CLK* operates with a period of T_s for every cycle, however in reality its timing can fluctuate which is called jitter or phase noise (Fig. 2)

*Corresponding author. Tel.: +81-277-30-1788; fax: +81-277-30-1707.

E-mail address: k_haruo@el.gunma-u.ac.jp (H. Kobayashi).

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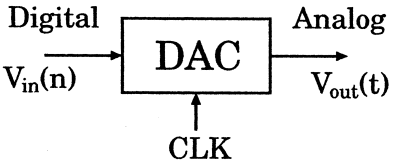

Fig. 1. A DAC with digital input signal, sampling clock and analog output signal.

[9,10]. If we denote jitter as ϵ_n, then the n-th sampling timing of CLK is $nT_s + \epsilon_n$ instead of nT_s. Since the jitter ϵ_n is sufficiently smaller than the sampling period of T_s in most of practical situations, we assume that

$$-\frac{T_s}{2} < \epsilon_n < \frac{T_s}{2}. \tag{1}$$

Also we suppose that the DAC has sufficiently good resolution so that quantization can be neglected, and the DAC output $V_{out}(t)$ is zero-order hold [3]. Then Fig. 3 shows the DAC outputs with an ideal clock (without jitter) and an actual clock (with jitter) while Fig. 4 shows the DAC output error due to jitter.

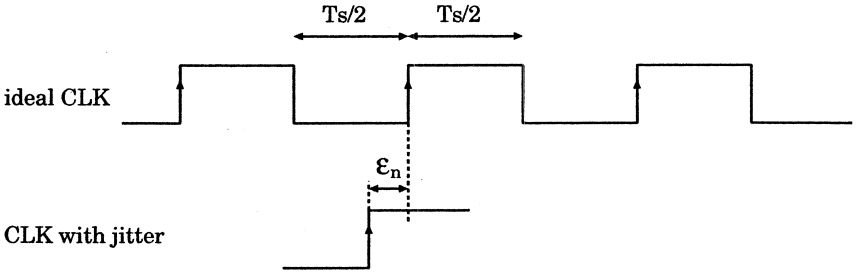

Fig. 2. Ideal sampling clock (without jitter) and actual sampling clock (with jitter ϵ_n) provided to a DAC.

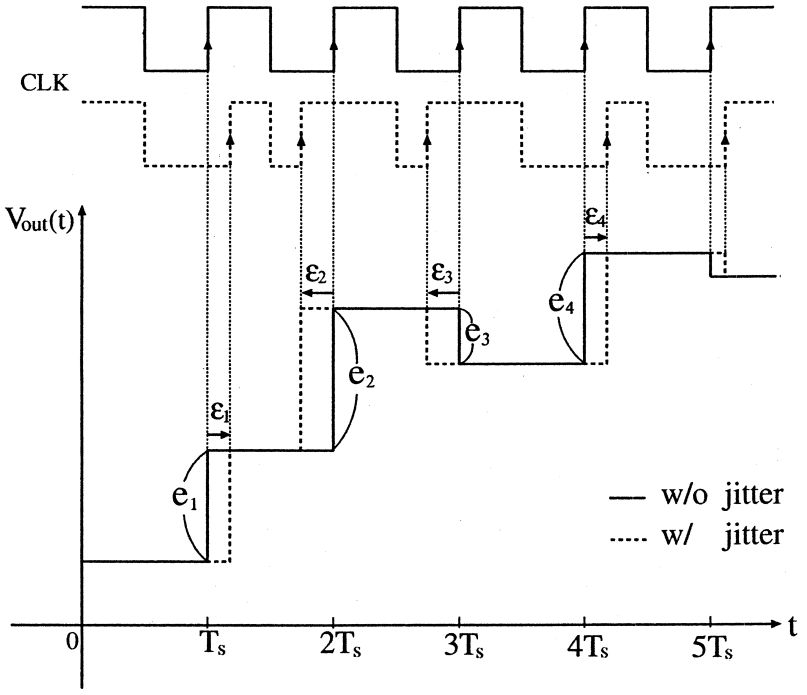

Fig. 3. DAC output waveforms with ideal sampling clock (without jitter) and actual sampling clock (with jitter ϵ_n).

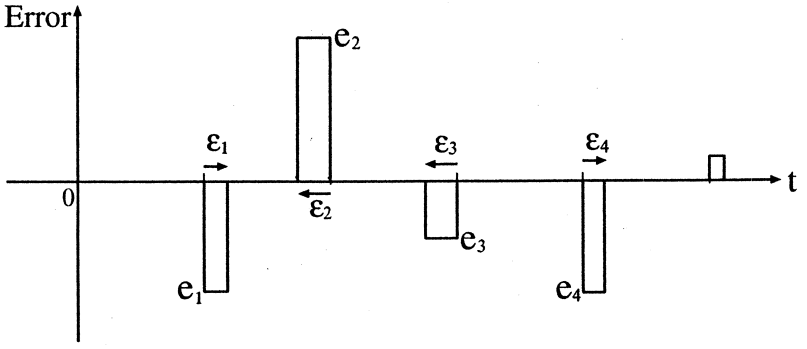

Fig. 4. DAC output error due to sampling clock jitter ϵ_n.

2.2. Error power formula due to jitter

The DAC output error power P_e due to the sampling clock jitter is defined as follows:

$$P_e := \lim_{N\to\infty} \frac{1}{N} \sum_{n=0}^{N-1} e_n^2 |\epsilon_n| \quad \text{(Time Average)} \\ = E[e_n^2 |\epsilon_n|] \quad \text{(Ensemble Average)}. \tag{2}$$

Here e_n is the DAC output error due to jitter (see Fig. 4). If the input signal $V_{in}(t)$ and the sampling jitter are not correlated (which is the case in general), ϵ_n and e_n are independent and we obtain

$$P_e = E[e_n^2] E[|\epsilon_n|]. \tag{3}$$

Proposition. When the input $V_{in}(n)$ to the DAC is a cosine wave

$$V_{in}(n) = A \cos\left(2\pi \frac{f_{in}}{f_s} n\right),$$

the error power P_e due to jitter is given by

$$P_e = 2A^2 \sin^2\left(\pi \frac{f_{in}}{f_s} n\right) E[|\epsilon|].$$

Here f_{in} is the input frequency and f_s is the sampling frequency ($f_s = 1/T_s$).

Proof of Proposition. See Appendix A.

Remark. The references of [11,12] discuss non-uniform sampling effects to DACs, however, our problem formulation is different from theirs. In Ref. [11], periodic fixed-amount of timing offsets are assumed for the DAC sampling clock; the n-th DAC sampling timing is $nT_s + \Delta_n$ instead of nT_s, where Δ_n is a periodic sequence with period M. This problem formulation is similar to that for the timing skew effect in time-interleaved ADC systems [4,13]. In Ref. [12] it is considered that the DAC sampling clock is phase-modulated by a deterministic sine wave and it is given by

$$A \cos(\omega_s t + \beta \sin(\omega_j t))$$

where ω_s is the nominal DAC clock frequency, ω_j is the jitter frequency and β is the modulation index. On the contrary, in this paper we consider the case that the DAC sampling clock is phase-modulated by a random signal, as described above in this section.

3. Numerical simulation of DAC output error power due to sampling clock jitter

Example 1. Suppose that the jitter ϵ_n follows a uniform distribution whose probability function $p(\epsilon_n)$ is shown in Fig. 5:

$$p(\epsilon_n) = \begin{cases} \dfrac{1}{2a} & (-a \le \epsilon_n \le a) \\ 0 & \text{(otherwise)}. \end{cases}$$

Note that $0 < a < T_s/2$ according to Eq. (1). Since

$$E[|\epsilon_n|] = \frac{1}{2} a,$$

we obtain

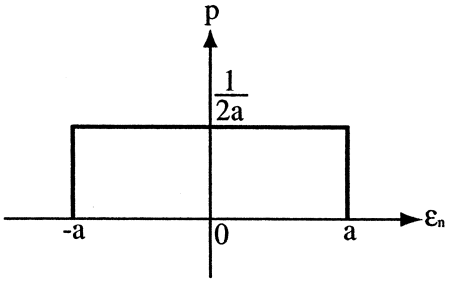

Fig. 5. Probability distribution of the jitter ϵ_n (uniform distribution, $0 < a < T_s/2$).

$$P_e = A^2 a \sin^2\left(\pi \frac{f_{in}}{f_s}\right). \quad (4)$$

Fig. 6 shows a graph of f_{in}/f_s versus P_e calculated numerically from Eq. (4) and a graph obtained from a DAC simulation including jitter, where $a = T_s/4$ and $A = 2$ are used in both cases. We see that both match well and hence Eq. (4) is verified by simulation.

Example 2. Suppose that the jitter ϵ_n follows a distribution whose probability function $p(\epsilon_n)$ is in triangular shape as shown in Fig. 7:

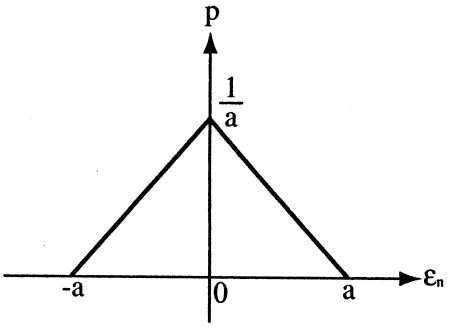

Fig. 7. Probability distribution of the jitter ϵ_n (triangular distribution, $0 < a < T_s/2$).

$$p(\epsilon_n) = \begin{cases} \dfrac{1}{a^2}(a - |\epsilon_n|) & (-a \le \epsilon_n \le a) \\ 0 & (\text{otherwise}). \end{cases}$$

Similarly, we assume $0 < a < T_s/2$ according to Eq. (1). Since

$$E[|\epsilon_n|] = \frac{1}{3}a,$$

we obtain

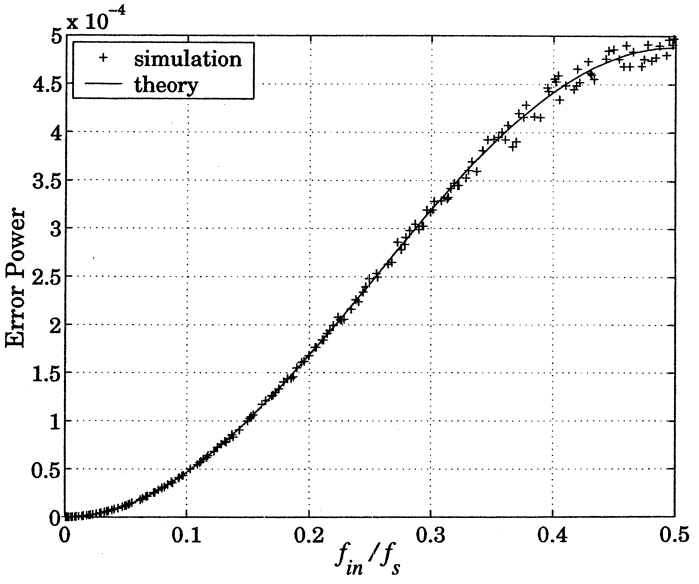

Fig. 6. f_{in}/f_s versus P_e characteristics for the cosine wave input of amplitude $A = 2$ and the jitter of the uniform distribution with $a = T_s/4$ (Fig. 5). The solid line shows numerical calculation results from Eq. (4) while + indicates DAC simulation results including jitter.

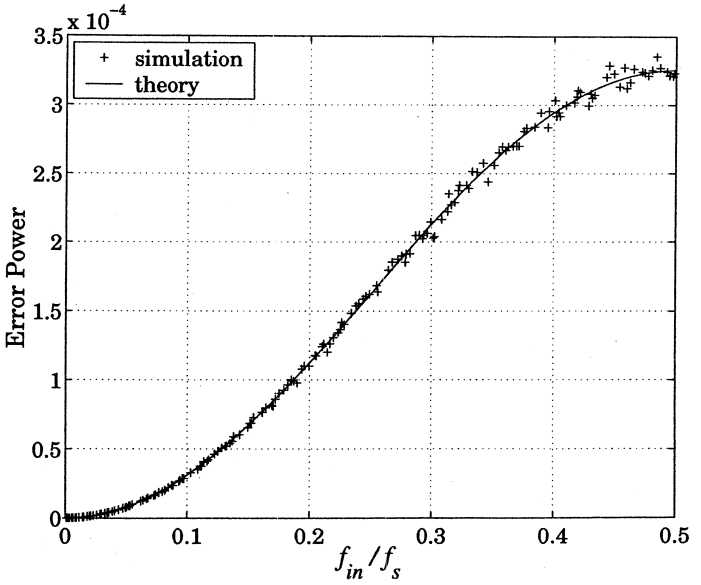

Fig. 8. f_{in}/f_s versus P_e characteristics for the cosine wave input of amplitude $A = 2$ and the jitter of the triangular distribution with $a = T_s/4$ (Fig. 7). The solid line shows numerical calculation results from Eq. (5) while + indicates DAC simulation results including jitter.

$$P_e = \frac{2}{3} A^2 a \sin^2\left(\pi \frac{f_{in}}{f_s}\right). \tag{5}$$

Fig. 8 shows a graph of f_{in}/f_s versus P_e calculated numerically from Eq. (5) and a graph obtained from a DAC simulation including jitter, where $a = T_s/4$ and $A = 2$ are used in both cases. We see that both match well and Eq. (5) is verified by simulation.

Example 3. Suppose that the jitter ϵ_n follows a distribution whose probability function is in cosine shape as shown in Fig. 9:

$$p(\epsilon_n) = \begin{cases} \dfrac{\pi}{4a} \cos\left(\dfrac{\pi \epsilon_n}{2a}\right) & (-a \le \epsilon_n \le a) \\ 0 & \text{(otherwise).} \end{cases}$$

Similarly, we assume $0 < a < T_s/2$ according to Eq. (1). Since

$$E[|\epsilon_n|] = \frac{a}{\pi}(\pi - 2),$$

we obtain

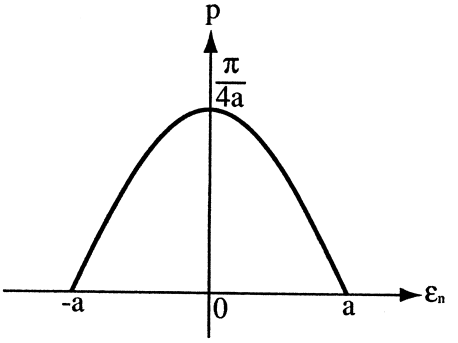

Fig. 9. Probability distribution of the jitter ϵ_n (cosine distribution, $0 < a < T_s/2$).

$$P_e = \frac{2}{\pi}(\pi - 2) A^2 a \sin^2\left(\pi \frac{f_{in}}{f_s}\right). \tag{6}$$

Fig. 10 shows a graph of f_{in}/f_s versus P_e calculated numerically from Eq. (6) and a graph obtained from a DAC simulation including jitter, where $a = T_s/4$ and $A = 2$ are used in both cases. We see that both match well and Eq. (6) is verified by simulation.

Example 4. Suppose that the jitter ϵ_n follows a

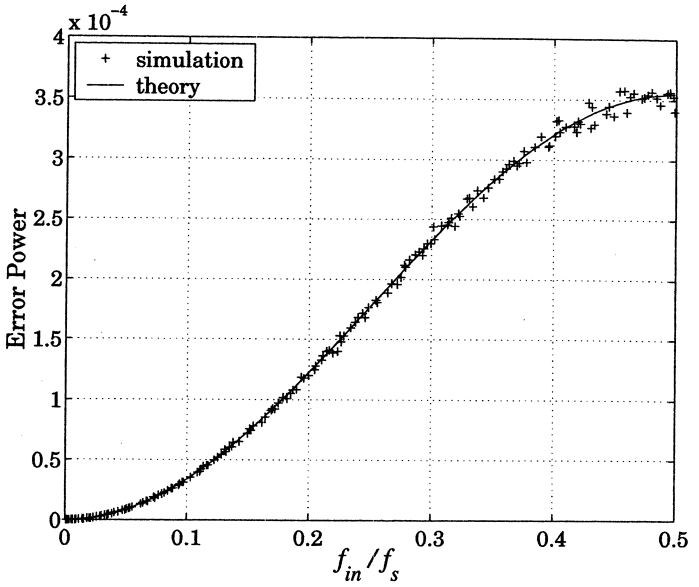

Fig. 10. f_{in}/f_s versus P_e characteristics for the cosine wave input of amplitude $A = 2$ and the jitter of the cosine distribution with $a = T_s/4$ (Fig. 9). The solid line shows numerical calculation results from Eq. (6) while + indicates DAC simulation results including jitter.

distribution whose probability function is in cosine squared shape as shown in Fig. 11:

$$p(\epsilon_n) = \begin{cases} \frac{1}{a}\cos^2\left(\frac{\pi\epsilon_n}{2a}\right) & (-a \le \epsilon_n \le a) \\ 0 & (\text{otherwise}). \end{cases}$$

Similarly, we assume $0 < a < T_s/2$ according to Eq. (1). Since

$$E[|\epsilon_n|] = \frac{a}{2\pi^2}(\pi^2 - 4),$$

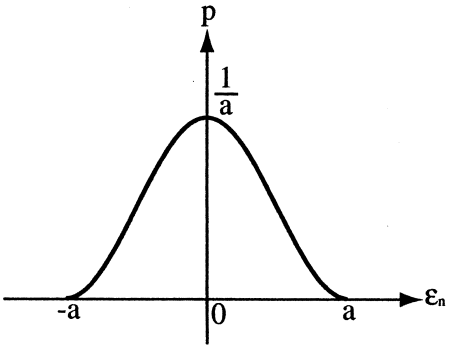

Fig. 11. Probability distribution of the jitter ϵ_n (cosine squared distribution, $0 < a < T_s/2$).

we obtain

$$P_e = \frac{1}{\pi^2}(\pi^2 - 4)A^2 a \sin^2\left(\pi\frac{f_{in}}{f_s}\right). \quad (7)$$

Fig. 12 shows a graph of f_{in}/f_s versus P_e calculated numerically from Eq. (7) and a graph obtained from a DAC simulation including jitter, where $a = T_s/4$ and $A = 2$ are used in both cases. We see that both match well and Eq. (7) is verified by simulation.

Remark. (i) The numerical simulation results in this section show the plausibility of ergodic process assumption in Eq. (2); Eqs. (4)–(7) are derived by ensemble average while the numerical simulation uses time average, and as Figs. 6, 8, 10 and 12 show that the equations and the simulation results match very well.

(ii) In general the quantization noise (which we neglect in our problem formulation in Section 2) and the noise due to the sampling jitter in a DAC are statistically independent. Hence the total error power when both the quantization and the sampling jitter exist is just the simple addition of the error power due to quantization and that due to the sampling jitter. We have confirmed this fact by numerical

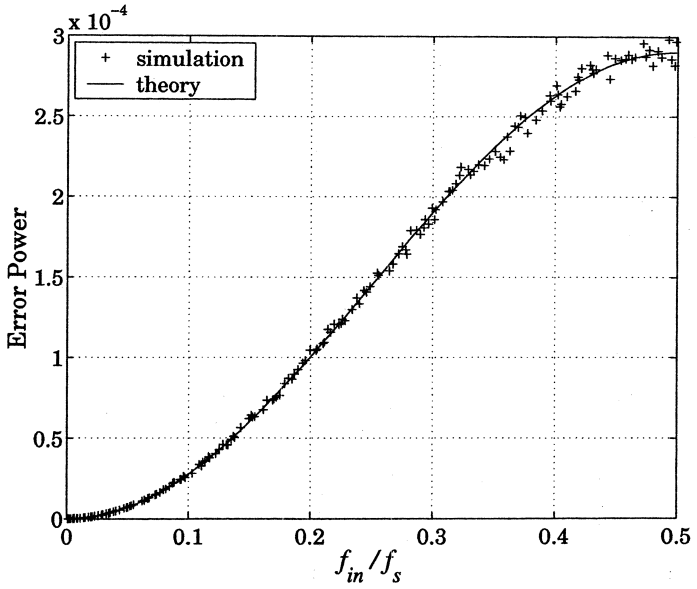

Fig. 12. f_{in}/f_s versus P_e characteristics for the cosine wave input of amplitude $A = 2$ and the jitter of the cosine squared distribution (Fig. 11) with $a = T_s/4$. The solid line shows numerical calculation results from Eq. (7) while + indicates DAC simulation results including jitter.

simulation; Fig. 13 shows simulation results for jitter and quantization effects, where jitter of the uniform distribution with $a = T_s/800$ (Fig. 5) and 6-bit quantization are assumed. We see that the error power when both jitter and quantization exist is the addition of the error power when only jitter exists to that when only quantization exists. According to our simulation, this fact holds for jitter of other dis-

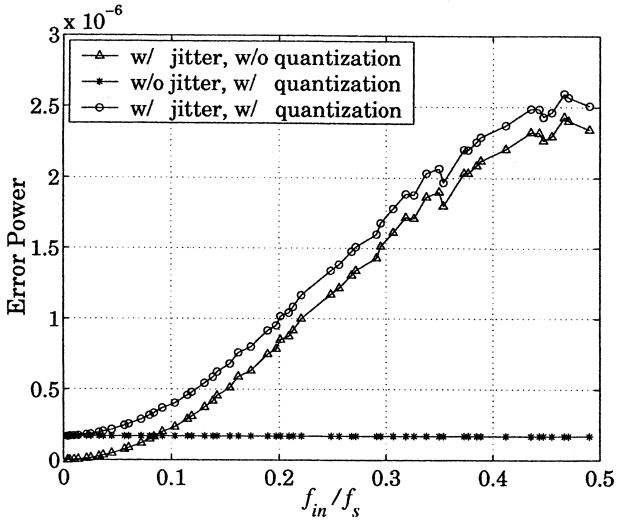

Fig. 13. Simulation results for jitter and quantization effects, where jitter of the uniform distribution with $a = T_s/800$ (Fig. 5) and 6-bit quantization are assumed. We see that the error power when both jitter and quantization exist are the addition of the error power when only jitter exists to that when only quantization exists.

tributions and other levels of quantization (e.g. 8-bit quantization).

(iii) According to our experiences, the cosine squared distribution in Example 4 (Fig. 11) approximates the actual jitter distribution most accurately.

4. Power spectrum of DAC output error due to sampling clock jitter

Next we will consider the power spectrum characteristics of the DAC output error due to the jitter. Suppose that the input $V_{\text{in}}(n)$ to the DAC is a cosine wave

$$V_{\text{in}}(n) = A\cos\left(2\pi\frac{f_{\text{in}}}{f_{\text{s}}}n\right)$$

and the DAC suffers from sampling clock jitter of the uniform distribution (Fig. 5). Fig. 14 shows simulation results of the power spectrum of the error, and we see that their power has peaks at

$$kf_{\text{s}} \pm f_{\text{in}} \quad (k = 1, 2, 3, \ldots). \tag{8}$$

Remark. For all of the other jitter distributions shown in the above examples, the error power due to the jitter has peaks at the same frequencies. This can be explained qualitatively as follows: the error can be approximated by multiplication of the sampling impulse by e_n, where $e_n = \pm 2A\ \sin(\pi(f_{\text{in}}/f_{\text{s}}))\ \sin(2\pi(f_{\text{in}}/f_{\text{s}})(n-\frac{1}{2}))$. The sampling impulse can be approximated by Fourier series with a fundamental frequency of f_{s}. Hence the peak frequencies of the DAC error power due to jitter are $kf_{\text{s}} \pm f_{\text{in}}$.

5. Sampling jitter effects on DAC SNR

According to Eq. (8), one might ponder as follows: '*If the input signal f_{in} is smaller than Nyquist frequency $f_s/2$ (which is usually the case), $kf_s \pm f_{in}$ are beyond $f_s/2$ for all of $k = 1, 2, 3, \ldots$ (in other words these are out of signal band) and hence the error peaks can be attenuated by an analog filter following the DAC. Therefore the sampling jitter effects on DACs are not serious.*' However, this statement is not true. Their effects are very serious and now we will show their effects to DAC SNR. Fig. 15 shows the power spectrum of a 10-bit ideal DAC output *without jitter* for $f_{\text{in}}/f_{\text{s}} = 103/512$. Since we consider the case that the DAC output is zero-order hold, the DAC output error due to the zero-order hold output has peaks of the power spectrum at $kf_{\text{s}} \pm f_{\text{in}}$ $(k = 1, 2, 3, \ldots)$ [3]. Then it follows from Eq. (8) that the DAC output errors due to jitter and zero-order hold have the peaks of the power spec-

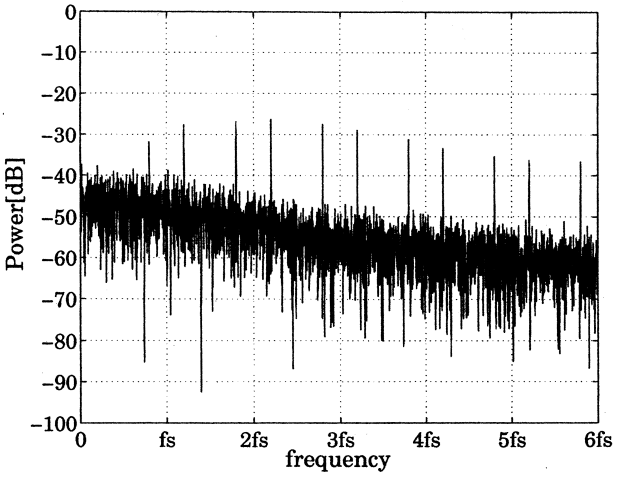

Fig. 14. The power spectrum of DAC output error power due to jitter (whose distribution is shown in Fig. 5 with $a = T_{\text{s}}/4$) for the input $V_{\text{in}}(n) = \cos(2\pi(f_{\text{in}}/f_{\text{s}})n)$ with $f_{\text{in}}/f_{\text{s}} = 103/512$. The peaks are located at $f_{\text{s}}k \pm f_{\text{in}}$ where $k = 1, 2, 3, \ldots$.

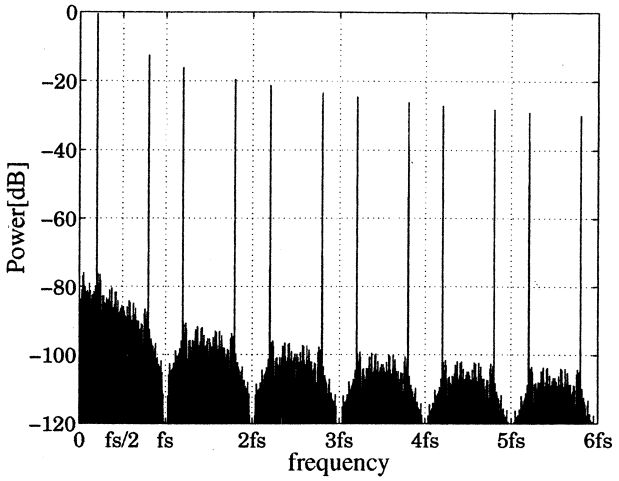

Fig. 15. The power spectrum of a 10-bit DAC zero-hold output without the sampling clock jitter for $f_{in}/f_s = 103/512$.

trum at the same frequencies. On the other hand, Fig. 16 shows the power spectrum of the same DAC *with jitter* (cosine squared distribution of $a = T_s/4$ in Fig. 11), and we see that the noise floor increases. Figs. 17 and 18 show the SNRs of the DAC with and without jitter, where the whole noise (outside as well as inside the signal band $f_s/2$) is considered. We see that SNR degrades slightly (by a few dB) due to the jitter. However, in practical situation, the DAC is often followed by an analog low filter which sufficiently attenuates the noise components beyond $f_s/2$. In this case we consider that SNR is given by 10 $\log_{10}$ {signal power}/{noise power between 0 to $f_s/2$ (total noise power in the signal band)} [dB], and Figs. 19 and 20 show the simulation results of SNRs using the above definition with the sampling clock

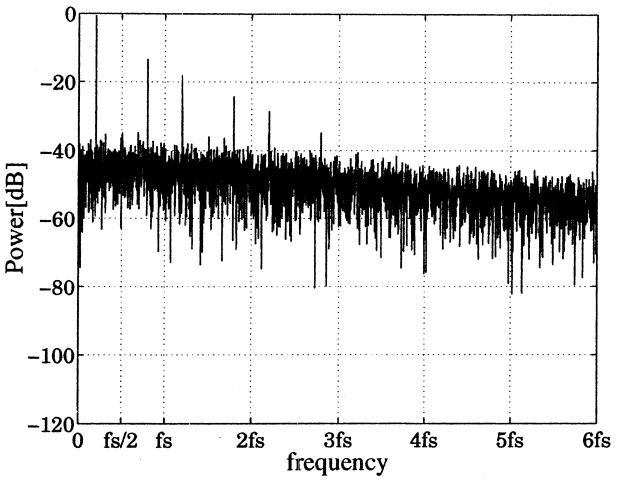

Fig. 16. The power spectrum of a 10-bit DAC zero-hold output with the sampling clock jitter of cosine squared distribution of $a = T_s/4$ (Fig. 11), for $f_{in}/f_s = 103/512$.

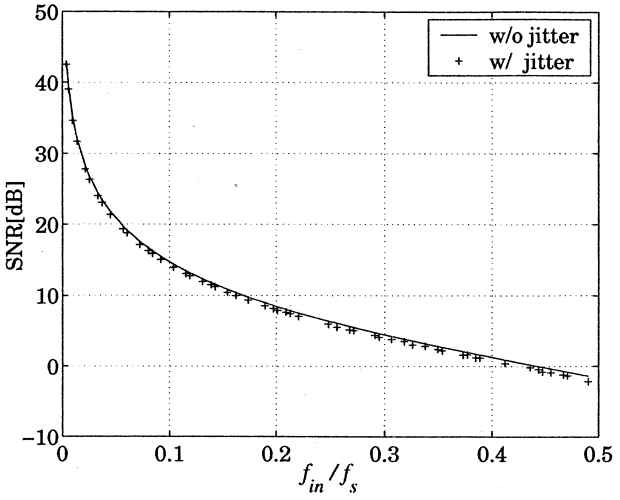

Fig. 17. Simulation result of SNR versus f_{in}/f_s of a 10-bit DAC with and without jitter of cosine squared distribution of $a = T_s/4$ (Fig. 11). Here the total noise power outside as well as inside the signal band is considered.

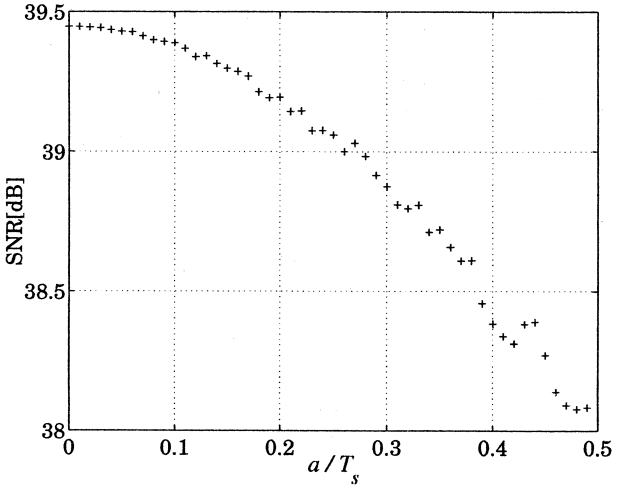

Fig. 18. Simulation result of SNR versus the jitter a/T_s of a 10-bit DAC with jitter of cosine squared distribution (Fig. 11) for $f_{in}/f_s = 3/512$. Here the total noise power outside as well as inside the signal band is considered.

jitter; Fig. 19 shows that as the input frequency f_{in} increases for a given jitter, SNR gets worse while Fig. 20 shows that as the jitter increases for a given input frequency f_{in}, SNR degrades significantly. These results can be interpreted as follows: the noise power due to the zero-hold output and the jitter has the peaks at $kf_s \pm f_{in}$ ($k = 1, 2, 3, \ldots$) (which is higher than $f_s/2$ for all k) and if we consider the whole noise outside as well as inside the signal band $f_s/2$, the dominant noises are located at these fre-

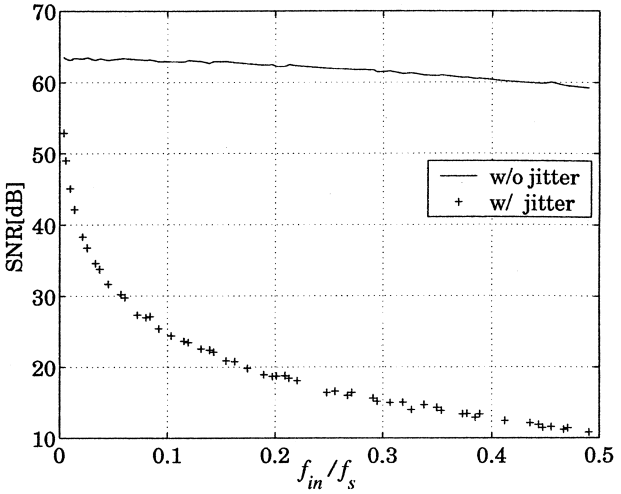

Fig. 19. Simulation result of SNR versus f_{in}/f_s of a 10-bit DAC with and without jitter of cosine squared distribution of $a = T_s/4$ (Fig. 11). Here only the noise power inside the signal band $f_s/2$ is considered.

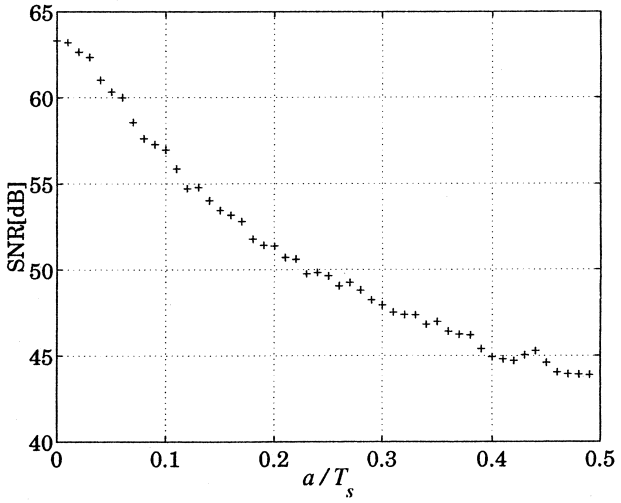

Fig. 20. Simulation result of SNR versus the jitter a/T of a 10-bit DAC with jitter of cosine squared distribution (Fig. 11) for $f_{in}/f_s = 3/512$. Here only the noise power inside the signal band $f_s/2$ is considered.

quencies. The sampling clock jitter induces *the spread spectrum effects* for the peak frequency noises (as well as the signal power) and the power at these frequencies is widely spread to other frequencies, and hence the noise floor increases. However, the total noise power remains almost constant. Hence when the total noise power is considered, the SNR of the DAC is almost constant regardless of the sampling jitter. On the other hand, when only the noise inside the signal band $f_s/2$ is taken into account, the

SNR degrades significantly due to the sampling jitter because the noise floor inside the signal band is raised by the jitter (in this case the noise peaks at $kf_s \pm f_{in}$ are out of signal band and we do not have to consider them).

6. Conclusion

We have described sampling clock jitter effects in DACs. A formula for the output error power due to sampling clock jitter is derived and its spectrum characteristics is shown. Also we have investigated its effects on SNR by numerical simulation and found the following:

(i) When the total noise power outside as well as inside the signal band is taken into account, the DAC SNR remains almost constant regardless of the sampling jitter.

(ii) However, when an analog lowpass filter follows the DAC and only the noise power inside the signal band is considered, the DAC SNR degrades as the jitter increases and the input signal frequency becomes higher. Thus the sampling clock jitter is serious for the high speed DAC.

As another DAC timing non-ideality issue, we are currently investigating the characterization of the glitches which are caused by the timing skew inside the DAC [2,3] and this result will be reported elsewhere.

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Appendix A

This Appendix gives proof of Proposition in Section 2. Look at Fig. 4, and in case $\epsilon_n \leq 0$,

$$\begin{aligned} e_n &= V_{in}(n-1) - V_{in}(n) \\ &= A\cos\left(2\pi \frac{f_{in}}{f_s}(n-1)\right) - A\cos\left(2\pi \frac{f_{in}}{f_s} n\right) \\ &= 2A\sin\left(\pi \frac{f_{in}}{f_s}\right)\sin\left(2\pi \frac{f_{in}}{f_s}\left(n-\frac{1}{2}\right)\right). \end{aligned}$$

In case $\epsilon_n > 0$,

$$e_n = V_{in}(n) - V_{in}(n-1).$$

In both cases,

$$\begin{aligned} e_n^2 &= [V_{in}(n) - V_{in}(n-1)]^2 \\ &= 4A^2\sin^2\left(\pi \frac{f_{in}}{f_s}\right)\sin^2\left(2\pi \frac{f_{in}}{f_s}\left(n-\frac{1}{2}\right)\right) \\ &= 2A^2\sin^2\left(\pi \frac{f_{in}}{f_s}\right)\left[1 - \cos\left(4\pi \frac{f_{in}}{f_s}\left(n-\frac{1}{2}\right)\right)\right]. \end{aligned}$$

Since

$$E\left[\cos\left(4\pi \frac{f_{in}}{f_s}\left(n-\frac{1}{2}\right)\right)\right] = 0,$$

we obtain

$$E[e_n^2] = 2A^2\sin^2\left(\pi \frac{f_{in}}{f_s}\right). \tag{A.1}$$

Then it follows from Eqs. (3) and (A.1) that

$$P_e = 2A^2\sin^2\left(\pi \frac{f_{in}}{f_s}\right)E[|\epsilon_n|],$$

and thus the proposition is proved. (Q.E.D.)

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Naoki KUROSAWA received the B.S. degree in electronic engineering from Gunma University, Japan in 2000, and currently he is an M.S. course student there. His research interests include analog integrated circuit design.

Haruo KOBOYASHI received the B.S. and M.S. degrees in information physics from University of Tokyo in 1980 and 1982 respectively, the M.S. degree in electrical engineering from University of California, Los Angeles (UCLA) in 1989, and the Dr. Eng. degree in electrical engineering from Waseda University in 1995. In 1982, he joined Yokogawa Electric Corp. Tokyo, Japan, where he was engaged in the research and development related to measuring instruments and a mini-supercomputer. From 1994 to 1997 he was involved in the research and development of ultra-high-speed ADCs and DACs at Teratec Corporation. He was also an adjunct lecturer at Waseda University from 1994 to 1997. In 1997 he joined Gunma University and presently is an Associate Professor in Electronic Engineering Department there. Dr. Kobayashi received the 1994 Best Paper Award from the Japanese Neural Network Society, and he is a member of the IEEE.

Hideyuki KOGURE received the B.S. degree in electronic engineering from Gunma University, Japan in 2000, and currently he is an M.S. course student there. His research interests include analog integrated circuit design.

Takanori KOMURO received his BSEE degree in electronic engineering from the University of Tokyo, and joined Yokogawa Electronic Works in 1985. He had developed AD converter for measurement instruments. From 1991 to 1995, he had joined a consortium called Superconductive Sensor Laboratory, at which he took part to develop electronic portion of MEG system. In 1995 he joined Kanazawa Institute of Technology as researcher. Then he had developed SQUID system. In 1997, he joined Agilent Technologies Japan Ltd. And he is now developing measuring sub-system for LSI tester. He is a member of the IEEE.

Hiroshi SAKAYORI received his BSEE degree in electronic engineering from Waseda University, and joined Agilent Technologies Japan Ltd. (former Hewlett-Packard Japan Ltd.) in 1972. He has developed LCR meters and related products, and semiconductor parameter analyzer. From 1992 to 1997, he has temporarily left Agilent Technologies and has joined a consortium called Teratec, at which he took part to develop high speed data conversion technology. He is now responsible for developing measuring sub-system for mixed-signal LSI tester. He is a member of the Institute of Electrical Engineers of Japan.