Dynamics of Parallel-Type and Serial-Type Charge Pump Circuits for High Voltage Generation

Kenji KASHIWASE, Haruo KOBAYASHI, Nobuyuki KUROIWA, Naoto HAYASAKA,
Shinya INABA, Takao MYONO †, Tatsuya SUZUKI, † Takashi IIJIMA †, and Shuhei KAWAI †
Dept. of Electronic Engineering, Gunma University, 1-5-1 Tenjin-cho Kiryu 376-8515 Japan
phone: 81-277-30-1788 fax: 81-277-30-1707 e-mail: k_haruo@el.gunma-u.ac.jp
† Sanyo Electric Corp. 1-1-1 Sakata Oizumi-Machi Ora-Gun Gunma 370-0596 Japan.

Abstract – This paper describes the dynamics of Dickson-type (parallel-type) charge pump circuits as well as serial-type (switched-capacitor-type) charge pump circuits for high voltage generation. We derive several formulas for their energy dissipation, node voltage, and efficiency which may be useful for their design and analysis.

Keywords: Charge Pump, High Voltage Generator, Power Supply Circuit, Efficiency

I. Introduction

Recently video products such as digital video cameras, digital still cameras (DSC), and DSC phones incorporate charge coupled devices (CCDs) for video image acquisition, and in order to drive CCDs it is necessary to generate high voltages such as +12V (at output current of several mA) and − 6.5V (at several mA) from a Vdd=5V supply. At present, switching regulators are widely used for such applications because they can generate high voltages with excellent power efficiency. However, they generate harmonic noise during switching, and also require bulky, costly, off-chip coils. Charge-pump circuits, on the other hand, have the advantage of low noise, and do not require coils. Hence recently much attention has been paid to charge pump circuits which can provide large output current with relatively high efficiency to realize miniature, low-cost mobile equipment [1, 2]. There are two types of charge pump circuits; parallel-type (Dickson-type) and serial-type (switched-capacitor type). In this paper we analyze both types of charge pump circuits, and derive several formulas of their dynamics and efficiency which show quantitatively that parallel-type one provides better efficiency and higher output voltage (lower voltage loss) for certain parasitic capacitances and output current load.

II. Parallel-type Charge Pump Circuit

2.1 Operation of Dickson Charge Pump Circuit

Dickson-type (or parallel-type) charge pump circuits generate higher output voltages than the regular supply voltage [1, 2, 3, 4, 5, 6], and Fig.1 shows a three-stage Dickson charge pump circuit. Drain-gate connected NMOS FETs (MD1 - MD4) are used as diodes here, so charge can be pumped in only one direction. CLK and $\overline{CLK}$ are two out-of-phase pumping clocks, and C_1 - C_4 are coupling capacitors with the same capacitance C. The two clocks pump the charge upward through the MOSFETs (and hence increase the node voltage). When CLK goes from high to low and $\overline{CLK}$ from low to high, the voltage at node 1 settles at $V_1 + \Delta V$, and the voltage at node 2 to V_2, where V_1 and V_2 are defined as the steady-state lower voltage at nodes 1 and 2 respectively. Both MD1 and MD3 are reverse biased, charge is pumped from node 1 to node 2 through MD2, and the final voltage difference between nodes 1 and 2 is the threshold voltage of MD2.

2.2 Energy Dissipation of Dickson Charge Pump Circuit at Start-Up

This subsection shows that in an ideal three-stage charge pump circuit (Fig.2), one half of the energy E_{Supply} supplied from V_{dd} and clock drivers from $t = 0$ to ∞ is stored in the capacitors C at $t = \infty$, and the other half is dissipated through the switches from $t = 0$ to ∞.

The following example helps us to understand the energy dissipation in a circuit which consists of capacitors and switches:

Example : Suppose that we charge a capacitor C in the RC circuit of Fig.3, and the initial voltage across the capacitor is zero at $t = 0$. The differential equation and solution for $V_{out}(t)$ for $t \geq 0$ are given by

$$RC\frac{d}{dt}V_{out}(t) + V_{out}(t) = V_{dd}, \quad V_{out}(0) = 0,$$

$$V_{out}(t) = V_{dd}(1 - \exp(-\frac{t}{RC})).$$

The energy E_{Supply} supplied from V_{dd} for $t = 0$ to ∞ is given by $E_{Supply} = CV_{dd}^2$ because the charge CV_{dd} flows from V_{dd}. The energy stored in C at the steady state ($t = \infty$) is given by $E_C = \frac{1}{2}CV_{dd}^2$. Also the energy E_R dissipated in R from $t = 0$ to ∞ is obtained by

$$E_R = \frac{1}{R}\int_0^\infty (V_{dd} - V_{out}(t))^2 = \frac{1}{2}CV_{dd}^2.$$

Thus we have the following relationships:

$$E_{Supply} = E_C + E_R, \qquad E_C = E_R.$$

One half of the energy supplied from V_{dd} is stored in C and the other half is dissipated in R.

Now we consider the ideal three-stage charge pump circuit in Fig.2.

Proposition 1 : When the charges in all the capacitors are zero at $t = 0$ in Fig.2, we have the following:

$$E_{Supply} = E_C + E_R, \qquad E_C = E_R. \tag{1}$$

Here E_{Supply} is the energy supplied from V_{dd} and clock drivers for $t = 0$ to ∞, E_C is the energy stored in all the capacitors C at the steady state ($t = \infty$) and E_R is the energy dissipated in the resistance of the switches for $t = 0$ to ∞.

Proof : See Appendix 1.

2.3 Node Voltage of Dickson Charge Pump Circuit in Transient State

In this subsection we derive a formula for the node voltage in the transient state as well as the steady state of a three-stage charge pump circuit which includes the following circuit nonidealities (Fig.4).

(i) Voltage drop V_d across switch : Consider the case that the switch is realized with a diode or a diode-connected MOSFET and it has some voltage drop V_d when it is ON.

(ii) Parasitic capacitance C_p at each node : Consider the case that each node has parasitic capacitance C_p to ground.

(iii) Output current I_{out} : Consider the case that the output node provides a load current I_{out}.

Proposition 2 : In a three-stage charge pump circuit in Fig.4, the output voltage node $V_{out}(n)$ and the internal node voltage $V_1(n)$ at n-th clock cycle are given by

$$\mathbf{v}(n) = L \cdot \mathbf{v}(0) + M \cdot \mathbf{b} \cdot V_{dd}, \tag{2}$$

where

$$\mathbf{v}(n) := \begin{bmatrix} V_1(n) \\ V_{out}(n) \end{bmatrix},$$

$$L := \begin{bmatrix} (\lambda_1^n + \lambda_2^n)/2 & (\lambda_1^n - \lambda_2^n)/(2\sqrt{2}) \\ (\lambda_1^n - \lambda_2^n)/\sqrt{2} & (\lambda_1^n + \lambda_2^n)/2 \end{bmatrix},$$

$$M := \begin{bmatrix} 2 - \lambda_1^{n+1} - \lambda_2^{n+1} & 2 - 4\lambda_1^{n+1} + 4\lambda_2^{n+1} \\ 4 - 8\lambda_1^{n+1} - 8\lambda_2^{n+1} & 4 - 4\lambda_1^{n+1} - 4\lambda_2^{n+1} \end{bmatrix},$$

$$\mathbf{b} := \begin{bmatrix} 1/4 + (1-x)/[4(1+\alpha)] \\ -\beta + (1-3x)/[2(1+\alpha)] \end{bmatrix}, \tag{3}$$

$$\lambda_1 = \frac{2+\sqrt{2}}{4}, \qquad \lambda_2 = \frac{2-\sqrt{2}}{4}, \tag{4}$$

$$x := \frac{TI_{out}}{CV_{dd}}, \qquad \alpha := \frac{C_p}{C}, \qquad \beta := \frac{V_d}{V_{dd}}. \tag{5}$$

Proof : See Appendix 2.

Remark (i) Since $|\lambda_1| < 1$ and $|\lambda_2| < 1$,

$$\text{as } n \to \infty, \quad \lambda_1^n \to 0, \quad \lambda_2^n \to 0,$$

$$V_1(n) \to \left(2 - \frac{3}{2}\frac{C_p}{C + C_p}\right)V_{dd} - 2V_d - \frac{7}{2}\frac{TI_{out}}{C + C_p}$$

$$V_{out}(n) \to \left(4 - 3\frac{C_p}{C + C_p}\right)V_{dd} - 4V_d - 7\frac{TI_{out}}{C + C_p}.$$

(ii) The proof of Proposition 2 in Appendix 2 uses a so-called state-space approach. With this approach we can derive output node and internal node voltages at the n-th cycle in an N-stage charge pump circuit for any positive integer N.

2.4 Efficiency of Dickson Charge Pump Circuit in Steady State

In this subsection we describe several formulas regarding to the efficiency of the Dickson charge pump circuit.

Proposition 3 : (i) Efficiency η_p of an N-stage Dickson charge pump circuit (which has the circuit nonidealities V_d, C_p and the output current I_{out} in Fig.4) at the steady state is given by

$$\eta_p := \frac{\text{Output Power from } V_{out}}{\text{Supplied Power from } V_{dd} \text{ and Clock Drivers}}$$

$$= 1 - \frac{N\alpha + 2(N+1)(1+\alpha)\beta x + 4Nx^2}{N\alpha + 2\gamma x} \tag{6}$$

where x, α, β and γ have no dimension, and are defined by eq.(5) and $\gamma := N + 1 + \alpha$.

(ii) Efficiency η_p has a maximum value of η_{pmax} at $x = x_{popt}$, where

$$\eta_{pmax} := 1 - \frac{2N\lambda + \beta\gamma(\gamma + N\alpha) - 2N^2\alpha}{\gamma^2} \tag{7}$$

$$\lambda := \sqrt{N^2\alpha^2 - \alpha\gamma[\beta(\gamma + N\alpha) - \gamma]}$$

$$x_{popt} := \frac{-N\alpha + \sqrt{N^2\alpha^2 + [(1-\beta)\gamma - N\alpha\beta]\gamma\alpha}}{2\gamma}. \tag{8}$$

Proof : See Appendix 3.

Fig.5 shows η_p versus x - calculated from eq.(6) - for $N = 3$ and several values of α, β, and we see that η has a peak value for given N, α and β. Fig.6 shows measurement results for our charge pump circuit [1] and we see that its efficiency has a peak as the output current I_{out} changes; comparing Figs.5 and 6, we see that Proposition 3 can explain the measurement results.

III. Serial-Type Charge Pump Circuit

Let us consider a switched-capacitor-type (serial-type) charge pump circuit [4] which consist of N capacitors $C_1, C_2, ..C_N$ and switches, and Fig.7 shows $N = 4$ case. As shown in Fig.7 (a), one terminal of each capacitor is connected to GND while the other terminal is connected to V_{dd}, and then $C_1, C_2, ..., C_N$ store the charge of $C_1V_{dd}, C_2V_{dd}, ...C_NV_{dd}$ respectively. Then each capacitor is connected in series (Fig.7 (b)) and the output voltage V_{out} is ideally NV_{dd} (N times higher than the supply voltage V_{dd}). However in actual circuits there are parasitic capacitors C_p associated with each node, and also the output voltage provides load current $2I_{out}$, and in this case, the output voltage is lower than NV_{dd}.

Proposition 4 In the switched-capacitor circuits in Fig.7 (b), each node voltage is given as follows:

$$V_{out} = \frac{V_{dd}}{D}\Big[\left(4 + 20\alpha + 21\alpha^2 + 8\alpha^3 + \alpha^4\right) - x\left(4 + 10\alpha + 6\alpha^2 + \alpha^3\right)\Big],$$

$$V_3 = \frac{V_{dd}}{D}\Big[\left(3 + 13\alpha + 16\alpha^2 + 7\alpha^3 + \alpha^4\right) - x\left(3 + 4\alpha + \alpha^2\right)\Big],$$

$$V_2 = \frac{V_{dd}}{D}\Big[\left(2 + 8\alpha + 14\alpha^2 + 7\alpha^3 + \alpha^4\right) - x\left(2 + \alpha\right)\Big],$$

$$V_1 = \frac{V_{dd}}{D}\Big[\left(1 + 4\alpha + 10\alpha^2 + 6\alpha^3 + \alpha^4\right) - x\Big].$$

where α and x are defined in eqs.(5), and

$$C := C_1 = C_2 = ... = C_{N-1} = C_N,$$
$$D := 1 + 10\alpha + 15\alpha^2 + 7\alpha^3 + \alpha^4.$$

Proof See Appendix 4.

Proposition 5 (i) Efficiency η_s of the switched-capacitor-type charge pump circuit in Fig.7 is given by

$$\eta_s = \frac{Fx - (Hx^2/2)}{G + 2Fx}, \tag{9}$$

where

$$F := 4 + 20\alpha + 21\alpha^2 + 8\alpha^3 + \alpha^4,$$

$$G := 14\alpha + 34\alpha^2 + 19\alpha^3 + 3\alpha^4,\ H := 4 + 10\alpha + 6\alpha^2 + \alpha^3.$$

(ii) Efficiency η_s has a maximum value at $x = x_{sopt}$, where

$$x_{sopt} := \frac{G}{F}\left(-1 + \sqrt{1 + \frac{2F^2}{GH}}\right). \tag{10}$$

Proof See Appendix 5.

IV. Comparison of Parallel-Type and Serial-Type Charge Pump Circuits

Let us compare the output voltage and efficiency of parallel-type and serial-type charge pump circuits in Figs.2 and 7 using the derived formulas in the previous sections. Fig. 8 shows their output voltages with respect to x for several values of α with $\beta = 0$, and we see that the parallel-type charge pump circuit provides higher output voltage. Fig.8 shows their output voltages with respect to x for several values of α with $\beta = 0$, and we see that the maximum achievable efficiency of the parallel-type charge pump circuit for a given α is higher than that of the serial-type one. These can be explained as follows; one terminal of parasitic capacitance C_p is connected to the corresponding node (while the other is connected to GND), and in the parallel-type charge pump circuit, the node voltage associated with parasitic capacitance C_p changes only by V_{dd} between clk =high and clk =low states. On the other hand, in the serial-type charge pump circuit, some node voltages associated with parasitic capacitance C_p change by more than V_{dd} between clk =high and clk =low states, which cause voltage loss as well as efficiency loss. But note that the break-down voltage of capacitors C in parallel-type one should be higher than that in serial-type one.

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Appendix 1 (Proof of Proposition 1)

In Fig.2, using the charge conservation law for each cycle, the energy loss $E_{loss}(n)$ and the energy stored in all capacitors $E_c(n)$ at n-th cycle are given by

$$E_{loss}(n) = \frac{C}{16}\Bigg[10V_1(n)^2 + 5V_{out}(n)^2 + 74V_{dd}^2 - 8V_1(n)V_{out}(n) - 16V_{out}(n)V_{dd} - 28V_1(n)V_{dd}\Bigg],$$

$$E_c(n) = \frac{C}{2}\Bigg[2V_1(n)^2 + 2V_{dd}(n)^2 - 2V_1(n)V_{dd} + V_{out}(n)^2\Bigg],$$

where

$$V_{out}(n) = \frac{1}{2}(\lambda_1^n + \lambda_2^n)V_{out}(0) + \frac{1}{\sqrt{2}}(\lambda_1^n - \lambda_2^n)V_1(0) + \left[-(2+\frac{3}{\sqrt{2}})\lambda_1^n - (-2+\frac{3}{\sqrt{2}})\lambda_2^n + 4\right]V_{dd},$$

$$V_1(n) = \frac{1}{\sqrt{2}}(\lambda_1^n - \lambda_2^n)V_{out}(0)\frac{1}{2}(\lambda_1^n + \lambda_2^n)V_1(0) + + \left[-(2+\frac{3}{\sqrt{2}})\lambda_1^n - (2-\frac{3}{\sqrt{2}})\lambda_2^n + 3\right]V_{dd},$$

and λ_1, λ_2 are defined by eq.(4). Then considering an initial condition E_{loss0},

$$E_R := \sum_{n=0}^{\infty} E_{loss}(n) + E_{loss0} = 15CV_{dd}^2,$$

$$E_c := \lim_{n\to\infty} E_c(n) = 15CV_{dd}^2,$$

and eq.(1) is obtained.

Appendix 2 (Proof of Proposition 2)

Using the charge conservation law, we have the following state equation for Fig.4:

$$\mathbf{v}(n+1) = A\mathbf{v}(n) + \mathbf{b}V_{dd}$$

where

$$\mathbf{v}(n) := \begin{bmatrix} V_1(n) \\ V_{out}(n) \end{bmatrix}, \quad A := \begin{bmatrix} \frac{1}{2} & \frac{1}{4} \\ \frac{1}{2} & \frac{1}{2} \end{bmatrix},$$

and $\mathbf{b}$ is defined by eq.(3). Then we have the following

$$\mathbf{v}(n) = A^n\mathbf{v}(0) + \sum_{k=0}^{n-1} A^k\mathbf{b}V_{dd}.$$

Note that λ_1 and λ_2 defined by eq.(4) are eigenvalues of A, and then we obtain eq.(2).

Appendix 3 (Proof of Proposition 3)

Consider the steady state (i.e., $n \to \infty$) in Fig.4. Then the energy E_{load} supplied from the output node during one clock cycle T is given by

$$E_{load} = \left[2V_{dd} - 8V_d + 6\frac{C}{C+C_p}V_{dd} - 12\frac{TI_{out}}{C+C_p}\right]TI_{out}.$$

Also the energy $E_{supply}(\infty)$ supplied from V_{dd} and clock drivers during one clock cycle T is given by

$$E_{supply}(\infty) = 3CV_{dd}^2 - 3\frac{C^2}{C+C_p}V_{dd}^2 + 6\frac{C}{C+C_p}V_{dd}TI_{out} + 2V_{dd}TI_{out}.$$

Since $\eta_p = E_{load}/E_{supply}(\infty)$, eq.(6) has been obtained. Also byy calculating $\partial\eta_p/\partial x = 0$ and $x > 0$, we obtain eq.(8). Also putting x_{popt} in eq.(8) to eq.(6), we obtain eq.(7).

Appendix 4 (Proof of Proposition 4)

According to the charge conservation law at each node in Fig.7, we have the followings:

$$C_1V_{dd} + C_{p1}V_{dd} - C_2V_{dd} = C_1V_1 + C_{p1}V_1 - C_2(V_2 - V_1),$$

$$C_2V_{dd} + C_{p2}V_{dd} - C_3V_{dd} = C_2(V_2 - V_1) + C_{p2}V_2 - C_3(V_3 - V_2),$$

$$C_3V_{dd} + C_{p3}V_{dd} - C_4V_{dd} = C_3(V_3 - V_2) + C_{p3}V_3 - C_4(V_{out} - V_3),$$

$$C_4V_{dd} + C_{p4}V_{dd} = C_4(V_{out} - V_3) + C_{p4}V_{out} + TI_{out}.$$

By solving the above equations, we have V_1, V_2, V_3 and V_{out} given in Proposition 5.

Appendix 5 (Proof of Proposition 5)

In Fig.7 (b), the energy E_{load} supplied from the circuit to the output load during $T/2$ is given by

$$E_{load} = \frac{CV_{dd}^2}{2D}(2Fx - Hx^2).$$

In Fig.7 (a), the energy E_{supply} from V_{dd} to the circuit during $T/2$ is given by

$$E_{supply} = \frac{CV_{dd}^2}{D}(G + Fx).$$

Then the efficiency η_s is given by $\eta_s = E_{load}/E_{supply}$ and eq.(9) is obtained. Also from $\partial\eta_s/\partial x = 0$, we obtain eq.(10).

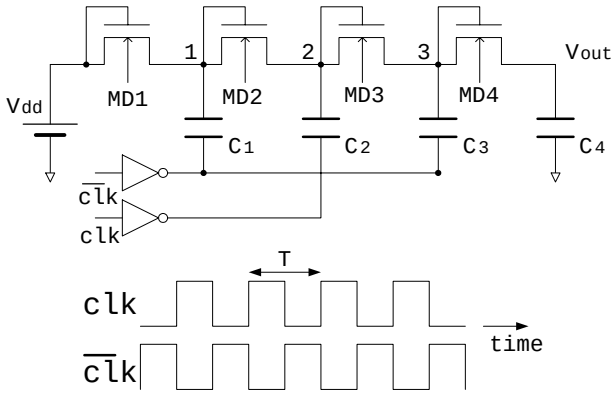

Fig.1: A three-stage Dickson charge pump in CMOS IC.

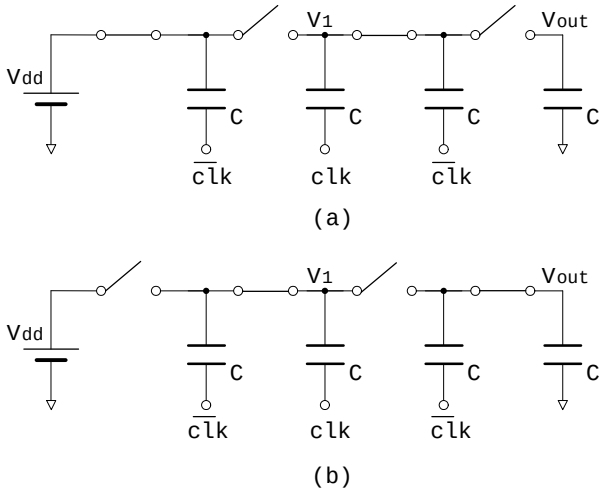

Fig.2: An ideal three-stage Dickson charge pump circuit. (a) $clk = 0, \overline{clk} = V_{dd}$. (b) $clk = V_{dd}, \overline{clk} = 0$.

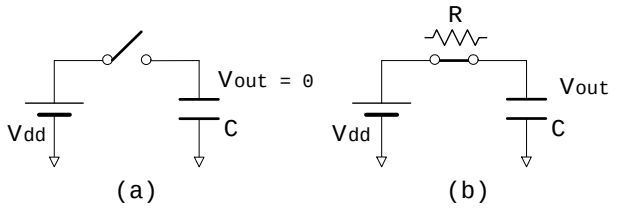

Fig.3: An RC circuit. (a) The switch is OFF and $V_{out}(t) = 0$ during $t < 0$. (b) The switch turns on at $t = 0$, and its on-resistance value is R.

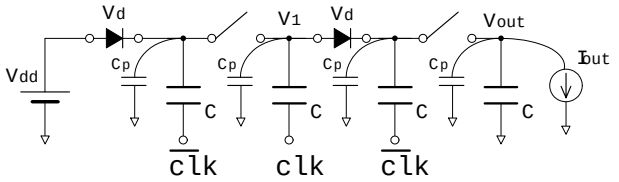

Fig.4: A non-ideal three-stage Dickson charge pump circuit where voltage drop V_d across each switch, parasitic capacitance C_p at each node, and output load current I_{out} are considered.

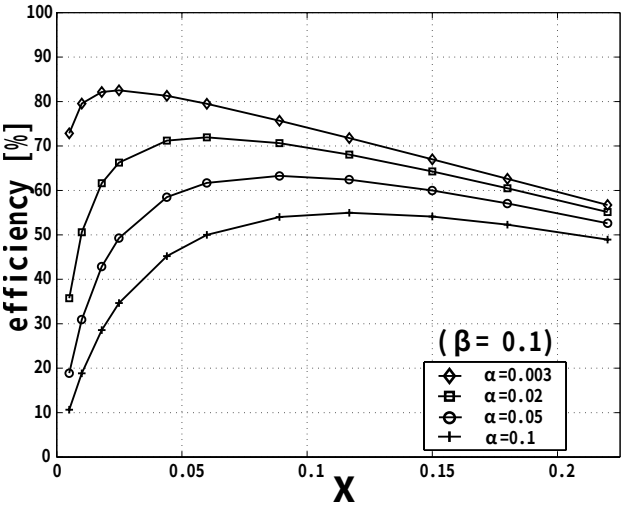

Fig.5: Theoretical efficiency obtained from eq.(6) of Dickson charge pump circuit for $N = 3$, $\alpha = 0.003, 0.02, 0.05, 0.1$ and $\beta = 0.1$ with respect to $x := TI_{out}/(CV_{dd})$.

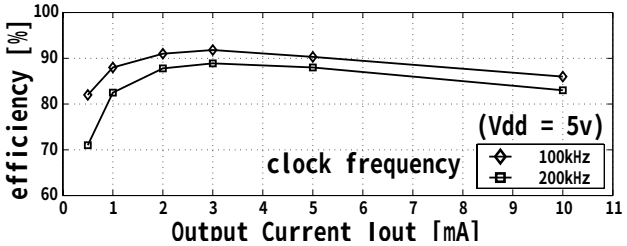

Fig.6: Measured efficiency of our three-stage ($N = 3$) Dickson charge pump circuit [1] with respect to I_{out}.

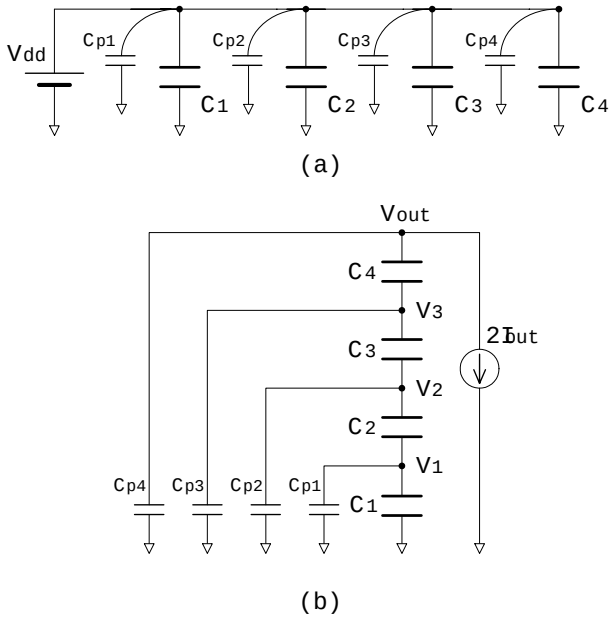

Fig.7: A switched-capacitor charge pump circuit. (a) All capacitors of $C_1, C_2, ..., C_N$ are connected in parallel and charged to V_{dd}. (b) All capacitors are connected in series to produce high output voltage.

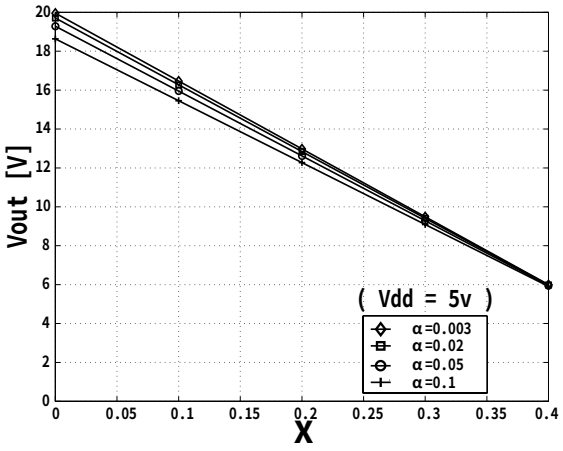

Fig.8 (a): Theoretical output voltage of the Dickson charge pump circuit in Fig.2 for $N = 3$, $\alpha = 0.003, 0.02, 0.05, 0.1$ and $\beta = 0.0$ with respect to $x := TI_{out}/(CV_{dd})$.

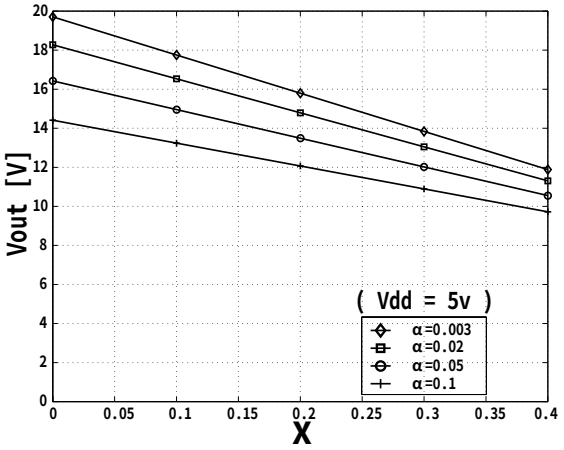

Fig.8 (b): Theoretical output voltage of the switched-capacitor charge pump circuit in Fig.7 for $\alpha = 0.003, 0.02, 0.05, 0.1$ with respect to x.

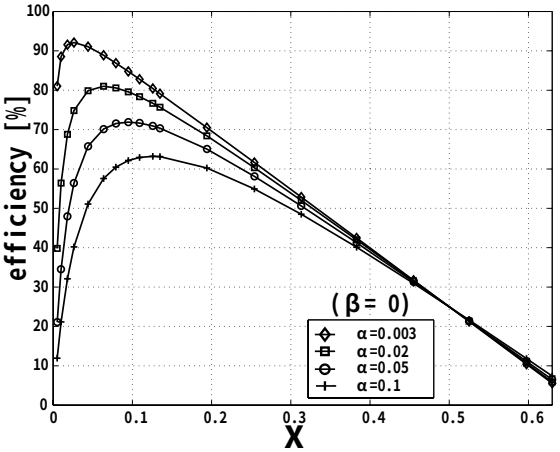

Fig.9 (a): Theoretical efficiency of the Dickson charge pump circuit in Fig.2 obtained from eq.(6) for $N = 3$, $\alpha = 0.003, 0.02, 0.05, 0.1$ and $\beta = 0.0$ with respect to x.

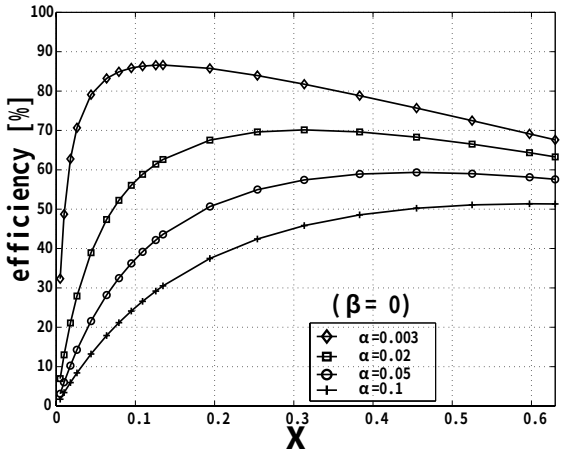

Fig.9 (b): Theoretical efficiency of the switched-capacitor charge pump circuit in Fig.7 obtained from eq.(9) for $\alpha = 0.003, 0.02, 0.05, 0.1$ with respect to x.