



ADC standard and testing in Japanese industry

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Abstract

This paper presents case studies of ADC standards and testing in Japanese industry from the viewpoints of ADC users, an ADC designer and an ADC tester manufacturer. These studies report the opinions of experienced ADC engineers in three Japanese companies (Iwatsu Electric, Agilent Technologies Japan, Sanyo Electric) about standards for ADCs. In most Japanese companies, ADC standards belong to engineers, and there is no comprehensive document that can be used as a *Bible* of ADC standards and testing methods, so ADC standards, which satisfy the requirements of engineers in industry, would be very useful. © 2001 Elsevier Science B.V. All Rights Reserved.

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1. Introduction

This paper presents case studies of ADC standards and testing in Japanese industry from the viewpoints of ADC users, an ADC designer and an ADC tester manufacturer. These studies report the opinions of experienced ADC engineers in three Japanese companies:

- Iwatsu Electric—a user of ADCs (in measuring instruments, especially digital storage oscilloscopes)
- Agilent Technologies Japan (a part of former Hewlett-Packard), LSI tester division—a user and manufacturer of ADCs for LSI and particu-

larly ADC testers (analog-digital-mixed LSI testers)

- Sanyo Electric, semiconductor company—an ADC designer.

In most Japanese companies, ADC standards belong to engineers and there is no comprehensive document that can be used as a *Bible* of ADC standards and testing methods, so ADC standards, which satisfy the requirements of engineers in industry, would be very useful. Opinions and comments of the engineers here may be somewhat biased and do not necessarily represent their companies' opinions; all technical details of recent research into ADC standards and testing in academia may not have reached them yet, but we can learn a lot—about what people in the industry really need in this field—from their comments, and we believe that some of their comments are worth reflecting in ADC stan-

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dards. Design engineers (as distinct from research engineers) generally do not write many technical papers, hence, it is difficult to know what their problems really are—there is a gap between academia and industry. We hope that this article can be a bridge between them in the ADC standards field.

The reader can find descriptions of ADC parameter terminology used here in Refs. [1,2].

2. Iwatsu Electric

Iwatsu is one of the top measuring instrument (especially oscilloscope) manufacturers in Japan, and they use ADCs in their measuring instrument products. Basically, there are no written standards for ADCs used in measuring instruments in Iwatsu, and engineers and their sections are responsible for selecting ADCs for measuring instruments. The following subsections contain the opinions, from the ADC-user viewpoint, of experienced Iwatsu engineers who have been involved in the design of high-speed wideband digital storage oscilloscopes and highly accurate measuring instruments (such as digital multimeters (DMM)) for low-frequency signals.

2.1. ADCs for digital storage oscilloscope

This subsection contains the opinions of Iwatsu engineers about ADCs for high-speed wideband digital storage oscilloscopes.

- Usually, the Track/Hold (T/H) circuit is not tested by itself; it is tested in combination with the ADC which follows it.

- Separate T/H circuit and ADC ICs are often assembled on a board; not so many good monolithic ICs, which include both T/H circuit and ADC, are commercially available.

- The T/H circuit may be omitted when the required band width is smaller than 100 MHz and/or the input capacitance of the ADC is small enough for the preceding amplifier to drive.

- Important specifications of ADCs for oscilloscope applications are the effective number of bits (ENOB), word error rate, overdrive recovery, band width, step response settling time and monotonicity.

- IMD, SFDR, DP and DG are not important in oscilloscope applications.

- Recently, many commercial ADCs have good ENOB even at input frequencies beyond the Nyquist rate. Experience suggests that, for oscilloscope applications, an 8-bit ADC has to have an ENOB of at least 6 bits at high input signal frequencies.

- ENOB is the most important specification of the ADC. When this is not sufficiently large, then linearity and total harmonic distortion (THD), etc. will also be investigated.

- In measuring ENOB, the amplitude of the sinusoidal input signal with respect to full scale needs to be specified; different manufacturers (such as HP, Tektronix) use different amplitudes. An amplitude of 70–80% of full scale seems appropriate.

- When measuring ENOB of a stand-alone ADC, the FFT method with coherent sampling is effective.

- However, when the ADC is embedded in an oscilloscope, the clock inside the oscilloscope has to be used as the sampling clock of the ADC, which results in incoherent sampling. Hence, in this case, a sine curve fitting method is usually used to obtain ENOB; if the FFT method is used, windows have to be used.

- The sine curve fitting method often has problems when the input frequency is near the Nyquist rate.

- Word error rate is important specification for oscilloscope applications; this is because newer oscilloscopes often have long memory (more than 1 M words) and also have wave storage functions.

- Word error rate should be less than 10^{-9} , but word error rate is reduced when the ADC is preceded by a T/H circuit. It is not easy to configure a test system.

- An overdrive recovery test is always performed, input is overdriven and recovery time is measured; also, it is checked whether overdrive causes any failure.

- Offset, gain and drift of the ADC have to be measured.

- Interleaved ADC architectures are important for high-speed oscilloscopes; there is a need for standards related to interleaved architecture, and for research into algorithms which compensate for channel mismatches in interleaved ADCs.

- For measuring instrument applications, operation may be stopped for calibration, however, stoppage is not permitted in communication, video and disk-drive applications.

- Some commercial ADCs generate fairly large aperture jitter inside the ADC chip, and so are not acceptable in oscilloscope applications.

- ADCs with *differential* input are very useful for oscilloscope applications; however, there are not so many commercial ADCs with differential input, except for some ADCs from Maxim (Tektronix).

- The ADC should be considered in conjunction with the amplifier that drives it. One commercial 1 GS/s 8-bit ADC has an input capacitance of 10 pF, but the preceding amplifier cannot drive such a large capacitive load at high frequencies. For example, “input capacitance of 20 pF, and 2-V full scale” is not an acceptable specification for a high-speed ADC.

- In many cases, the input capacitance of the ADC is nonlinear; its step responses may be different for rising and falling step inputs. There need to be standards for specifying nonlinear voltage-dependent input capacitance.

- The testing of the complete ADC system, which includes T/H circuits, ADCs, amplifiers and time-base circuit, is as important as the testing of the stand-alone ADC.

- When an ADC with better than 8-bit resolution is tested, the sinusoidal input is applied from a signal generator through an *analog bandpass filter* to reject harmonic distortion components of the sinusoidal signal.

- ADC manufacturers often specify the full-scale input of their ADCs as being ≈ 2 V (allowing for V_{be} variations in the bipolar transistor). However, for most oscilloscope applications, a full-scale input of ≈ 1 V is sufficient.

- It would be useful if a figure of merit relating the full-scale input, input capacitance, and sampling speed of an ADC (comparable to the gain-bandwidth product of an amplifier) were derived.

- For oscilloscopes, ADCs are intensively tested and then selected during the design stage, but in the manufacturing stage, high-speed ADC testing may be omitted because it is not practical to use an IC socket on the board. (An IC socket significantly degrades ADC AC performance.)

2.2. ADC for highly accurate measuring instrument

This subsection provides a collection of comments from Iwatsu engineers about ADCs for highly

accurate (better than 16-bit) measuring instruments for low frequency signals.

- Delta-sigma ADCs are replacing dual-slope (or triple-slope) integration ADCs in DMMs.

- For DC signal measurement applications, digital filters of delta-sigma ADCs must have zeros at 50 and/or 60 Hz to improve NMR and CMR.

- For DMM applications, delta-sigma ADCs have to have auto-calibration and drift-compensation functions.

- When the voltage resolution of the delta-sigma ADCs is better than $1 \mu\text{V}$, special care is required to test them accurately; pure copper traces are used on their test boards (evaluation boards) to reduce thermal voltages, and low-noise operational amplifiers and resistors also have to be used. Furthermore, when testing them, the environment temperature has to be controlled within $22\text{--}24^\circ$. When voltage resolution is worse than $1 \mu\text{V}$, on the other hand, the testing requirements are considerably relaxed.

- Leakage currents at the ADC input (e.g., due to base current of BJT, protection diode) are often troublesome.

- The output of the delta-sigma ADC should be stable, i.e., the least-significant digit of the DMM should not fluctuate, at a given DC input.

- When the linearity is required to be better than 18 bit, the linearity of the delta-sigma ADC is measured using a DC input from a standard voltage generator traceable to national standards.

2.3. Other comments

This subsection contains further comments about ADCs as well as DACs.

- Usually an ADC for communication applications is embedded in the system and in such a case, the testing of the ADC alone is difficult.

- Research into an ADC model, which can predict performance (such as word error rate and effective number of bits) without time-consuming circuit simulation (such as SPICE), would be very useful.

- For measuring instrument applications, DACs are mainly used for arbitrary waveform generators (AWG), and here, the settling time of the DAC is the important specification; we have to avoid including the settling time of the following amplifier when we measure the settling time of the DAC.

- In the design of the arbitrary waveform generator, a direct digital synthesizer is often more difficult to design than a DAC.

- A DAC has a smaller number of specification parameters than an ADC and the effects of some nonidealities of the DAC can be reduced by following it with an analog filter.

3. Agilent Technologies Japan

Agilent Technologies (a part of former Hewlett-Packard) is well-known as the largest measuring instrument company in the world and is famous for their very advanced technology. This section describes the opinions of Agilent Technologies Japan engineers who have been involved in development of analog-digital-mixed LSI testers. They have two standpoints: one is an ADC user for LSI testers and the other is an ADC tester (analog-digital-mixed LSI tester) manufacturer. Currently, Agilent Technologies Japan is involved in HP94000 series and HP9490 series as analog-digital-mixed LSI testers. These series consist of individual products, which have varieties of the number of digital channels and the maximum operating clock frequency. (For example, HP94000 model 266 has 256 digital channels with the maximum clock frequency of 266 MHz.) Analog modules are common for all series and can be configured according to DUTs. (For example, 1-MHz AWGs and 1 MS/s 16-bit digitizers may be used for DUTs for audio applications.)

3.1. ADCs for LSI testers

This subsection provides comments from the viewpoint of an ADC user for LSI testers. There is no written standard of ADC to adopt in their LSI testers in Agilent Technologies Japan. Engineers are assigned for design of certain functional blocks and they select electrical parts to satisfy the specifications of the blocks. Then their design is reviewed and their sections check and approve it if it is proper. Thus, design engineers select ADCs for LSI testers and their sections approve them. Generally speaking, the throughput and the cost for measurement are

more focused on, rather than the performance in LSI tester market, compared to the case of so-called “box instruments” (such as oscilloscopes and DMMs) market. Important specifications of ADCs to use for LSI testers are as follows.

- Frequency flatness. This is important for measuring the frequency response of devices under test (DUTs) using an ADC.

- Input impedance. A flash ADC has a large input capacitance and the input capacitor of a CMOS ADC is input-dependent and nonlinear, while the impedance (especially inductance) of the ADC package can be troublesome for high-speed operation.

- Differential input. ADCs with differential input are now being demanded in the commercial market, however, many signal generators, which provide differential signal to test them, are not available.

- Drift. There are two kinds of drifts, i.e., one is due to temperature while the other is due to aging. For measuring instrument applications, drift after calibration (i.e., drift due to temperature) is important.

- Settling time in step response. Settling time is determined by time constant (e.g., electrical RC time constant) and thermal tail, and for high precision delta-sigma ADCs (more than 20 bit), attention should be paid to the thermal tail.

- Intermodulation distortion (IMD). IMD is very important for recent ADSL applications, which require approximately 90 dB of IMD at 1-MHz input. However, its testing method may not be established yet and reliable signal generators for its testing may not be available.

- Noise from digital circuit. In high-speed ADCs, their digital noise may go to their analog part, which degrades their conversion accuracy, and this effect can be measured as SFDR. For example, when the output of a high-speed ADC is stored in slow SRAM using bank-multiplexing, the clock noise for the bank-multiplexing can enter into the signal band of the ADC as spurious components. Note that the effect of this digital noise can depend on pin assignment and ground lines inside the ADC chip, and hence this effect is often considered as one of performance measures of the ADC itself.

- DC characteristics. Some delta-sigma ADCs show that their noise level characteristics can change as time goes on when DC input is applied, and such

delta-sigma ADCs are not good for measuring instrument applications.

•DNL, INL. There are two methods for DNL and INL measurements for DC input.

(1) DC input method. DC input signal to the measured ADC is given by a DAC, which has better accuracy than the ADC, and this method is used to assure the traceability for NIST. Sometimes their drift may be a problem because their measurement time is long.

(2) Usage of ramp-fit method. A ramp signal is applied to the ADC and the ramp-fit method is used. For high-resolution ADC this measurement method is much faster than the DC input method, and here the high-precision ramp signal generation is important.

3.2. ADC testing using LSI tester

This subsection gives opinions from the viewpoint of an ADC tester manufacturer. Required specification for ADC testing using LSI testers of Agilent Technologies depends on customer's demands. However, Agilent Technologies Japan has developed many programs for testing ADCs according to customers' demands, and the programs may be *de-fact standard* for ADC testing in Agilent Technologies Japan. If some of the programs satisfy new customer's demands, they use them, while if any of them does not, they modify or newly develop testing programs. Table 1 shows ADC examples tested with their LSI testers (HP94000, HP9490 series) and the

following are examples of important testing parameters in their experiences.

- DC parameters test: INL, DNL, Gain/offset, monotonicity, miss-code
- Distortion: THD, IMD, MTPR(multi-tone power ratio)
- Noise, spurious: SFDR, SNR
- Dynamic test: Histogram, SNR for sinusoidal input
- PSRR (for telecommunication application)
- DG/DP (for NTSC, PAL, video applications)
- Band width

DC parameters test is performed for almost all ADCs while other tests are performed according to applications and specifications.

3.3. ADC design for testability

LSI tester manufacturers cannot always meet requirements for testing parameters and conditions of DUTs demanded by their customers, and in such a case, they propose other possible measuring methods to customers and sometimes they request customers to modify the LSI design to be suitable for testing. As the LSI becomes so complex, LSI design for testability is very important today, and hence based on ADC testing experiences of Agilent Technologies Japan, one of the authors considers/proposes here ADC design for testability and built-in-test circuit. Ideally, it is desired that the ADC has whole self-calibration and self-check function inside the chip,

Table 1
ADC examples tested with LSI tester (HP94000, HP9490 series)

ADC application	ADC specification
ADC/CODEC for audio	16–24 bit, ≈ 20 kHz BW
CODEC for telephone	8 bit nonlinear, ≈ 4 kHz BW
Modem for telephone line	8 bit, ≈ 4 kHz BW
xDSL (ADSL)	12–14 bit, ≈ 1 MHz BW
ADC for video	8–10 bit, 20 MHz
HDTV (DVB/DTV/ISDB)	≈ 10 bit, ≈ 8 MHz BW on earth, ≈ 34 MHz BW in space
HDD read channel	6–7 bit, ≈ 300 MHz BW
DVD	8–10 bit, ≈ 150 MHz BW
ADC for industrial application	14 bit, ≈ 100 kHz BW
Dual slope integration ADC for measuring instruments	20 bit

however, so far this may not be realistic and the following are proposed, which would be relatively easy to implement, yet, very useful.

- Input full-scale report function. There are many situations where the sinusoidal signal as close as the full scale has to be applied to the ADC such as in case of linearity testing. However, in general, monolithic ADCs have large gain errors and it is difficult to apply the maximum input signal within its dynamic range (input range), and hence it would be very useful if the monolithic ADC outputs the input full scale.

- Linearity self-check function. It is proposed that for linearity self-checking, the ADC should include reference-voltage-generation circuits that are accurate enough for the ADC linearity testing. For example, if a switched capacitor circuit inside the ADC is designed to generate the reference voltage proportional to the clock frequency, this circuit may be able to generate highly accurate reference voltage because the clock frequency can be controlled very finely and accurately, and with this reference circuit the linearity self-calibration may be possible.

4. Sanyo Electric

Sanyo Electric is one of the major consumer electronics companies in Japan and their products are worldwide. They also have semiconductor divisions and they design, fabricate and test ADCs to incorporate in their analog-digital-mixed system LSIs; but note that their main products are not ADC/DAC ICs themselves (not like Analog Devices) and also remark that the testing methods and equipment for the embedded ADCs/DACs are very different from those for stand-alone ADC/DAC ICs. They have no written-standards for ADC testing, and basically they use well-known ADC testing algorithms and methods though different divisions may use different methods. The following subsections describe ADC testing methods and comments (which do not necessarily represent Sanyo's opinions though) given by an experienced engineer who belongs to one of the divisions which develop ADCs.

4.1. General strategy for ADC testing

- In manufacturing stage, they use LSI testers of HP and Advantest for ADC testing to satisfy the

customer's specification. As long as the LSI satisfies the customer's specification, they sometimes simplify the testing of ADCs/DACs embedded in the LSI in order to reduce the testing cost.

- In design stage, they use individual measuring instruments—in addition to the LSI testers—to evaluate the performance of their designed ADCs and they check their almost all parameters specified for stand-alone ADC ICs from ADC-specialized manufacturers.

4.2. High-speed ADC testing

They develop medium-resolution (6–10 bit) high-speed CMOS ADCs for digital demodulators, and in their design stage the following testing is performed; for ADC testing at sampling speeds of lower than 60 MHz, they use LSI testers of HP and Advantest, and hence they use the testing algorithms and methods, which can be performed with the LSI testers, and some of them are shown in Table 2. For dynamic performance measurements, basically the analog input and the sampling clock are synchronized (i.e., coherent sampling is used) and the FFT method is used without windowing. For ADC testing with sampling speed of higher than 60 MHz, individual instruments are combined to configure an ADC test system: a pulse generator for the sampling clock, a signal generator for the analog AC input, a logic analyzer for the digital output data acquisition, and a

Table 2
High-speed ADC testing parameters and algorithms in Sanyo Electric

Testing parameter	Testing algorithm
Statical integral linearity	bias step method
Statical differential linearity	bias step method
Dynamical integral linearity	sine curve fitting method
Dynamical differential linearity	histgram method
THD	FFT method (coherent sampling)
Number of effective bits	FFT method (coherent sampling)
SNDR	FFT method (coherent sampling)
SNR	FFT method (coherent sampling)
Dynamic range	FFT method (coherent sampling)
Suprious free dynamic range	FFT method (coherent sampling)
Monotonicity	bias step method
Miss code	bias step method
Differential phase	FFT method (coherent sampling)
Differential gain	FFT method (coherent sampling)

universal source for the analog DC input. In this case, the analog input and the sampling clock are not synchronized.

4.2.1. Remark

•Static integral nonlinearity (SINL) and static differential nonlinearity (SDNL) measurements are extensively performed in testing high-speed ADCs using the bias step method; binary search is an alternative method of measuring linearity, however, with high-resolution ADCs it may not converge.

4.3. High-precision ADC testing

A high-resolution (20 bit) delta-sigma ADC with more than 96-dB dynamic range is being developed for audio applications, and its THD + N, SNR and dynamic range (DR) are extensively tested using a UPD (Rohde and Schwartz) audio analyzer and a digital audio measurement system (Audio Precision). Table 3 shows some examples of testing parameters performed in design stage. Note that THD + N, SNR and DR are very important parameters for audio application ADCs and their testing is a must, and especially they evaluate THD + N as a function of the input level. Here, THD + N is the characteristic of a delta-sigma ADC for large signal input and SNR is that for zero-level input, while DR is that for small signal input.

4.3.1. Remark

•Definition of dynamic range (DR) in Sanyo. DR is defined as 60 dB + measured SNDR when an input of -60 dBFS is applied (e.g., 0.2 mV_{pp} when the analog input full scale is 2 V_{pp}).

Table 3
High-precision (delta-sigma) ADC testing parameters and algorithms in Sanyo Electric

Testing parameter	Testing algorithm
Gain, offset	
THD	FFT method (incoherent sampling, Blackman–Harris window)
THD + N	FFT method (incoherent sampling, Blackman–Harris window)
SNR	FFT method (incoherent sampling, Blackman–Harris window)
Dynamic range	FFT method (incoherent sampling, Blackman–Harris window)

•Definition of signal-to-noise ratio (SNR) in Sanyo. SNR is defined as the ratio of digital output, corresponding to analog full-scale input, to digital output noise level for zero-level input. In other words, SNR indicates the noise level for zero-level input referred to analog full-scale, hence, SNR is an ADC characteristic for zero-level input (e.g., SNR is degraded by idle noise in the delta-sigma modulator.) A 1-bit ADC has good linearity for small input levels, hence, SNR and DR usually have almost the same values.

•Comments on THD + N of delta-sigma ADC. In many cases, ADC-specialized manufacturers specify THD + N of a delta-sigma ADC as a function of the input signal level (e.g., 0 , -0.5 , -3 dBFS); this is because for a large input signal a delta-sigma modulator may become unstable and hence its performance may degrade. In other words, from the ADC design viewpoint, it is important to design a delta-sigma ADC that does not degrade the performance even if the input level is close to 0 dBFS.

4.4. Standard of Electronic Industries Association of Japan

Sanyo engineers use a kind of ADC testing standard from Electronic Industries Association of Japan as a reference. Unfortunately, this document is written in Japanese but its summary is as follows.

•Reference number: EIAJ ED-5140, title: “Measuring methods of linear ADCs and DACs” (about 40 pages) (established in Dec. 1994).

•Committee members from 15 Japanese electronics companies: Hitachi, Toshiba, NEC, Matsushita, Sony, Fujitsu, Sanyo, Oki, Sharp, Rohm, Yamaha, Seiko Epson, JRC, TI Japan and Mitsubishi.

•Definition of technical terms and measuring methods are described but some of them may be different from the IEEE standards [1,2].

•This standard may not be the Bible for ADC/DAC testing in Japan but several companies use it as one of their references.

5. Conclusion

In most Japanese companies, ADC standards belong to engineers, and which part of an ADC specification is important depends on the application and viewpoint (e.g., ADC user, ADC designer or ADC

tester manufacturer). It would be very useful if there were a comprehensive document, which could be used as a Bible of ADC standards and testing methods, and meet the requirements of such various different applications and viewpoints. There is a gap between academia and industry in the ADC field and we hope that this article can be a bridge between them.

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Kensuke Kobayashi received the BS degree in Electronic Engineering from the University of Tokyo in 1971. In 1971, he joined IWATSU Electric where he was engaged in designing wideband sampling oscilloscopes. Since 1993, he has been developing fast-sampling-rate and wideband data acquisition systems in Teratec.



Hiroshi Sakayori received his BSEE degree in Electronic Engineering from Waseda University and joined Agilent Technologies Japan (former Hewlett-Packard Japan) in 1972. He has developed LCR meters and related products, and semiconductor parameter analyzer. From 1992 to 1997, he has temporarily left Agilent Technologies and has joined a consortium called Teratec, at which he took part to develop high-speed data conversion technology. He is now responsible for developing measuring sub-system for mixed-signal LSI tester. He is a member of the Institute of Electrical Engineers of Japan.



Yasuyuki Kimura received the BE degree in 1982 from Tsukuba University, Ibaraki, Japan. In April 1982, he joined Sanyo Electric where he has been engaged in development of mixed-signal sub-system for usage within his company.