IEICE TRANS. FUNDAMENTALS, VOL.E89–A, NO.4 APRIL 2006

PAPER Special Section on Selected Papers from the 18th Workshop on Circuits and Systems in Karuizawa

High-Speed Continuous-Time Subsampling Bandpass ΔΣ AD Modulator Architecture Employing Radio Frequency DAC

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SUMMARY This paper proposes a continuous-time bandpass ΔΣAD modulator architecture which performs high-accuracy AD conversion of high frequency analog signals and can be used for next-generation radio systems. We use an RF DAC inside the modulator to enable subsampling and also to make the SNDR of the continuous-time modulator insensitive to DAC sampling clock jitter. We have confirmed that this is the case by MATLAB simulation. We have also extended our modulator to multi-bit structures and show that this alleviates excess loop delay problems.

key words: *continuous-time, subsampling, bandpass, ΔΣ modulator, RF DAC, jitter*

1. Introduction

Currently, research into bandpass ΔΣ AD modulators is very active, because they are expected to be capable of performing high-accuracy AD conversion of high-frequency narrowband signals with low power consumption [1]–[9] and so find wide application to wireless LANs and cellular phones. In this paper, we propose using a continuous-time subsampling bandpass ΔΣ AD modulator whose internal DAC is insensitive to clock jitter, for direct AD conversion of RF signals. Such a modulator can eliminate frequency downconversion circuitry, and help realize next-generation digital-rich analog-minimum receiver front-ends (Fig. 1). We will also discuss the DAC circuit implementation, and extension to multibit modulator architectures which reduce excess loop delay problems.

Note that the proposed bandpass ΔΣ AD modulator can perform AD conversion for any input signal with arbitrary modulation if it is within the specified bandwidth and within the input range (which is the same as other ADCs).

2. Discrete-Time vs. Continuous-Time Circuits

So far, most ΔΣAD modulators have been realized with discrete-time (switched-capacitor) circuits because it is relatively easy to realize high accuracy with them (Fig. 2). Currently there is active research into continuous-time circuit implementations, to obtain higher-speed operation with lower power. However in continuous-time modulators, clock jitter effects on the internal DAC degrade the accuracy of the whole modulator, although jitter effects on the internal ADC are noise-shaped. So we consider here how to overcome DAC jitter effects and also how to handle even higher-frequency signals with a continuous-time bandpass modulator (Fig. 3).

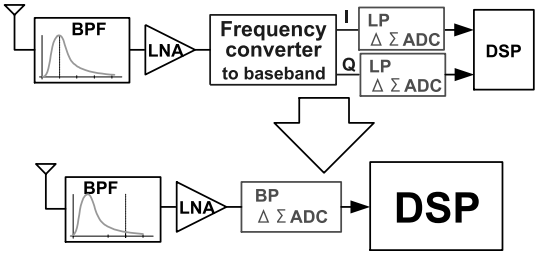

Fig. 1 Analog front-end of the targeted digital-rich analog-minimum receiver architecture.

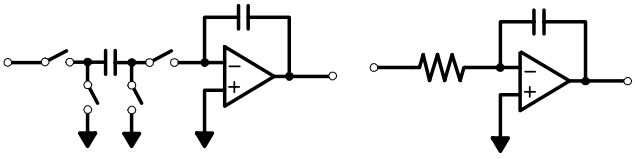

Fig. 2 Discrete-time circuit (left) and continuous-time circuit (right).

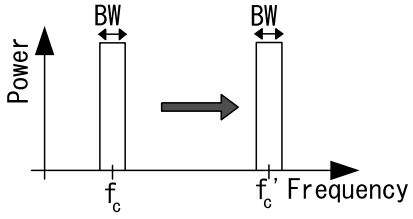

Fig. 3 For given sampling clock frequency, subsampling enables three-times higher center frequencies to be handled compared with conventional Nyquist sampling.

3. Nyquist Sampling vs. Subsampling

In most cases (regardless of discrete- or continuous-time

Manuscript received June 29, 2005.
Manuscript revised September 30, 2005.
Final manuscript received November 22, 2005.

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DOI: 10.1093/ietfec/e89–a.4.916

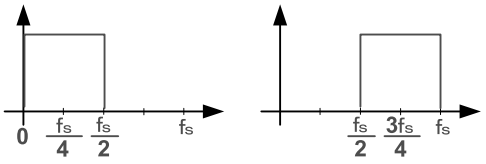


Fig. 4 Nyquist sampling (left) and subsampling (right).

circuit implementation), the sampling clock frequency of bandpass ΔΣAD modulators (f_s) is four times the center frequency of the input signal band (f_c) ($f_s = 4f_c$); one reason is ease of implementation of the digital filter that follows the modulator [10]. In other words, the center frequency of the signal band is one-fourth of the clock frequency at which the internal ADC and DAC operate ($f_c = f_s/4$); this is called as Nyquist sampling, and maximum signal bandwidth is from 0 to ($f_s/2$) (Fig. 4). Therefore, to handle high frequency input signals, the sampling clock frequency of the modulator has to be even higher, which makes the design of the internal ADC and DAC difficult.

To overcome this problem,"analog subsampling techniques" may be applied (Fig. 4), using a sampling frequency (f_s) which is 4/3 of the center frequency(f_c) of the input signal band ($f_s = (4/3)f_c$). That is, for given ADC and DAC clock frequency, this allows input signal frequency to be three times higher than with conventional Nyquist sampling ($f_c = (1/4)f_s$).

We call a modulator as a *Nyqusit-sampling* bandpass ΔΣ AD modulator if the center frequency of its signal band as well as that of its internal bandpass filter are $(1/4)f_s$, and also as a *subsampling* bandpass ΔΣ AD modulator if those are $(3/4)f_s$.

Some *discrete-time* bandpass AD modulators have already adopted this "subsampling technology," and LSI implementations have been reported. However, only a few of *continuous-time* bandpass AD modulator architectures using subsampling techniques have been reported [11], [12], and to our knowledge, no LSI implementations have been reported yet.

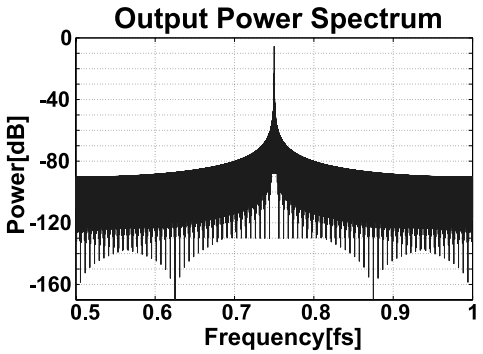
4. Subsampling Continuous-Time Bandpass ΔΣ AD Modulator

4.1 NRZ DAC Case

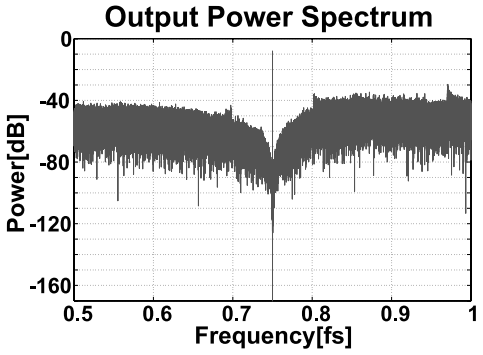
Subsampling in a continuous-time bandpass modulator is not easy to implement. If we use a NRZ (Non-Return-to-Zero, first-order-hold) output DAC (Fig. 6) inside a bandpass modulator and perform subsampling, then noise-shaped output spectrum is not obtained. (We confirmed this by MATLAB simulation, and the reason would be that gain of NRZ DAC impulse response is maximum at DC and it is attenuated by 10.45 dB at (3/4) f_s (Fig. 5(a)).)

4.2 RTZ DAC Case

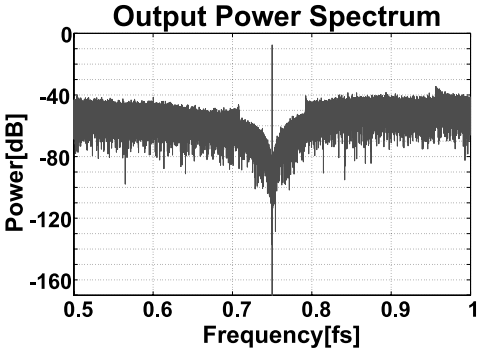
If we use a 25% RTZ (Return-to-Zero) output DAC (Fig. 6) and perform subsampling, there is a quantization noise notch at (3/4) f_s. (Fig. 5(b)). This method was proposed by Lucent Technology in 2004 [11]. However, when using this method, jitter of the RZ DAC sampling clock causes the accuracy of the entire AD modulator to significantly deteriorate; so in a continuous-time modulator with RTZ DAC, SNDR reduction due to jitter is more serious than with an NRZ DAC.



(a) NRZ DAC is used inside the modulator. There is a quantization noise peak at $(3/4)f_s$.



(b) 25% RZ DAC is used inside the modulator. There is a quantization notch at $(3/4)f_s$.

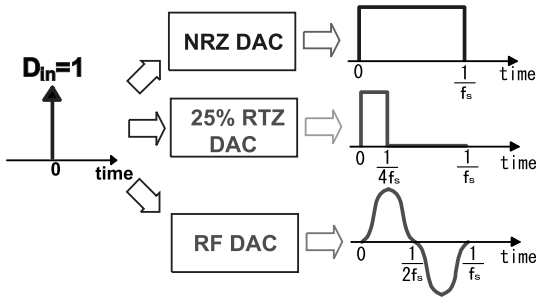


(c) RF DAC is used inside the modulator. There is a quantization notch at $(3/4)f_s$.

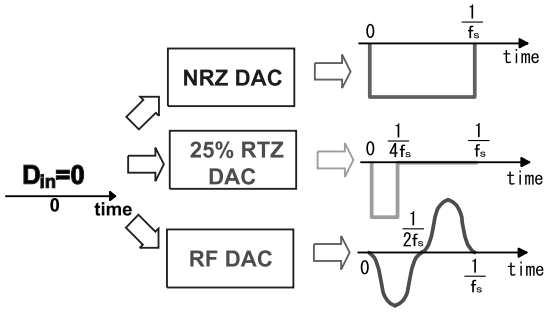
Fig. 5 Simulated output spectrum of subsampling continuous-time modulators with bandpass filters of $(3/4)f_s$ center frequency and input signal at $\approx (3/4)f_s$.

5. Proposed Subsampling Bandpass ΔΣAD Modulator Architecture

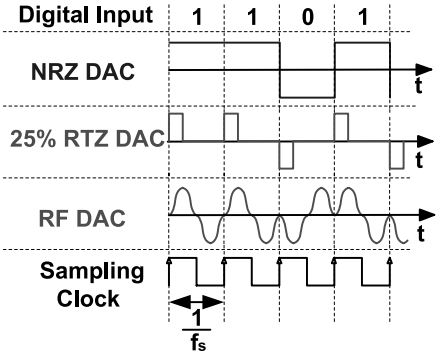
At MIT, on the other hand, a Radio-Frequency Digital-to-



(a) In case the digital input is "1."



(b) In case the digital input is "0."



(c) In case the digital input sequence is 1, 1, 0, 1.

Fig. 6 Output waveforms of 1-bit NRZ DAC, 25% RZ DAC and RF DAC.

Analog Converter (RF DAC) was proposed to generate the narrowband high frequency signal [13] (Fig. 6).

- The RF DAC output generates several cycles of a sine wave (or cosine wave) during one sampling period. An NRZ DAC, on the other hand, outputs a constant value during one sampling cycle.
- Gain of the RF DAC impulse response is maximum at 0.883 f_s and it is attenuated by only 0.23 dB at (3/4) f_s, and also it is 0 at DC. On the other hand, that of the NRZ DAC is maximum at DC and it is attenuated by 10.45 dB at (3/4) f_s (Fig. 7).
- Influence of sampling clock jitter on RF DAC is extremely small because its output is a continuous sine (or cosine) wave and its slew rate is 0 ($dDAC_{out}/dt = 0$) at each sampling timing. On the other hand, the output data value of an NRZ DAC changes discontinuously at each sampling timing, and the influence of jitter is significant.

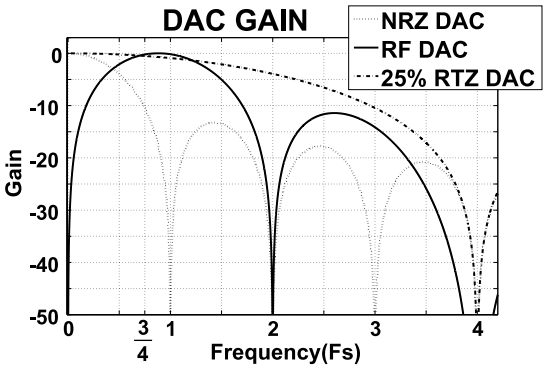


Fig. 7 Power spectrum of the impulse responses of NRZ DAC and RF DAC. Gain of NRZ DAC is maximum at DC, while that of the RF DAC is maximum at $\frac{3}{4}f_s$.

Remark (i) The RF DAC described in [13] is used as a standalone DAC, and its application to bandpass ΔΣ AD modulators is not discussed.
(ii) Application of a pulse-shaped DAC to a continuous-time bandpass ΔΣ AD modulator was proposed, to reduce effects of jitter, in [14]. However it does not discuss the subsampling technique.

Based on the above-mentioned considerations, we propose to use this RF DAC for $(4/3)f_c$ subsampling continuous-time bandpass modulators (Fig. 5(c)).

- The center frequency of the input signal band is 3/4 of the sampling clock frequency at which internal ADC and DAC operate. (That is, for given sampling clock frequency, it can handle three times higher input frequencies than with conventional Nyquist-sampling (Fig. 3).)
- SNDR deterioration of the entire AD modulator caused by sampling clock jitter of DAC is extremely small.

Also note that in general, continuous-time ΔΣ modulators have the following advantages over discrete-time (switched capacitor) circuits ones:

- Low power consumption
- High sampling clock frequency
- Design of the analog anti-aliasing filter that precedes the modulator is simplified.

Next we will describe the proposed bandpass modulator architecture, and MATLAB simulation results.

6. Principle and Operation of RF DAC

Figure 6 shows output waveforms of 1-bit NRZ DAC and and RF DAC. The output of 1-bit NRZ DAC at sampling time k is as follows:

- When the digital input is "1":
  $D_{out,NRZ}(t) \equiv 1 \quad \left(\text{for } \frac{k}{f_s} \le t \le \frac{k+1}{f_s}\right)$
- When the digital input is "0":

$$D_{out,NRZ}(t) \equiv -1 \quad \left(\text{for } \frac{k}{f_s} \le t \le \frac{k+1}{f_s}\right),$$

where ($k = 0, \pm1 \pm 2, \pm3, ...$). On the other hand, the output of a 1-bit RF DAC is as follows:

- When the digital input is "1":
  $D_{out,RF}(t) = A_1(t) \quad \left(\text{for } \frac{k}{f_s} \le t \le \frac{k+1/2}{f_s}\right)$
  $D_{out,RF}(t) = A_2(t) \quad \left(\text{for } \frac{k+1/2}{f_s} \le t \le \frac{k+1}{f_s}\right).$
- When the digital input is "0":
  $D_{out,RF}(t) = A_2(t) \quad \left(\text{for } \frac{k}{f_s} \le t \le \frac{k+1/2}{f_s}\right)$
  $D_{out,RF}(t) = A_1(t) \quad \left(\text{for } \frac{k+1/2}{f_s} \le t \le \frac{k+1}{f_s}\right).$

Here,

$$A_1(t) = -\frac{1}{2}\cos\{2\pi(2f_s)t\} + \frac{1}{2}$$
$$A_2(t) = \frac{1}{2}\cos\{2\pi(2f_s)t\} - \frac{1}{2}.$$

That is, the operation of RF DAC is as follows:

- When its digital input is "1," it outputs a wave switched at the middle of the sampling period in the order of $A_1(t) \to A_2(t)$ as shown in Fig. 6.
- When its digital input is "0," it outputs a wave switched at the middle of the sampling period in the order of $A_2(t) \to A_1(t)$.

This RF DAC circuit can be realized with a relatively-simple differential pair circuit with a tail current source that alternates the current at $\cos\{2\pi(2f_s)t\}$. We propose the differential circuit topology of Fig. 8.

Power Spectrum of the impulse response of the RF DAC is maximum at $\frac{3}{4}f_s$ and its DC component is 0 as shown in Fig. 7.

Noting these characteristics of the RF DAC, we propose a continuous-time bandpass ΔΣ modulator (Fig. 9) which uses an RF DAC inside the modulator and performs subsampling at the frequency $\frac{4}{3}f_c$.

Also the RF DAC has the following characteristics for $k = 0, \pm1, \pm2, \pm3, ...$:

$$A_1(k/(2f_s)) = 0, \quad A_2(k/(2f_s)) = 0, \tag{1}$$
$$\left.\frac{dA_1}{dt}\right|_{t=(k/(2f_s))} = 0, \quad \left.\frac{dA_2}{dt}\right|_{t=(k/(2f_s))} = 0. \tag{2}$$

Thanks to these characteristics of Eqs. (1), (2), the RF DAC is expected to be insensitive to sampling clock jitter [15], [16]. On the other hand, an NRZ DAC is sensitive to such jitter, and an RTZ DAC is much worse: it is influenced by jitter on both rising and falling timing edges.

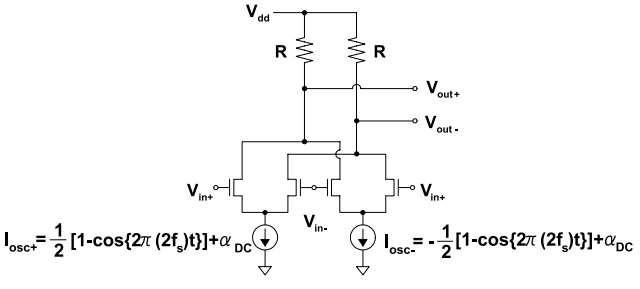


Fig. 8 1-bit RF DAC implementation circuit with differential topology.

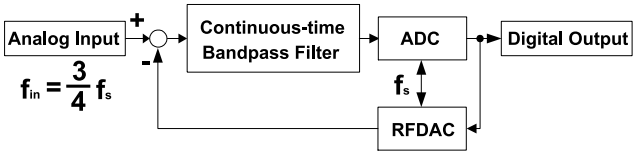


Fig. 9 A block diagram of the proposed continuous-time bandpass ΣΔAD modulator. The center freqeuency of the continuous-time bandpass filter is $\frac{3}{4}f_s$, and subsampling is achieved using RF DAC in the feedback path.

7. MATLAB Simulation

7.1 Subsampling Operation

To confirm the operation of the proposed bandpass modulator architecture, we have performed MATLAB simulation. We use a continuous-time second-order bandpass filter with center frequency $(3/4)f_s$ and a 1-bit RF DAC inside the modulator, and apply an input signal of $\approx (3/4)f_s$ as shown in Fig. 10. The loop filter coefficient values are set as follows:

$$b_1 = \frac{1.5}{30}\omega_c, \quad b_2 = \frac{5}{30}\omega_c \quad \text{where } \omega_c = 2\pi\left(\frac{3}{4}f_s\right). \tag{3}$$

Figure 11(a) shows the modulator output power spectrum, and we see that the quantization noise spectrum is noise-shaped at $(3/4)f_s$. Figure 11(b) shows SNDR vs. OSR (OverSampling Ratio), and the slope is 15 dB/oct which is close to the theoretical value [10]. Note that OSR is defined as $f_s/(2 \cdot \text{signal bandwidth})$. Thus it is confirmed that the proposed configuration of Fig. 10 operates correctly as a subsampling bandpass ΔΣ modulator.

7.2 Jitter Effects

Next, we will discuss the jitter effect through simulation, and compare the RF DAC case and RTZ DAC for pulse width 25% case ([11]). We apply Gaussian random clock jitter whose standard deviation (σ) is 1% of the clock period

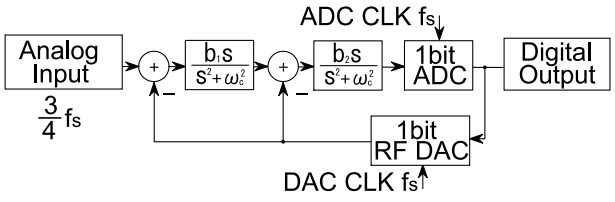
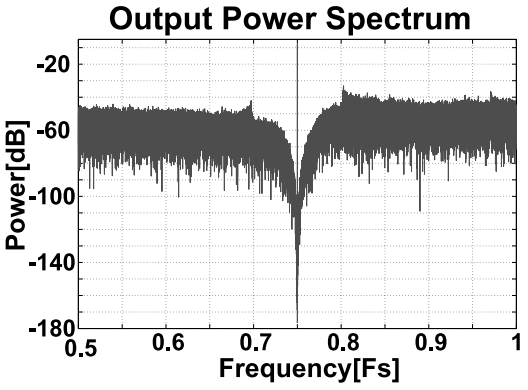
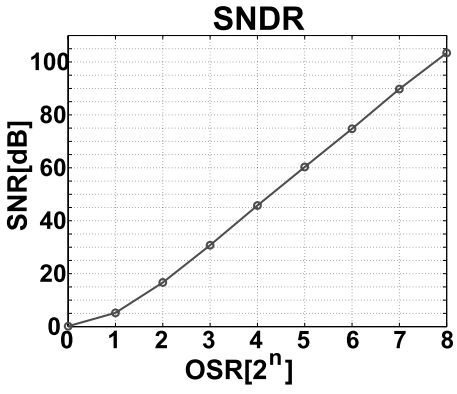


Fig. 10 Simulation block diagram of the proposed method with internal 1-bit ADC/DAC.

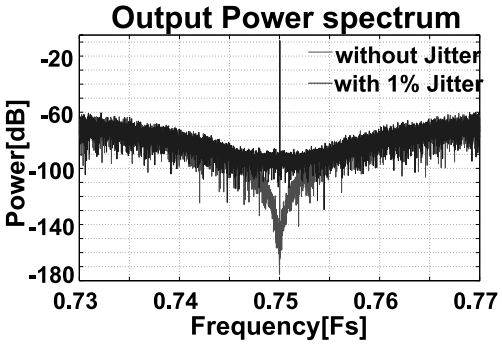


(a)

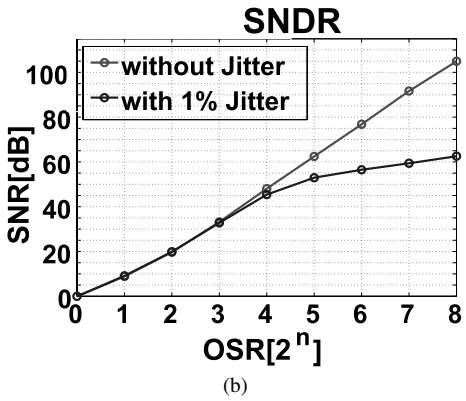


(b)

Fig. 11 (a) Output power spectrum of the proposed modulator (Fig. 10). There is a quantization notch at $\frac{3}{4}f_s$. (b) SNDR vs. OSR. The slope of the graph is $\approx$ 15 dB/oct. MATLAB simulation results of the proposed modulator (Fig. 10).



(a)



(b)

Fig. 12 (a) The output power spectrum of a subsampling modulator using 25% RTZ DAC when RZ DAC sampling clock jitter of 25% is considered. The noise floor rises greatly due to jitter. (b) SNDR vs. OSR of the modulator with 25% RTZ DAC when RTZ DAC sampling clock jitter of 25% is considered. The SNDR deterioration is significant.

to the DAC. Fig. 12(a) and Fig. 13(a) show the modulator output power spectrum for each case. Also Fig. 12(b), and Fig. 13(b) show SNDR vs. OSR; we see that in the RF DAC case, SNDR is insensitive to jitter, but in the RTZ DAC case, SNDR degrades significantly due to jitter.

8. Extension to Multibit Modulator

In this section, we consider extending our subsampling bandpass architecture by using multibit ADC/RF DAC inside the modulator to achieve higher resolution (Fig. 14). Figure 15 shows a 3-bit RF DAC input sequence and its corresponding output waveform. When a 3-bit ADC/RF DAC is incorporated inside a modulator, the stability is improved and we can choose larger values of loop filter coefficients inside the modulator (Fig. 14) which leads to further SNDR improvement:

$$b_1 = \frac{3}{30}\omega_c, \quad b_2 = \frac{18}{30}\omega_c, \quad \text{where } \omega_c = 2\pi\left(\frac{3}{4}f_s\right). \quad (4)$$

Note that the coefficient values for 3-bit RF case in Eq. (4) can be set larger than those in 1-bit RF DAC case in Eq. (3); if the values in Eq. (4) are used in the modulator with 1-bit RF DAC, it becomes unstable.

Figure 16(a) shows the output power spectrum comparison between 1-bit and 3-bit cases, and also Fig. 16(b) is their SNDR vs. OSR comparison: SNDR of 3-bit case is improved by 27 dB at OSR=64. We note that multibit modulators suffer from DAC nonlinearity problems, but Data Weighted Algorithm (DWA) can overcome such problems [5], [8].

9. Excess Loop Delay

Excess loop delay in the modulator can be defined as the delay from the internal ADC output (which is fed to the internal DAC input) to the corresponding DAC output timing (Fig. 17). It is known that the continuous-time bandpass $\Delta\Sigma$ AD modulator suffers from such excess loop delay problems [17]: when the excess loop delay becomes large, SNDR of the whole AD modulator degrades. We have investigated this problem for our architecture, and observe the following:

- For a Nyquist sampling ($f_{in} = (1/4)f_s$) bandpass modulator with 1-bit NRZ DAC, excess loop delay can be as much as $0.7/f_s$ without degrading SNDR.
- For subsampling ($f_{in} = (3/4)f_s$) bandpass modulator with 1-bit 25% RTZ DAC, excess loop delay can be as much as $0.06/f_s$.

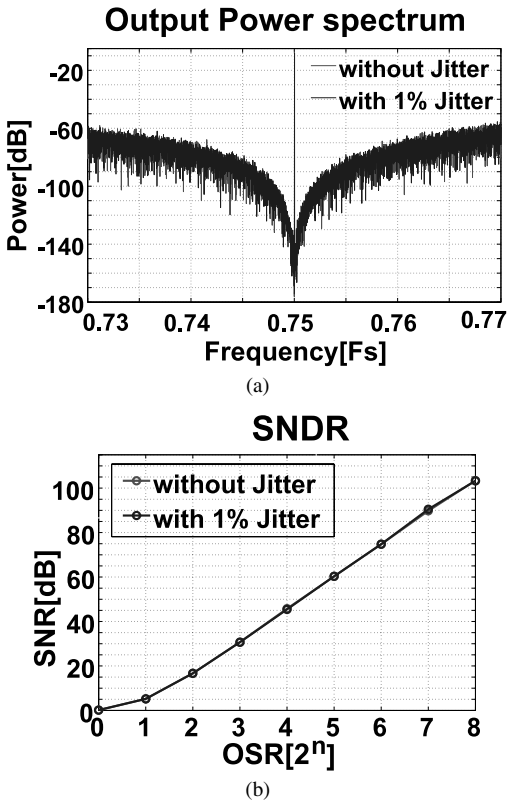


Fig. 13 (a) Power spectrum of the proposed modulator output when sampling clock jitter of RF DAC is considered. The noise floor rises slightly due to jitter. (b) SNDR vs. OSR of the proposed modulator with RF DAC when sampling clock jitter of RF DAC is considered. The SNDR does not degrade.

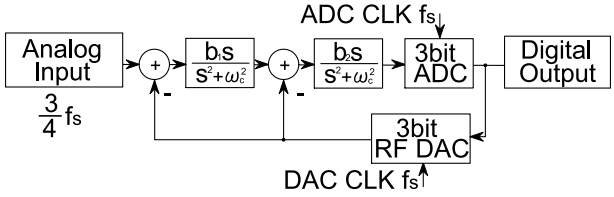


Fig. 14 Simulation block diagram of the proposed method with internal 3-bit ADC/DAC.

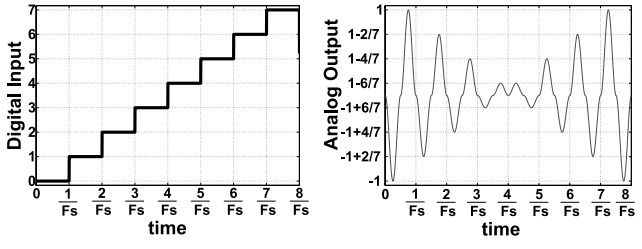


Fig. 15 3-bit RF DAC input (left) and output (right).

- For subsampling ($f_{in} = (3/4)f_s$) bandpass modulator with 1-bit RF DAC, excess loop delay can be as much as $0.03/f_s$.
- For subsampling ($f_{in} = (3/4)f_s$) bandpass modulator with 3-bit RF DAC, excess loop delay can be as much as $0.12/f_s$.

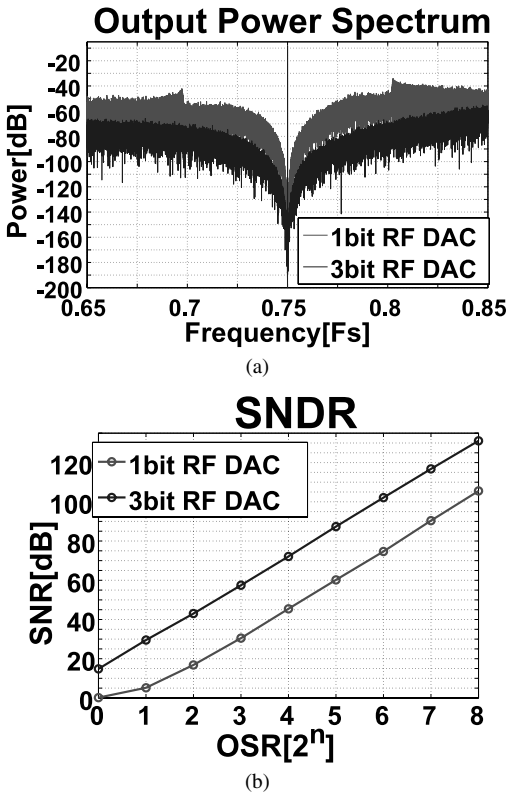


Fig. 16 (a) Output power spectrum of the proposed subsampling modulators with 1-bit RF DAC and 3-bit RF DAC. (b) SNDR vs. OSR of the proposed modulators with 1-bit RF DAC and 3-bit RF DAC.

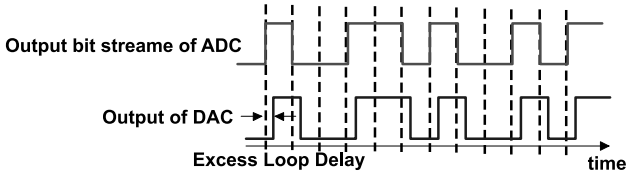


Fig. 17 Explanation of excess loop delay.

We see that subsampling continuous-time modulators suffer from excess loop delay problems, and modulators with RF DAC suffer worse; the reason why subsampling modulators with RF DAC suffer worse from excess loop delay than modulators with 25% RTZ DAC would be that RTZ DAC output responds faster than RF DAC to input changes (Fig. 18). However, multibit modulator structure is one way of reducing effects of excess loop delay.

10. Conclusions

We have proposed a high-speed continuous-time bandpass ΔΣ AD modulator with an RF DAC which enables subsampling techniques and reduces effects of DAC clock jitter, and have confirmed its operation by MATLAB simulation. We show a differential circuit implementation of the RF DAC. We extend our modulator to a multi-bit structure and show

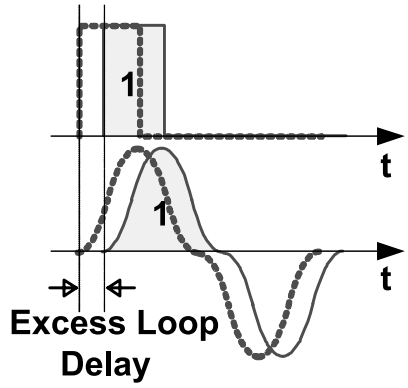


Fig. 18 Consideration why the modulator with RF DAC suffers from excess loop delay.

that this alleviates excess loop delay problems. This bandpass modulator architecture is expected to realize direct AD conversion of RF signals, which facilitates implementation of next-generation digital-rich analog-minimum radio systems.

Acknowledgements

We would like to thank T. Matsuura, M. Miyamoto, H. San, T. Kozawa and K. Wilkinson for valuable discussions. Thanks are also due to Semiconductor Technology Academic Research Center (STARC) that supports this research.

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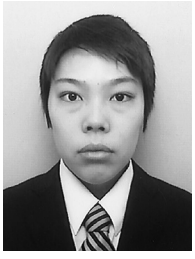

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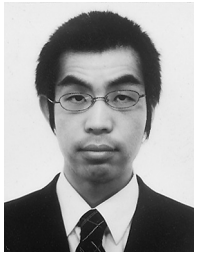

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