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Low-Voltage Rail-to-Rail CMOS Operational Amplifier Design

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SUMMARY

This paper describes the design of a low-voltage CMOS rail-to-rail operational amplifier. We have designed input signal compression circuitry that compresses rail-to-rail input signals to the input range of the following folded-cascode operational amplifier, which is capable of rail-to-rail output. The input signal compression circuitry and the following folded-cascode operational amplifier together comprise an input-output rail-to-rail operational amplifier. SPICE simulation with 0.18-μm CMOS BSIM3v3 parameters validates the operation of the rail-to-rail CMOS amplifier with supply voltage of 0.7 V and bias current of 3.1 μA. © 2006 Wiley Periodicals, Inc. Electron Comm Jpn Pt 2, 89(12): 1–7, 2006; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/ecjb.20297

Key words: CMOS; operational amplifier; rail-to-rail; low voltage.

1. Introduction

Here we consider the design of a standard-CMOS operational amplifier which can handle rail-to-rail inputs and outputs and operate on a supply voltage of 0.7 V (or lower) for applications in battery-operated handy mobile equipment such as cellular phones and digital still cameras [1–6]. We propose input signal compression circuitry to compress rail-to-rail input signals to the input range of the following folded-cascode operational amplifier, which is capable of rail-to-rail output. SPICE simulation was used to validate the operation of the proposed rail-to-rail operational amplifier with power supply voltage of 0.7 V current consumption of 3.1 μA.

2. Conventional Rail-to-Rail CMOS Operational Amplifiers

This section reviews topologies of already-reported CMOS rail-to-rail input operational amplifiers.

(1) Complementary input differential pair circuits, Fig. 1 [2].

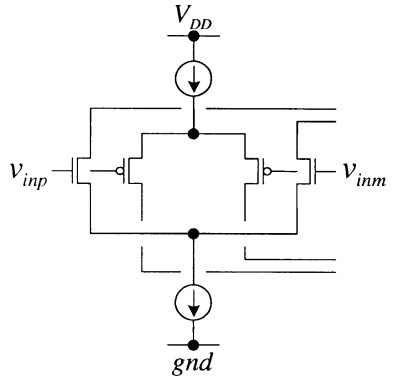

Fig. 1. Complementary input differential pair circuits.

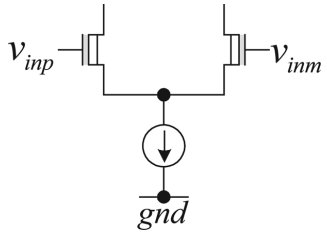

Fig. 2. Input differential pair circuit with depletion-type NMOS FETs.

This topology uses both an NMOS differential pair and a PMOS differential pair. Because overall transconductance (g_m) changes with input common mode voltage, it is difficult to stabilize this operational amplifier. This circuit is also not suitable for low-supply-voltage operation.

(2) Input differential pair circuit with depletion-type NMOS FETs, Fig. 2 [1].

This circuit requires depletion-type MOSFETs, which cannot be fabricated by standard digital CMOS processes.

(3) Input differential pair circuit driven by substrate voltages, Fig. 3 [1].

The differential input signals are fed into the bulk nodes of an NMOS differential pair instead of their gate nodes. Hence, input impedance is low; it may require depletion-type MOSFET source follower circuits to provide high-impedance input [1]. Also, a large γ value is required to achieve sufficient bulk conductance (g_{bs}).

3. Proposed Operational Amplifier Topology and Operation

3.1. Topology of whole operational amplifier

Using any of the above-mentioned topologies, and standard CMOS processes, it would be difficult to realize a

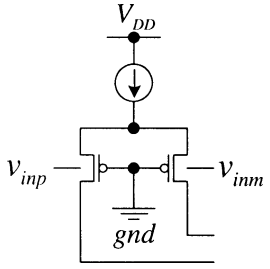

Fig. 3. Input differential pair circuit driven by substrate voltages.

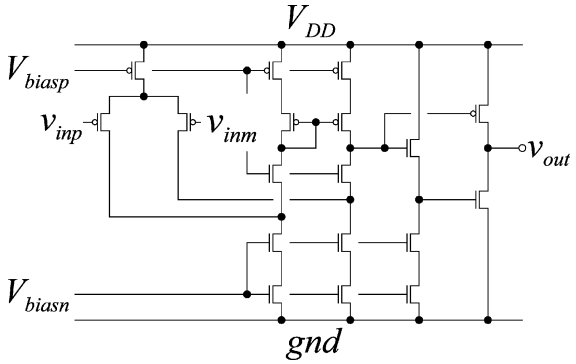

Fig. 4. A folded-cascode operational amplifier whose output is rail-to-rail, but whose input common-mode range (CMR) is not rail-to-rail.

CMOS rail-to-rail operational amplifier with supply voltage of 0.7 V; here we propose a new topology.

Figure 4 shows a CMOS folded-cascode operational amplifier. It is capable of rail-to-rail output, but it cannot handle rail-to-rail input; its input must be limited to its common-mode range. Hence, we propose using a signal compression circuit in front of the input differential pair to compress rail-to-rail input signals, with a range from GND to V_{dd}, to within the input range of the amplifier. The input-output transfer function of the proposed signal compression circuit is shown in Fig. 5: even when the input signal changes from GND to V_{dd}, its output is within the input range of the following operational amplifier, and this is equivalent to expanding the input common-mode range of the operational amplifier. Also note that DC feedback around the operational amplifier ensures that the differential input is balanced, and hence SNR is not degraded due to the input signal compression circuit.

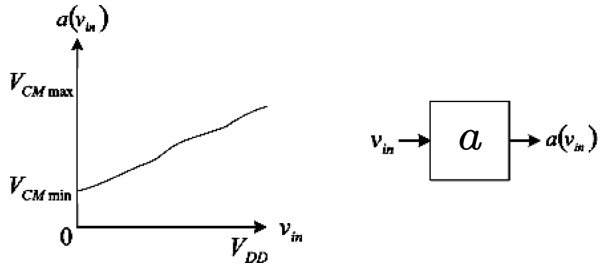

Fig. 5. Input-output characteristics of an input signal compression circuit that compresses the rail-to-rail input to the input range of the following operational amplifier. Monotonicity must be guaranteed, but some nonlinearity is tolerable, because feedback is applied around the operational amplifier as a whole.

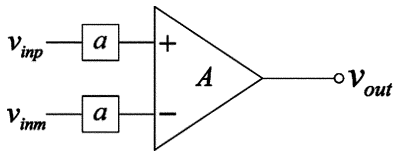

Fig. 6. The input signal compression circuits (*a*) and the output rail-to-rail operational amplifier (*A*) together comprise a rail-to-rail operational amplifier.

Figure 6 shows the overall topology of our proposed input-output rail-to-rail operational amplifier, with a newly designed signal compression circuit—whose input-output transfer function is shown in Fig. 5—added to each of the differential inputs of the folded-cascode operational amplifier (Fig. 4).

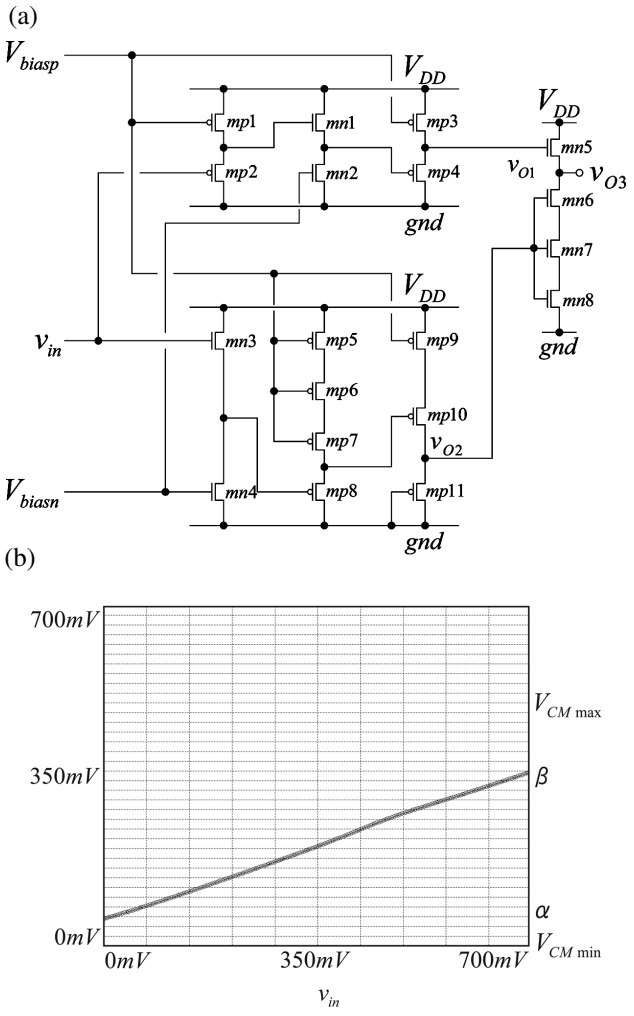

Fig. 7. (a) Our input signal compression circuit design, which corresponds to "a" in Fig. 6. (b) SPICE simulation result for the circuit in panel (a). We see that the input signal is compressed.

3.2. Proposed input signal compression circuit

We have designed input signal compression circuitry, with input-output transfer function as shown in Fig. 5, that operates on supply voltage of 0.7 V and consumes little power. Figure 7 shows a diagram of the circuit, which consists of the three parts shown in Figs. 8(a), 9(a), and 10(a).

Figure 7(b) shows results of SPICE DC simulation of the input-output transfer function of the circuit of Fig. 7(a), and we see that it is monotonic. (Small nonlinearity is not a problem because of feedback around the operational amplifier.) The values of α, β in Fig. 7(b) can be set by adjusting MOS device sizes and bias voltages V_{biasp} and V_{biasn} in Fig. 7(a).

(A) Explanation of circuit in Fig. 8

The circuit in Fig. 8 consists of a PMOS source follower in the first stage, an NMOS source follower in the second stage, and a PMOS source follower in the third stage. This cascade of three source follower circuits shifts the output signal to the proper voltage level and also makes its small-signal gain less than one. The output signal V_{o1} is

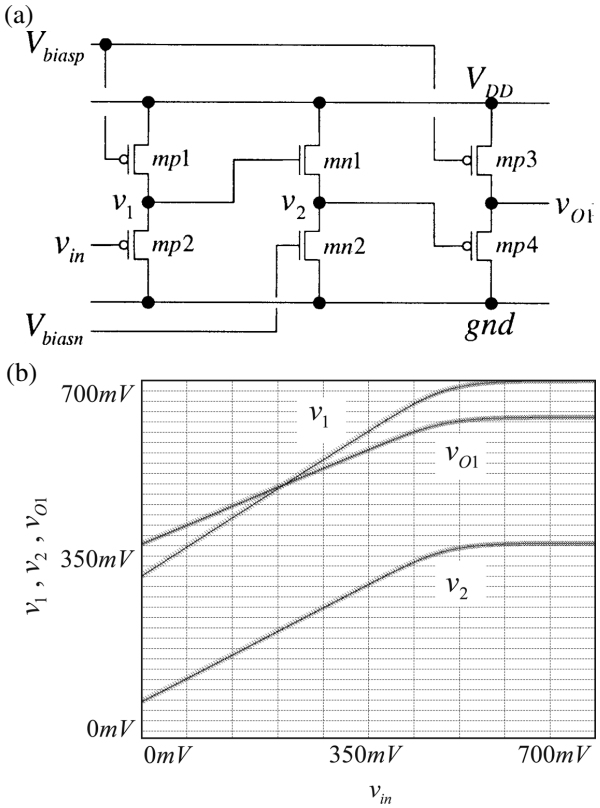

Fig. 8. (a) The upper-left part of the input signal compression circuit in Fig. 7(a). (b) SPICE simulation results for the circuit in panel (a).

shifted up by 350 mV when the input signal level is low, while V_{o1} saturates to a constant voltage (≈ 650 mV) when V_{in} is high (> 500 mV).

Figure 8(b) shows SPICE simulated DC characteristics of the circuit in Fig. 8(a).

(B) Explanation of circuit in Fig. 9

An NMOS source follower in the first stage and a PMOS source follower in the second stage shift the input voltage to a proper output voltage level.

The third-stage circuit inverts the signal and operates as follows: When V_4 is low, V_5 follows V_4 by source follower operation of mp9 and mp10, and V_{o2} output is constant because the source-gate voltages of mp9 and mp11 are almost the same. On the other hand, when V_4 is high, V_5 saturates close to V_{dd}; and the third-stage circuit (whose input is V_4 and output is V_{o2}) becomes a common-source amplifier, and V_{o2} is the inverted output of V_4.

Figure 9(b) shows SPICE-simulated DC characteristics of the circuit in Fig. 9(a).

(C) Explanation of circuit in Fig. 10

The inputs of the circuit in Fig. 10(a) are V_{o1} [which is the output of Fig. 8(a)] and V_{o2} [which is the output of Fig. 9(a)], and also its output is V_{o3}, which is a compressed version of V_{in}. Figure 10(b) shows SPICE-simulated DC characteristics of the circuit in Fig. 10(a).

When V_{in} is low (< ≈ V_{dd}/2), the circuit of Fig. 10(a) operates as an NMOS source follower with an input of V_{o1} and output of V_{o3}, because V_{o2} is constant, as shown in Fig. 9(b). On the other hand, when V_{in} is high (> ≈ V_{dd}/2), V_{o3} is proportional to V_{in}. This is because V_{o1} is constant, as shown in Fig. 8(b), V_{o2} and $V_{o1} - V_{o3}$ (≈ 650 mV – V_{o3}) are almost equal, and so V_{o2} is an inverted version of V_{in} (the small-signal gain of V_{o2} with respect to V_{in} is negative).

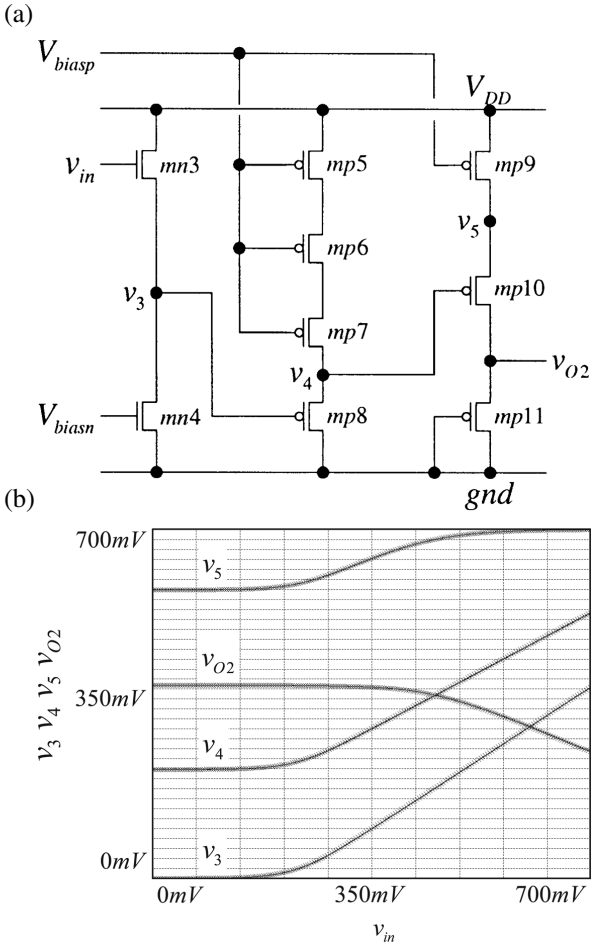

Fig. 9. (a) The lower-left part of the input signal compression circuit in Fig. 7(a). (b) SPICE simulation results for the circuit in panel (a).

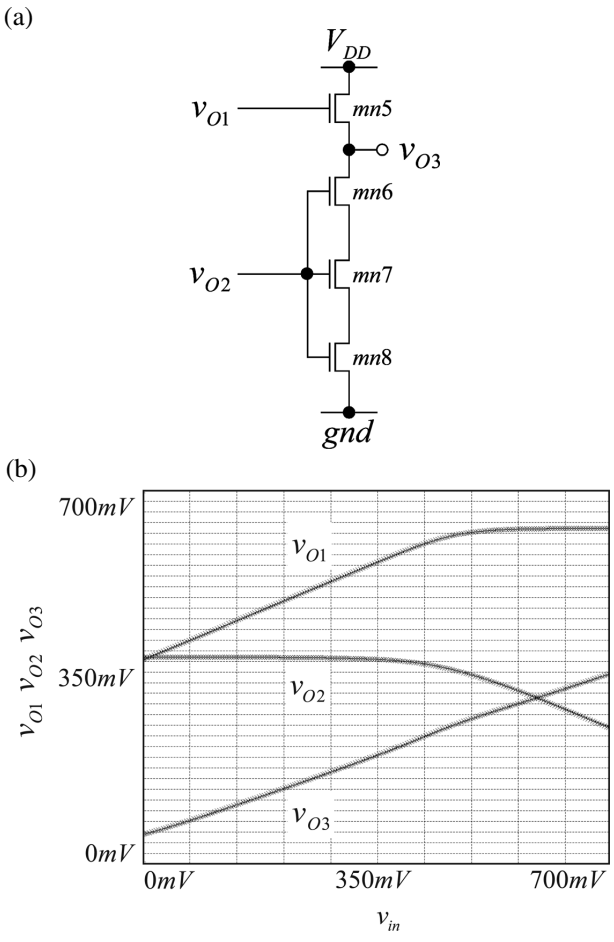

Fig. 10. (a) The right part of the input signal compression circuit in Fig. 7(a). (b) SPICE simulation results for the circuit in panel (a).

Table 1. SPICE-simulated characteristics of the operational amplifier in Fig. 4

Item	Condition	Performance
DC gain	No load	67 dB
Current consumption		0.3 μA
Common-mode input range		0∼0.5 V
Output voltage range	Load 50 pF	0∼0.7 V
Gain-bandwidth product	No load	100 Hz
Phase margin	No load	90 degrees
Maximum load capacitance		50 pF
Slew rate	Load 50 pF	46 V/ms
Supply voltage		0.7 V
Minimum channel length		0.18 μm

3.3. Gain stage and output circuit

Figure 4 shows only the gain stage and output circuit (these are preceded by the newly designed input compression circuit). Table 1 shows the characteristics of the operational amplifier in Fig. 4 (not including input compression circuitry), obtained by SPICE simulation.

Figure 11 shows the ramp response of this amplifier's voltage follower, with rail-to-rail input applied to check input common-mode range, and this verifies that the circuit in Fig. 4 cannot accept rail-to-rail input.

Note that most of the MOSFETs in Fig. 4 operate in the subthreshold region, because V_{dd} is 0.7 V and threshold voltages of NMOS and PMOS are 0.3 and –0.3 V, respectively. It is known that process-related variations in MOS subthreshold region characteristics are fairly large, and also our SPICE simulation shows that DC gain of the circuit in Fig. 4 varies with temperature due to subthreshold region

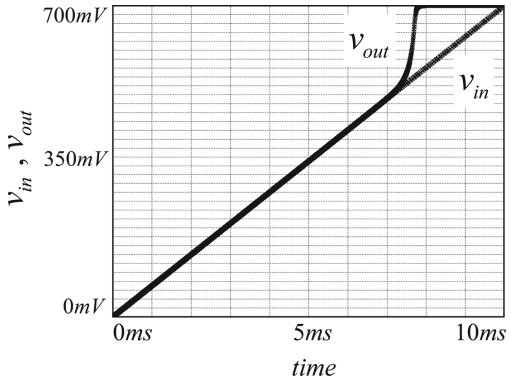

Fig. 11. Result of SPICE simulation to check the input common-mode range of the operational amplifier in Fig. 4. A ramp signal input from 0 to 0.7 V is applied to the voltage follower. We see that its input common-mode range is from 0 to ≈ 0.5 V, which is not rail-to-rail.

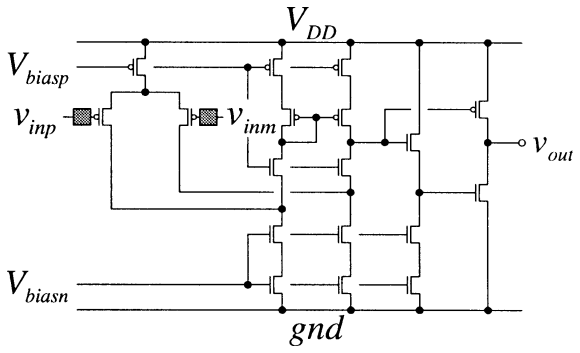

Fig. 12. Proposed rail-to-rail operational amplifier with the input signal compression circuits of Fig. 7 (represented by the boxes at the inputs) connected to the operational amplifier of Fig. 4.

operation. Hence, MOS circuits operating in the subthreshold region should be used in a temperature-controlled environment and/or should employ bias circuits that compensate for temperature change and process variation.

We note that combination of our new input signal compression circuit with another rail-to-rail-output operational amplifier (other than that shown in Fig. 4) would also realize an input-output rail-to-rail operational amplifier.

3.4. Simulation of overall operation amplifier circuit

Figure 12 shows the overall operational amplifier circuit, and Table 2 shows its characteristics obtained by SPICE simulation. Figure 13 shows its ramp response, while Fig. 14 shows the step response of its voltage follower configuration obtained by SPICE transient simulation. We see that the operational amplifier has input-output rail-to-rail characteristics, and it is stable.

Table 2. SPICE-simulated characteristics of our proposed rail-to-rail operational amplifier in Fig. 12

Item	Condition	Performance
DC gain	No load	64 dB
Current consumption		3.1 μA
Common-mode input range		0∼0.7 V
Output voltage range	Load 50 pF	0∼0.7 V
Gain-bandwidth product	No load	100 Hz
Phase margin	No load	60 degrees
Maximum load capacitance		50 pF
Slew rate	Load 50 pF	46 V/ms
Supply voltage		0.7 V
Minimum channel length		0.18 μm

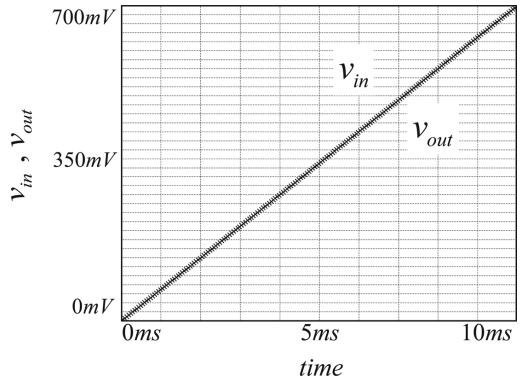

Fig. 13. Results of SPICE simulation to check the input common-mode range of the proposed operational amplifier of Fig. 12. A ramp signal input from 0 to V_{dd} (0.7 V) is applied to the voltage follower. We see that input common-mode range is from 0 to 0.7 V, which is rail-to-rail.

Note that the bandwidth of the designed operational amplifier is ≈100 Hz, which is quite low, but in its target applications of man–machine and sensor interfaces this bandwidth is sufficient but low power is mandatory. Of course, the bandwidth can be increased, according to application requirement, by increasing the bias currents.

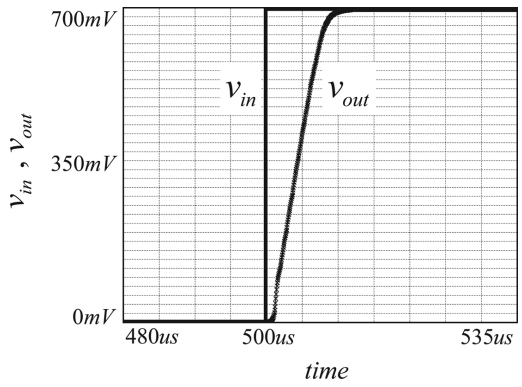

Fig. 14. SPICE-simulated step response of the proposed operational amplifier (Fig. 12) with voltage follower configuration. We see that the circuit is stable and V_{out} follows V_{in}.

4. Conclusion

We have proposed a new input-output rail-to-rail operational amplifier topology using standard digital CMOS processes, operating with supply voltage of 0.7 V. A newly designed input signal compression circuit was added to the input of a folded-cascode operational amplifier. The compression circuit enables rail-to-rail input, while the folded-cascode operational amplifier has rail-to-rail output. Next, we plan to investigate the following:

- Device mismatch effects due to operational amplifier offset voltages
- Further low-power designs
- Further low-voltage designs (voltages less than 0.5 V)

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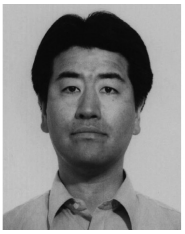


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