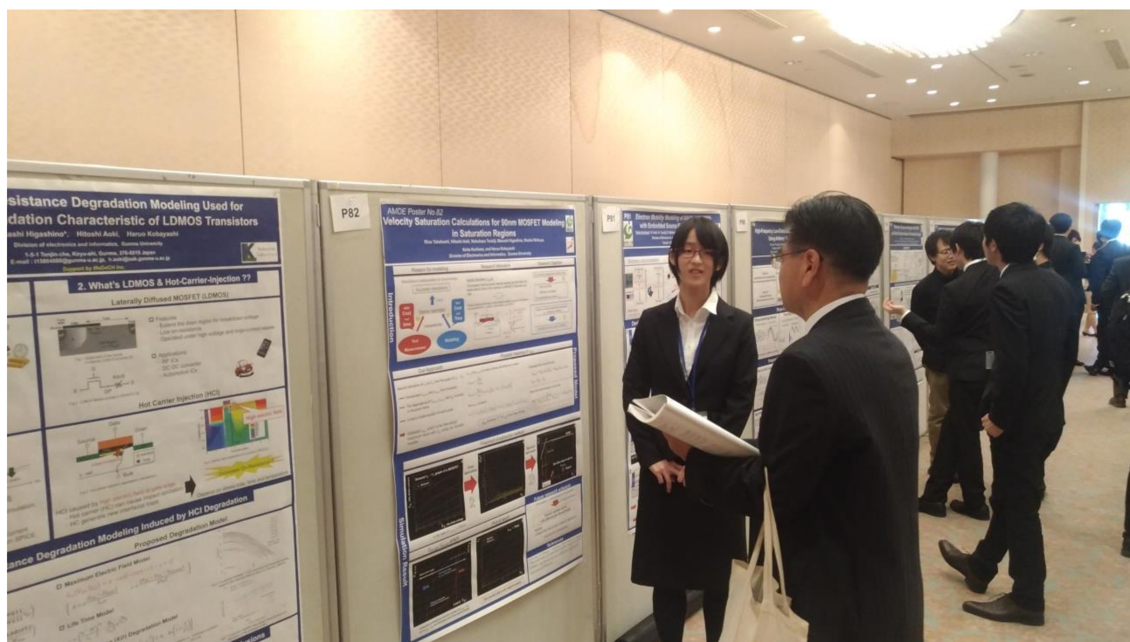
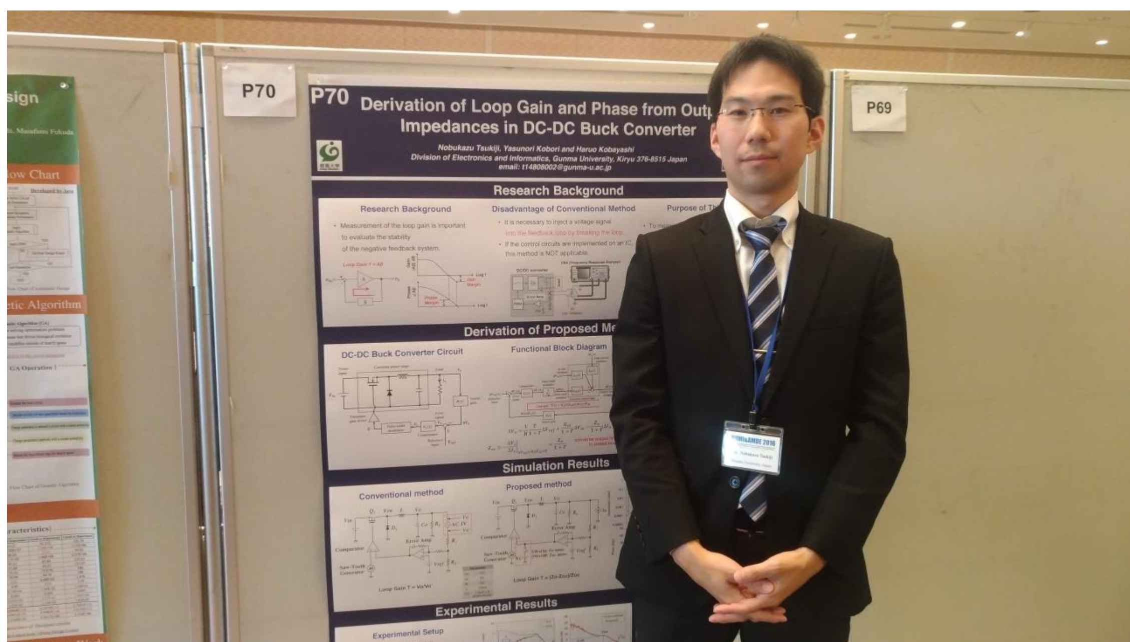
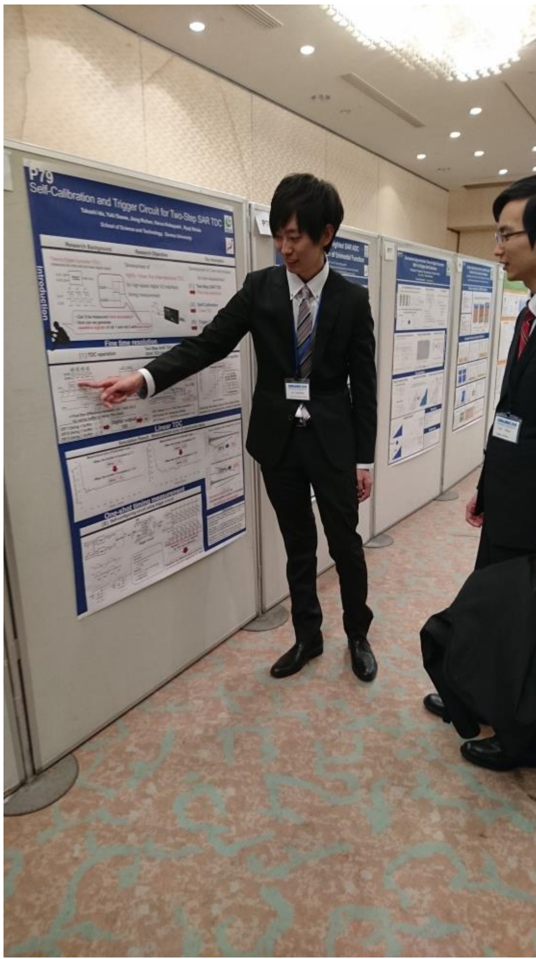
3rd International Symposium of Gunma University Medical Innovation (GUMI),
8th International Conference on Advanced Micro-Device Engineering (AMDE)

2016 年 12 月 9 日（金）群馬県桐生市市民文化会館にて開催

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Self-Calibration and Trigger Circuit for Two-Step SAR TDC
Introduction
Fine time resolution

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# P81 Electron Mobility Modeling of AlN/GaN MIS-HEMTs with Embedded Source Field-Plate Structures


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群馬大学

Kobayashi Laboratory

## Introduction

Electronic circuit simulator

Specification → Design → Implementation → Measurement → Evaluation

Need many money & Time...

Specification → Design → Simulation → Evaluation

Low cost & speedy.

Device Modeling

Measurement

Modeling

Simulation

Model

Research Background

Background

GaN

Breakdown voltage

Miniaturization

Switching speed

Circuit Size Large → Small

Performance

Circuit Density

Devices charastric | Application
---|---
Normally-On | Communication
Normally-Off | Power devices

Trend

Research Goal

Research & develop drain current model of normally-off GaN-MIS HEMTs

## Device Structure

① S G D

AlN/GaN layers

Employ MIS gate structure

② S G D

Oxidized AlN

AlN/GaN layers

## New Electron Mobility Model

New Electron Mobility Model

$$\mu_{eff} = \frac{\mu_0 \cdot U_{Leff}}{1 + U_{Gate} \cdot U_{SFP}}$$

Effective channel length

$$U_{Leff} = 1.0 - UP \cdot e^{-L_{eff}/LP}$$

Gate voltage

$$U_{Gate} = UA\left(\frac{V_{gs} + 2 \cdot V_{th}}{T_{ox}}\right) + UB\left(\frac{V_{gs} + 2 \cdot V_{th}}{T_{ox}}\right)^2$$

Source field plate

$$U_{SFP} = 1 + USFP \cdot V_{ds}$$

Surface

## Measurement & Simulations

Ids vs Vgs

Saturation region

Log(Ids) vs Vgs

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# Study on ON-Resistance Degradation Modeling Used for HCI Induced Degradation Characteristic of LDMOS Transistors


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## 1. Introduction

### Background

Reliability Test Problem in Circuit Design

Long testing time and high costs

Circuit design considering with reliability simulations

### Research Objective

Degradation modeling of n-channel LDMOS

- Model derivations for HCI degradation simulation.
  - Maximum electric field model
  - On-resistance degradation model
- Verifications our models with DC drain current simulations by using HiSIM-HV model on SPICE.

## 2. What's LDMOS & Hot-Carrier-Injection ??

### Laterally Diffused MOSFET (LDMOS)

- Features
  - Extend the drain region for breakdown voltage
  - Low on-resistance
  - Operated under high-voltage and large-current biases
- Applications
  - RF ICs
  - DC-DC converter
  - Automotive ICs

### Hot Carrier Injection (HCI)

Gate

Source

Drain

Bulk

High electric field

HCI caused by high electric field at gate edge.
- Hot carrier (HC) can cause impact ionization
- HC generate new interfacial traps

Increases On-Resistance !!

Depend on stress bias, time and temperature

## 3. ON-Resistance Degradation Modeling Induced by HCI Degradation

HiSIM-HV model

- Drift Resistance

Proposed Degradation Model

- Maximum Electric Field Model

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