エコ社会を支えるパワーIC技術
―高耐圧SOIと低耐圧BCD―

中川 明夫
中川コンサルティング事務所

謝辞

本報告で、出典等の表示のない部分の資料は、筆者が東芝在籍中に外部発表で使用した資料に基づいて再構成し、作成したものです。
関係する方々に感謝の意を表します。

1. 地球温暖化 CO_2削減

2. IT化によるエネルギー消費増大

3. エネルギー効率向上

---インバータ、電源効率、LED、HEV

4. 再生可能エネルギー開発

---太陽光、風力発電


太陽光発電


風力発電


EV／HEVモータ駆動


LED電球


ACサーボ

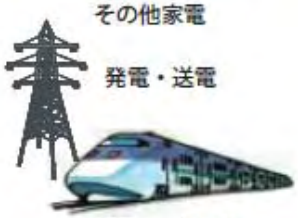

インバータ


洗濯機


冷蔵庫


エアコン


その他家電

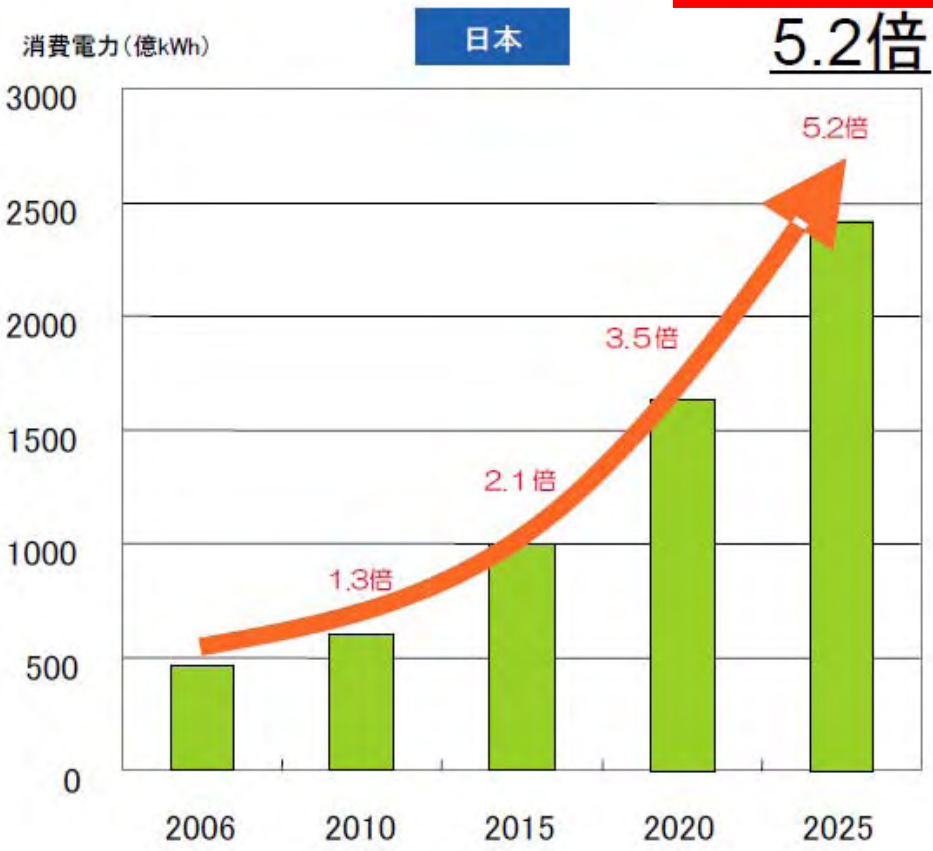

発電・送電

電鉄モータ駆動

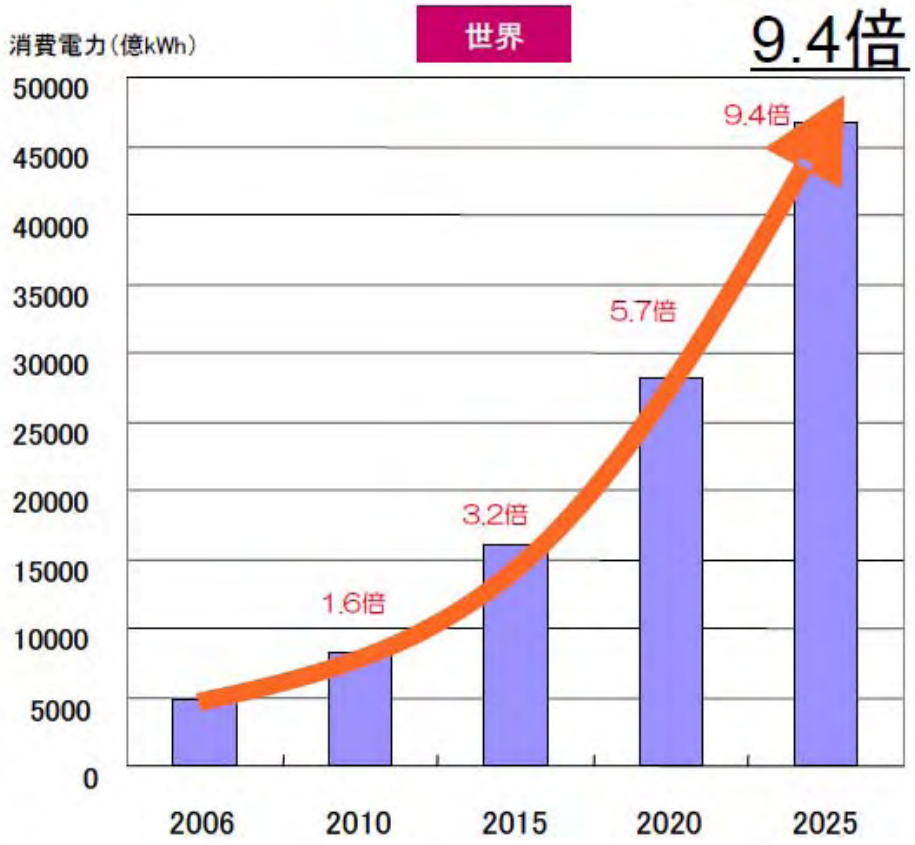
ＩＴ化でエネルギー消費増大

○ 情報化社会に伴うIT機器・システムの消費電力量の急増は、世界全体の課題。先進国に加えてBRICs等の発展により、世界のIT機器の普及は急増、**2025年には現在の9倍**（世界の総発電量の15%超、全エネルギー消費量の約6%）に達する恐れがある。

（国内総発電量の20%）

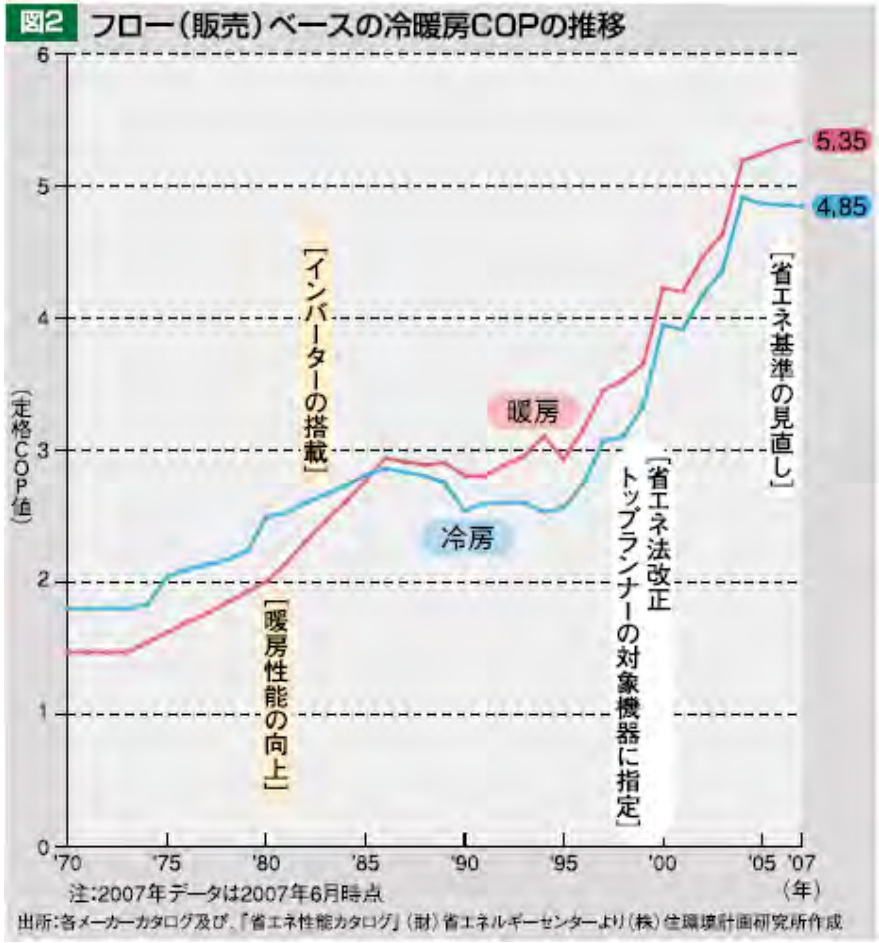


（世界総発電量の15%）



（出所）経済産業省/グリーンIT推進協議会試算(2008)

インバータの効率推移



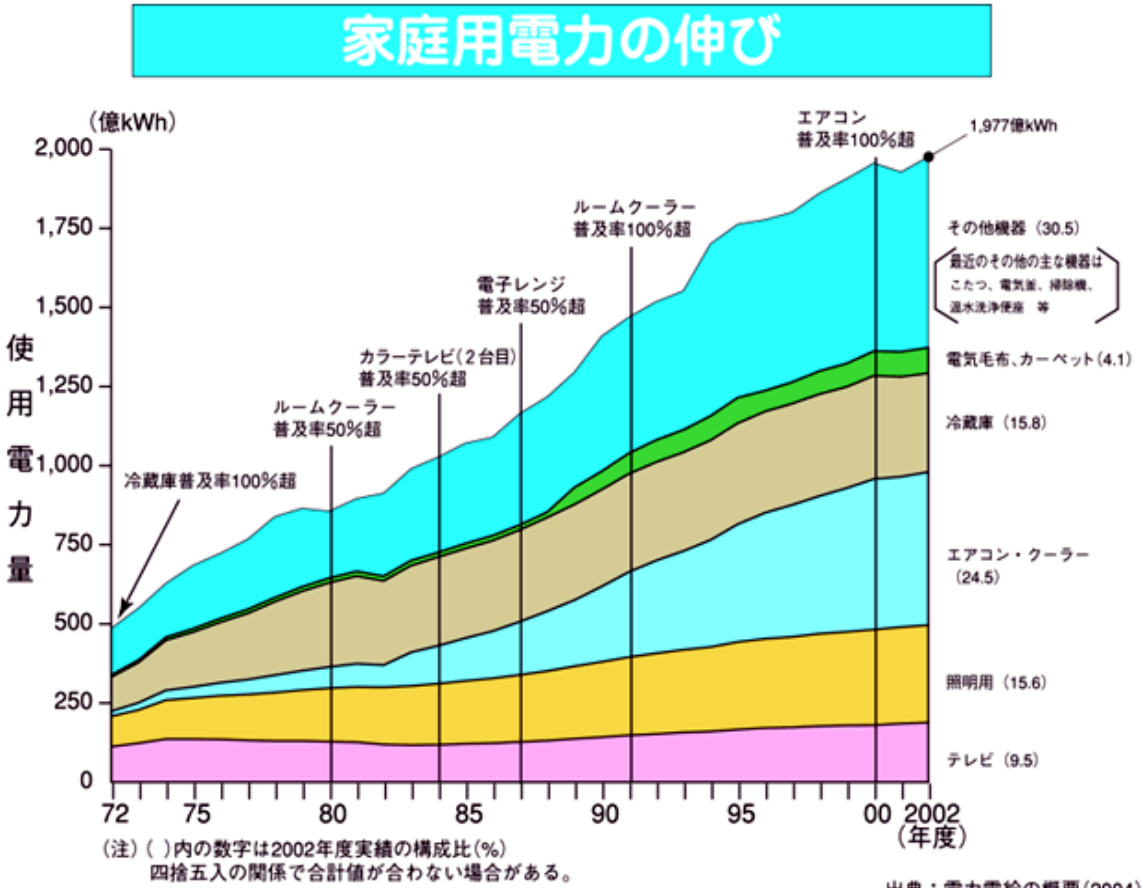
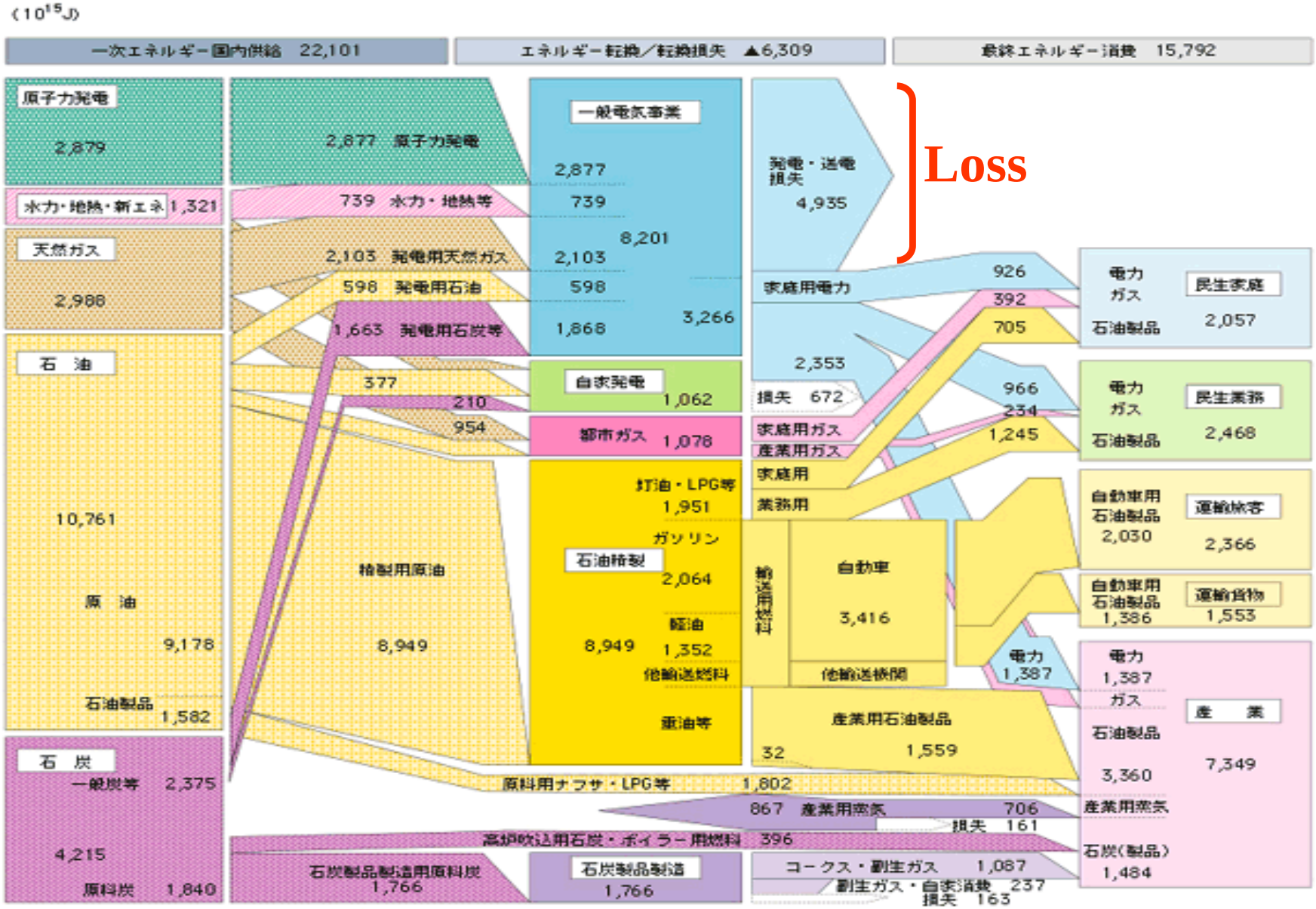


図1 家庭用電力の伸び

提供:(財)日本原子力文化振興財団:「原子力」図面集-2007年版-(2007.2)(同CD－ROM)



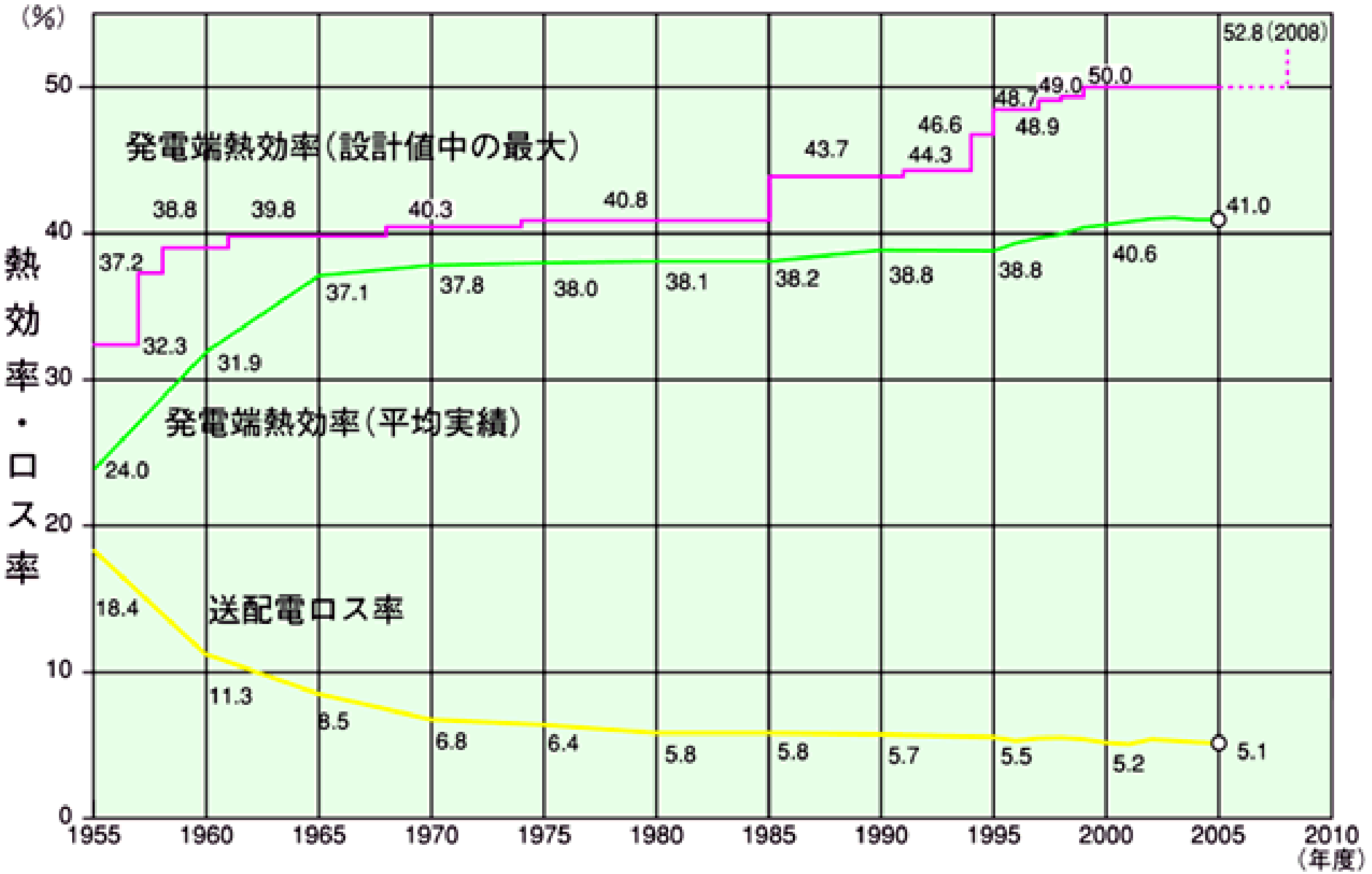
資料：資源エネルギー庁「総合エネルギー統計」

注）・単位は10^{15}J（ペタジュール）

図2　日本のエネルギー・フロー（2001年度）

提供: 経済産業省: エネルギー白書　2004年版、ぎょうせい（2004年6月）

火力発電設備の熱効率(高位発熱量)・送配電ロス率の推移

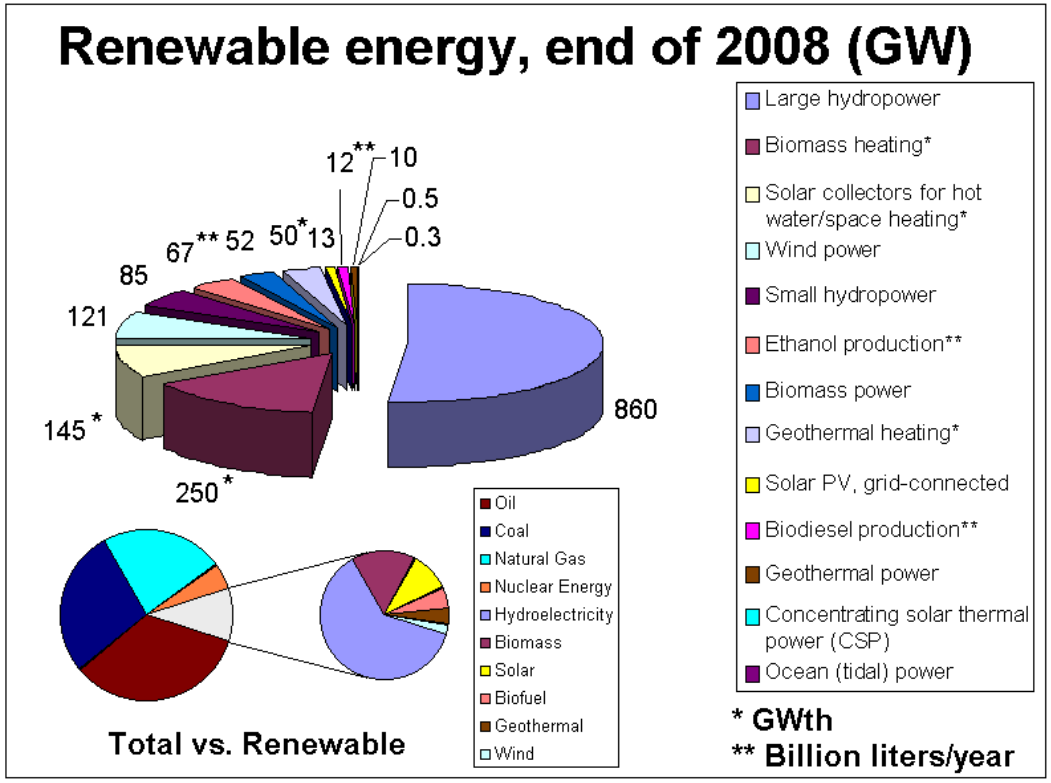


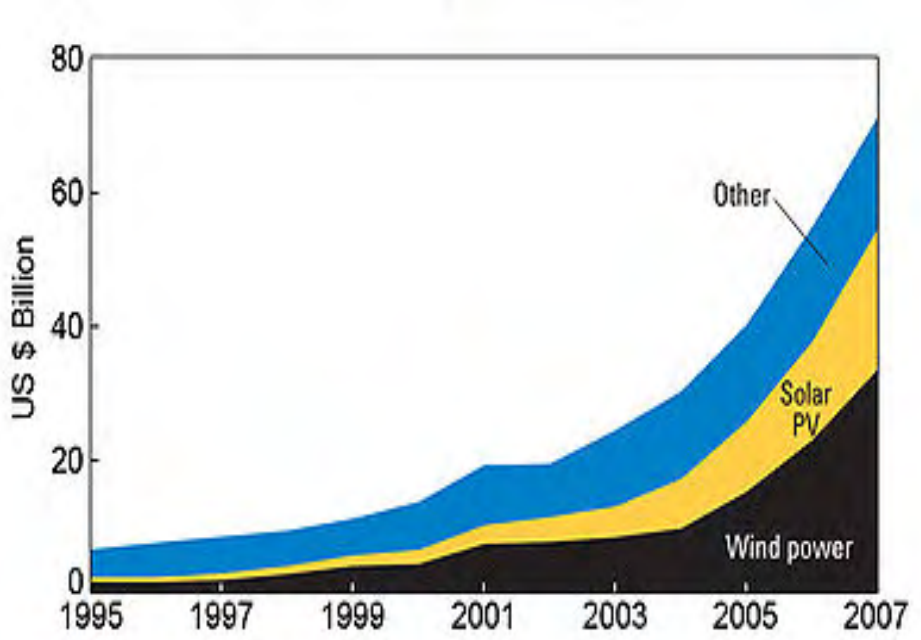
出典:電気事業便覧(平成18年版) 他

図　火力発電設備の効率と送配電ロスの推移

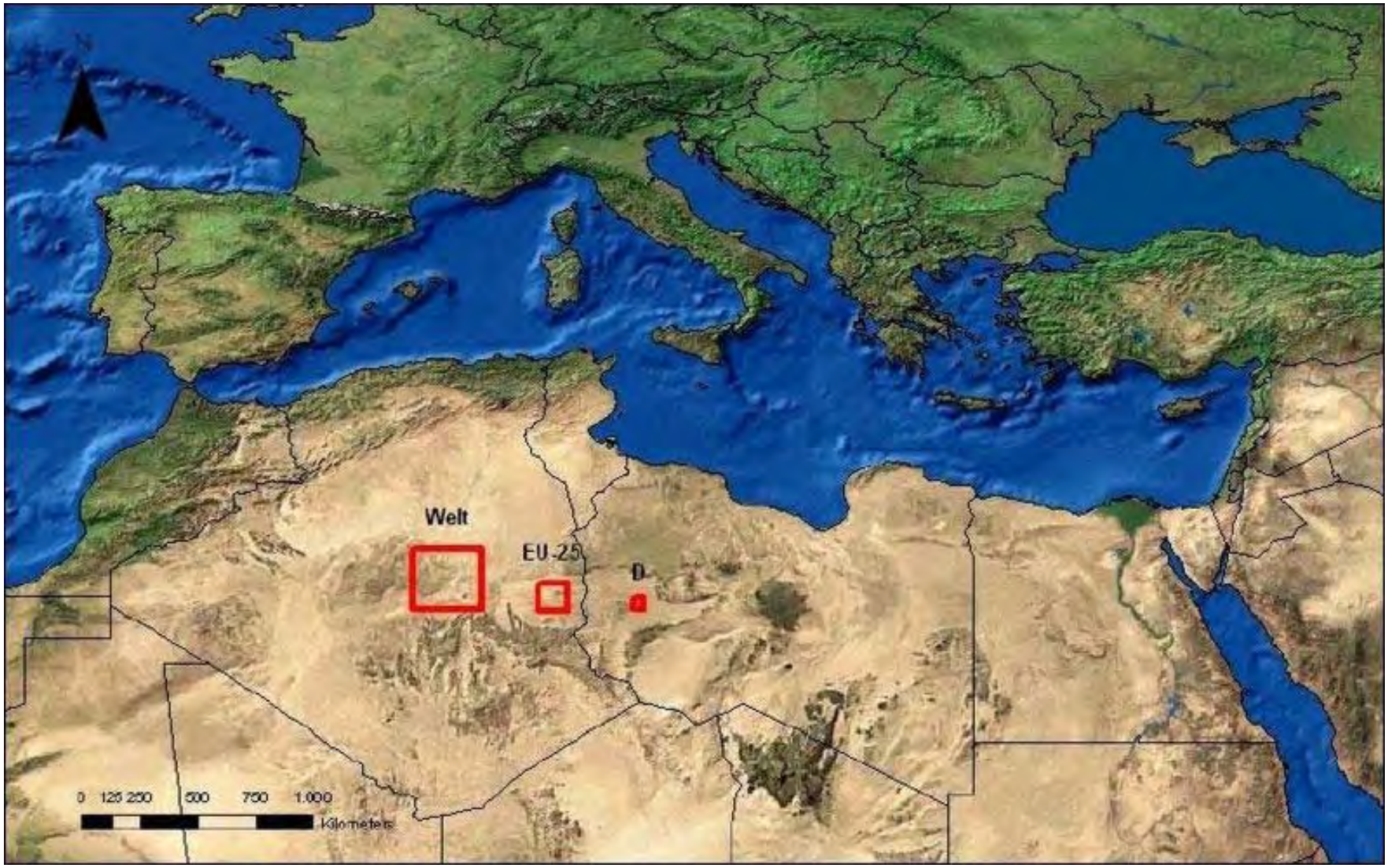
提供:(財)日本原子力文化振興財団:「原子力」図面集-2007年版-(2007.2)(同CD－ROM)

Renewable Energy



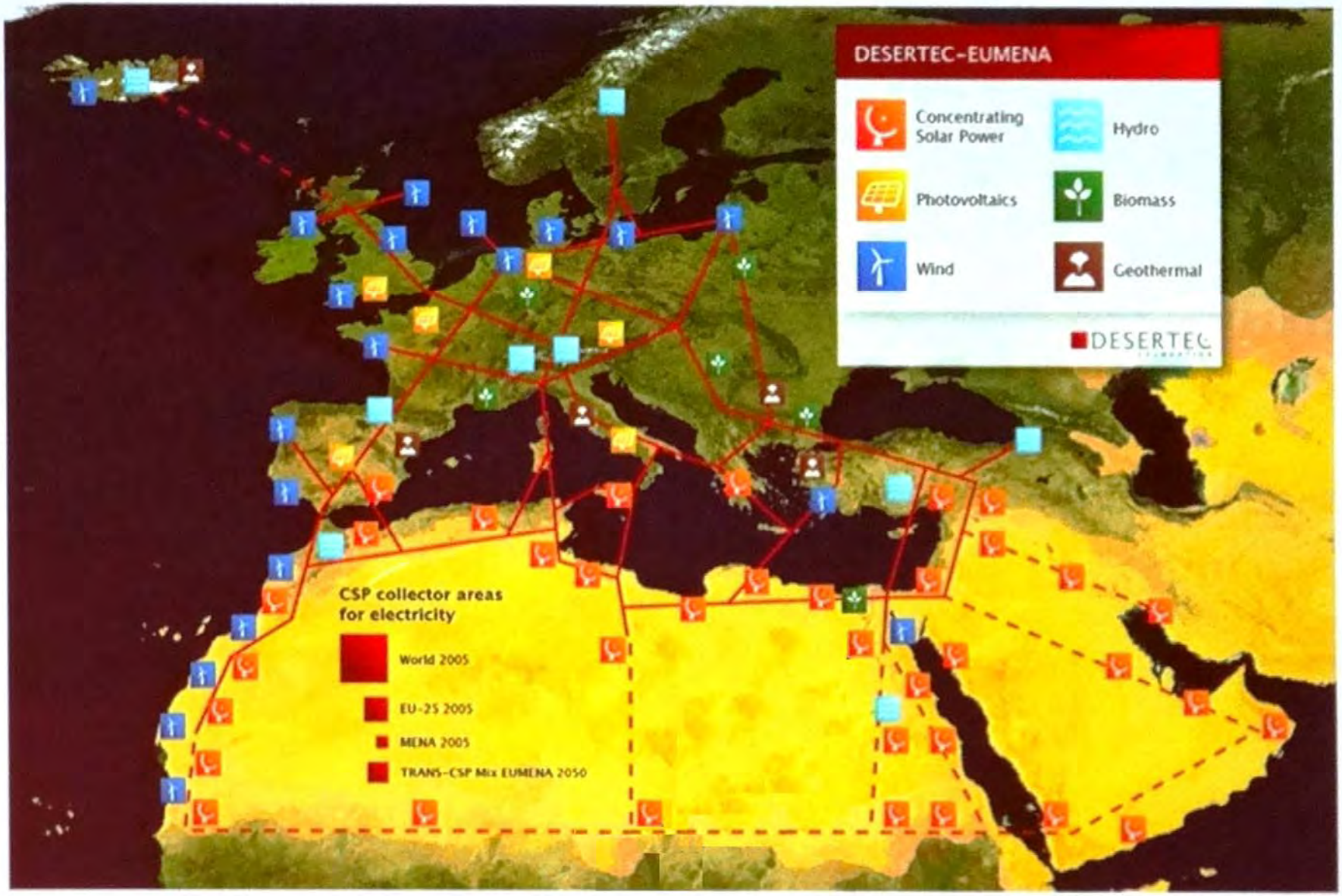


サハラ砂漠の6％の太陽光発電で全世界がまかなえる!!



ドイツ、EU25カ国および全世界の需要と等しい電力を太陽エネルギーで発電するのに必要な面積

Desertec and Seatec Concept



Source: www.desertec.org

Siデバイス性能限界 →　システムの変革

照明	蛍光灯	→	LED
車	ガソリン	→	HEV, EV
発電	石油	→	太陽光、風力
送電	従来	→	スマートグリッド 直流給電

システム変革・回路変革の時代

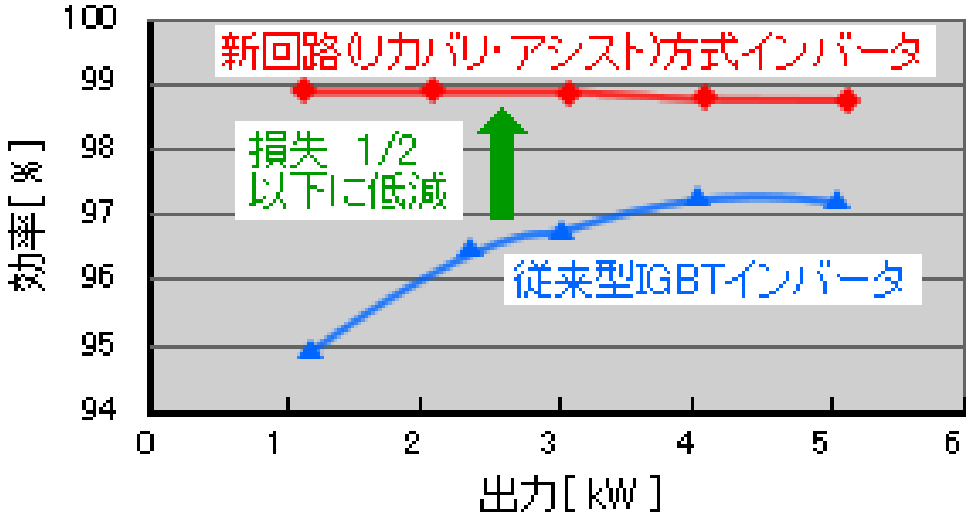


図4 インバータ効率実測結果

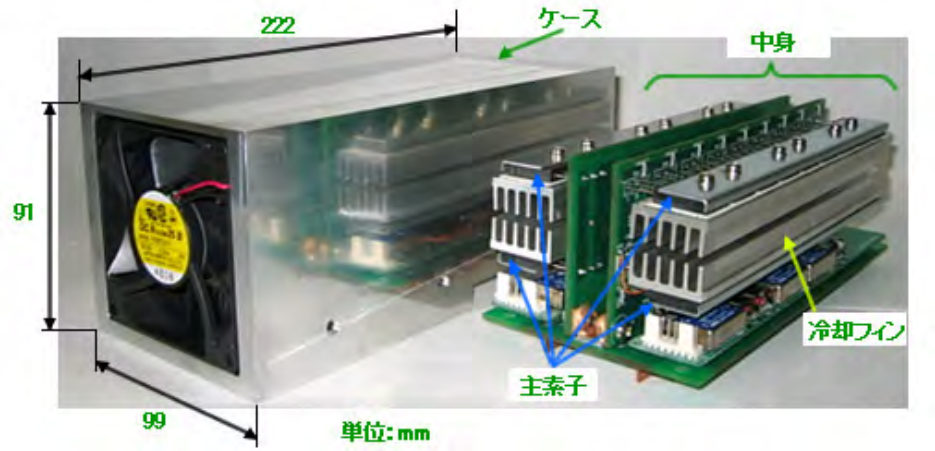


図5 20kWの試作インバータの概観

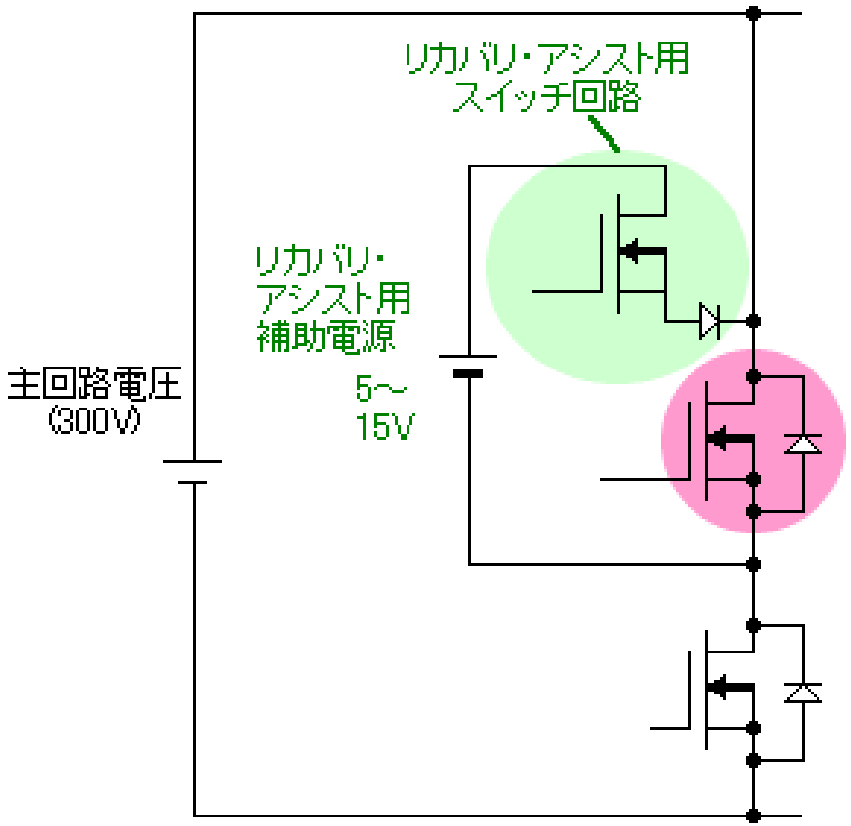


図3 新方式「リカバリ・アシスト」回路

東芝電力社会システム技術開発センター
http://www3.toshiba.co.jp/power/pic/secret/inverter.htm

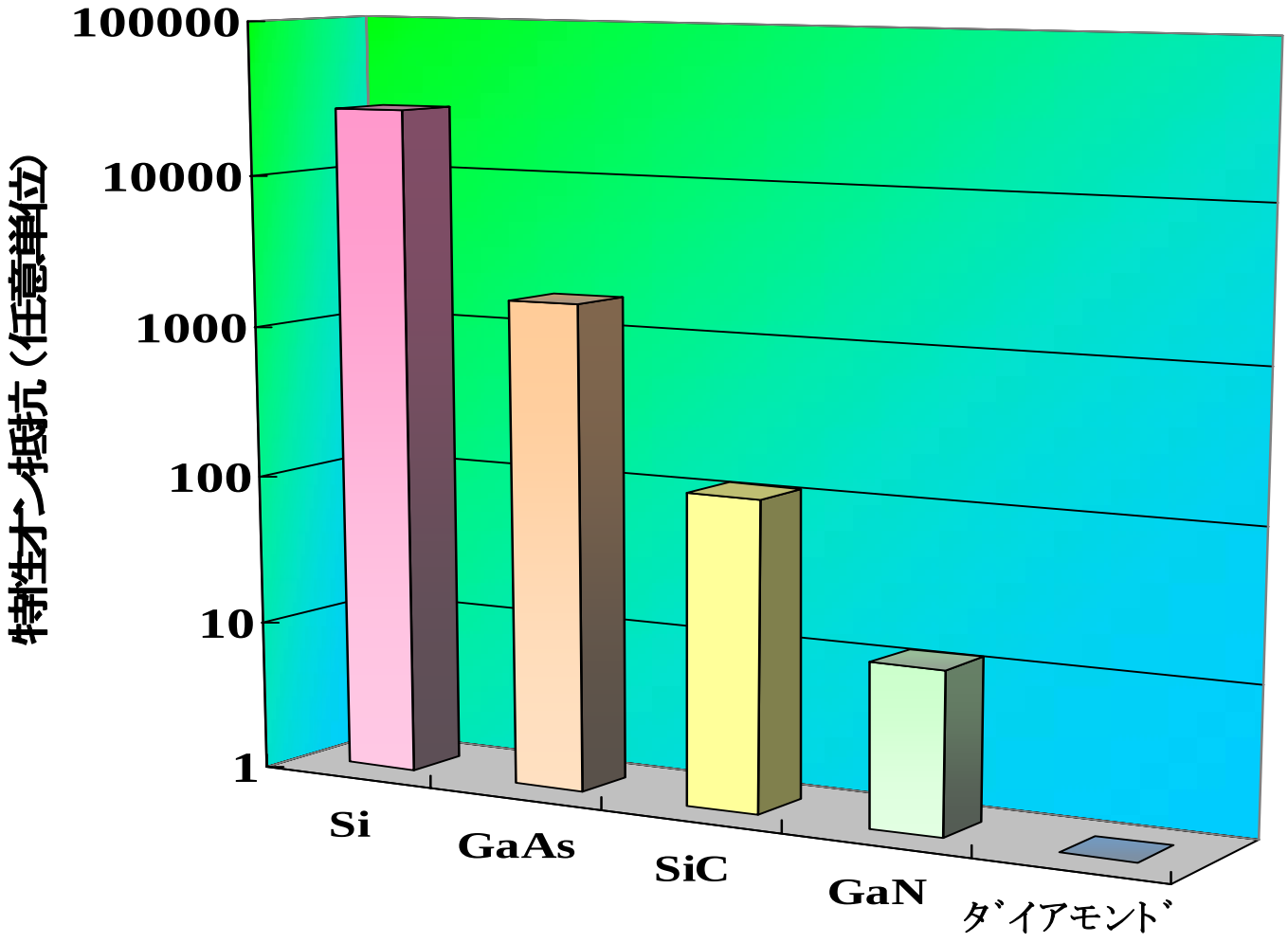
システム変革・回路変革の時代

韓国Seoul Semiconductor，直流変換回路や駆動回路が不要な白色LEDで75lm/W達成

図1　今回の白色LED

電源電圧が50V，光束は60lmで消費電力は0.8Wであり，75lm/Wの効率を達成した。パッケージ寸法は，平面方向が7mm角，高さ方向は2.95mmと小型化した。色温度は3000K，演色性指数（CRI）は85以上である。

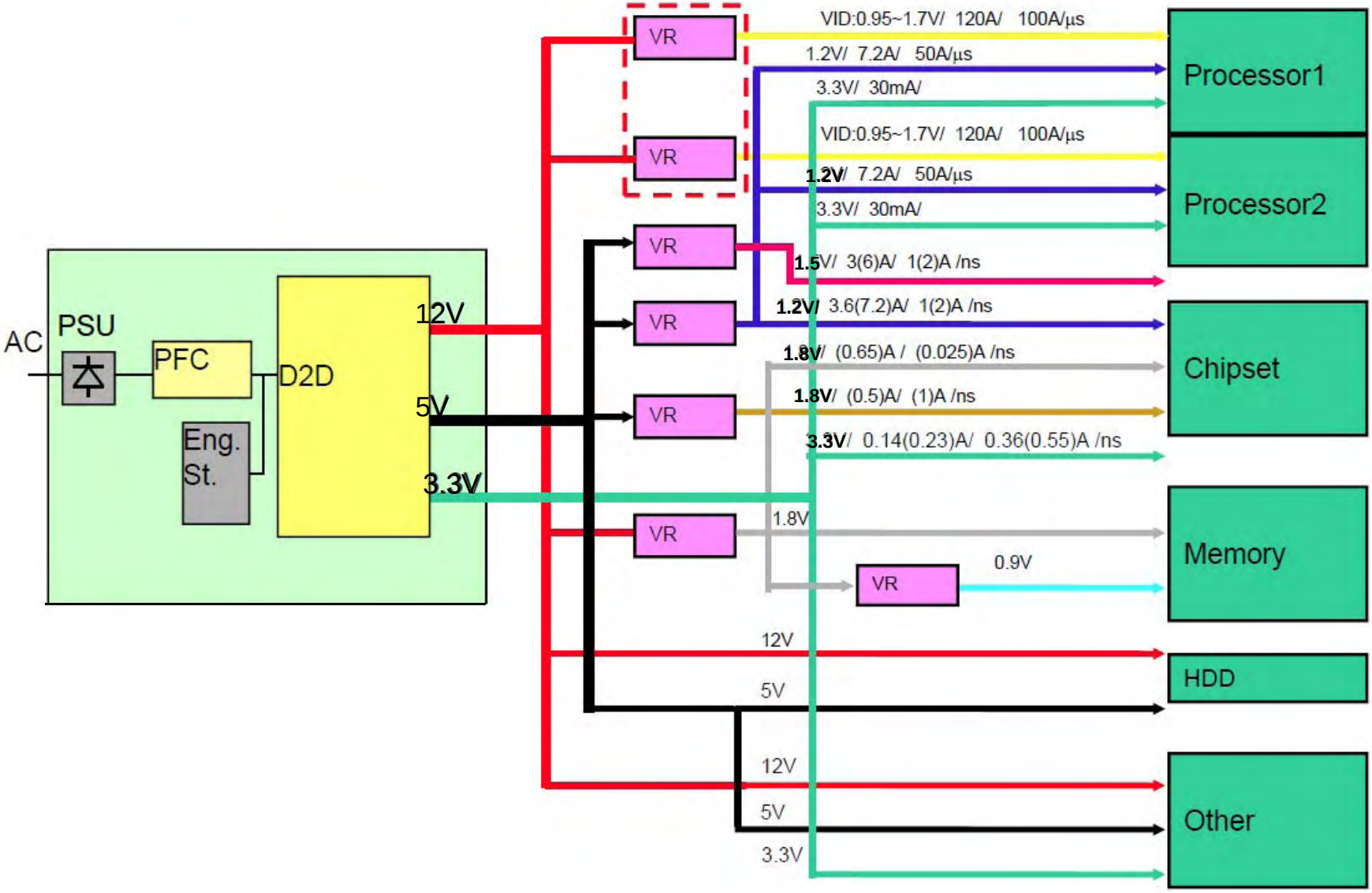
ワイドバンドギャップ半導体による低損失化



多種の電源電圧→電源の効率向上!!

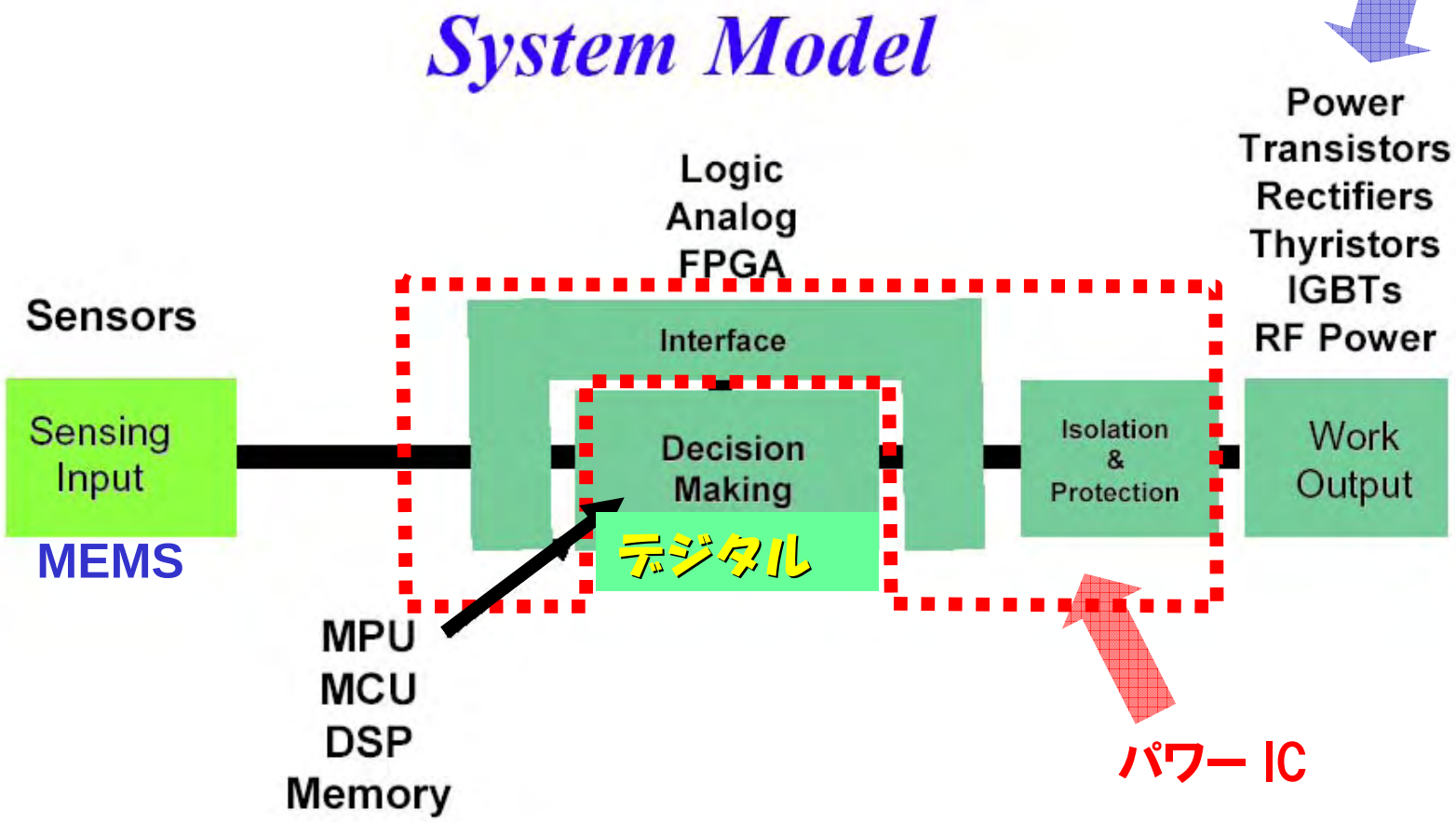
Present Server Power Architecture

F. Lee PWRSoC'08



パワーICの守備領域

パワー素子



MOTOROLA intelligence everywhere

digital dna

IT化電子化で拡大するPower ICの役割

デジタル家電

無線

RFMEMS

自動車

MEMS

アクチュエータ

センサー

デジタルコア

モータ

入力

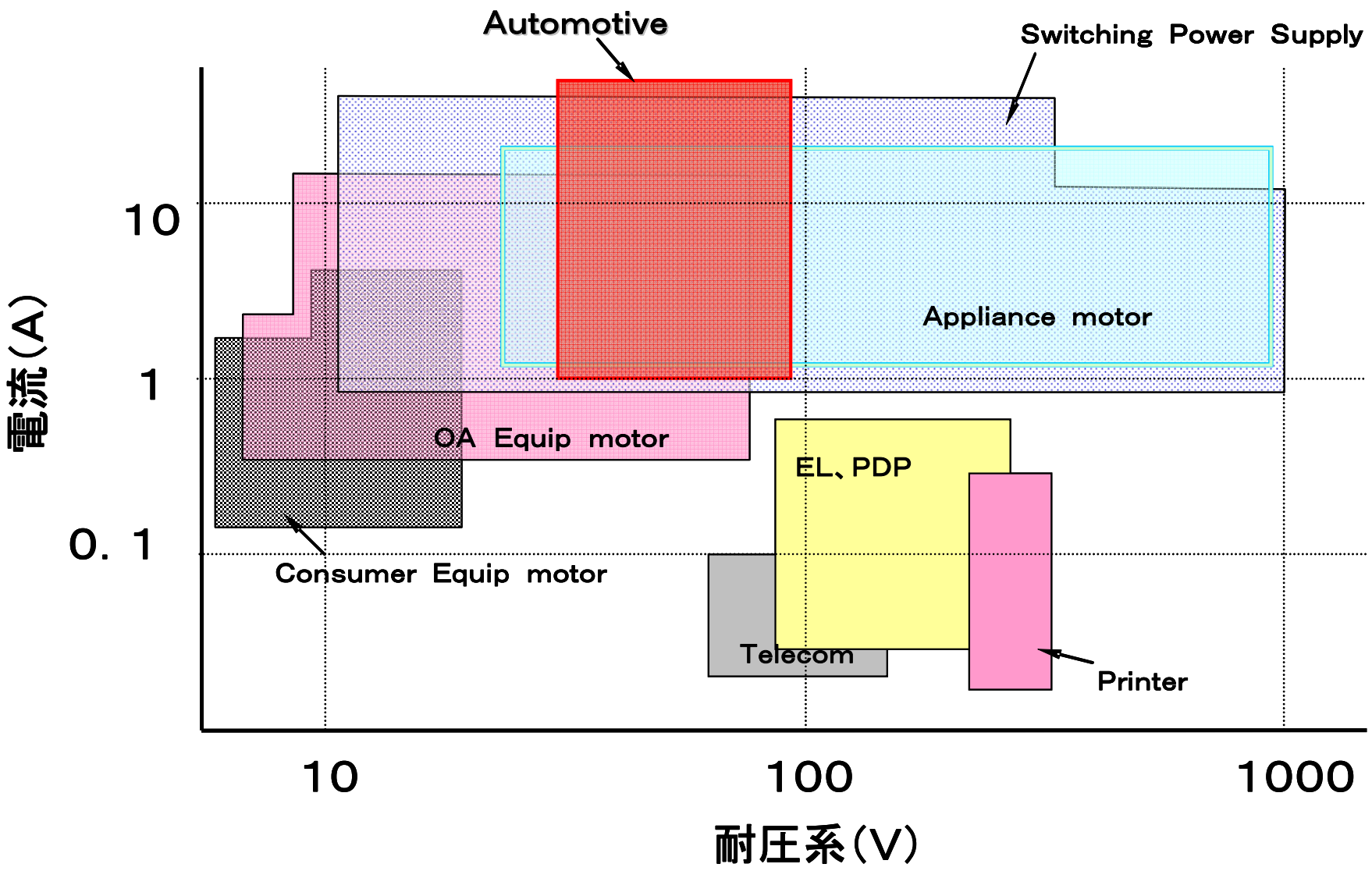
PSoC

Discrete
の領域

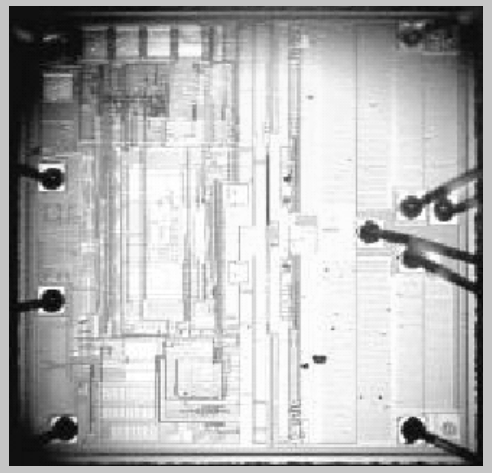
MEMS(L，C)

電源

パワーＩＣの応用


Automotive
Switching Power Supply
Appliance motor
OA Equip motor
EL、PDP
Consumer Equip motor
Telecom
Printer
10
1
0. 1
電流（A）
10
100
1000
耐圧系（V）

携帯機器、デジタル家電でパワーICが活躍



D級オーディオアンプ

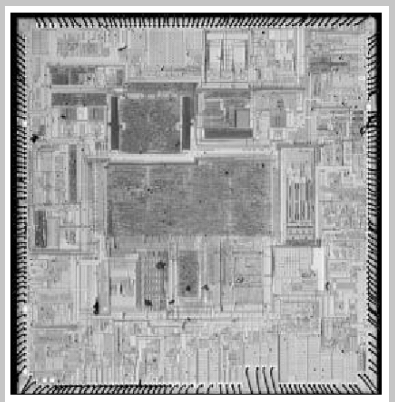
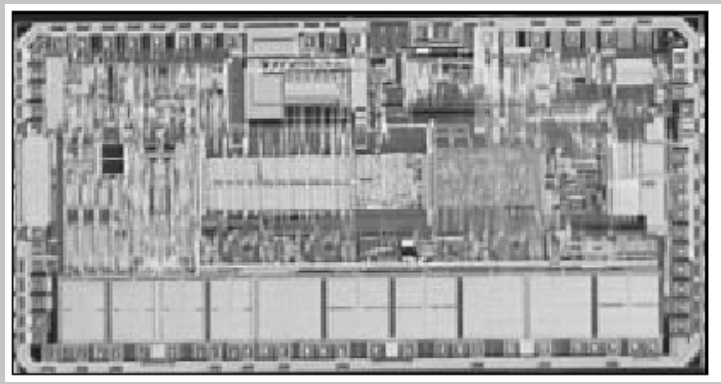


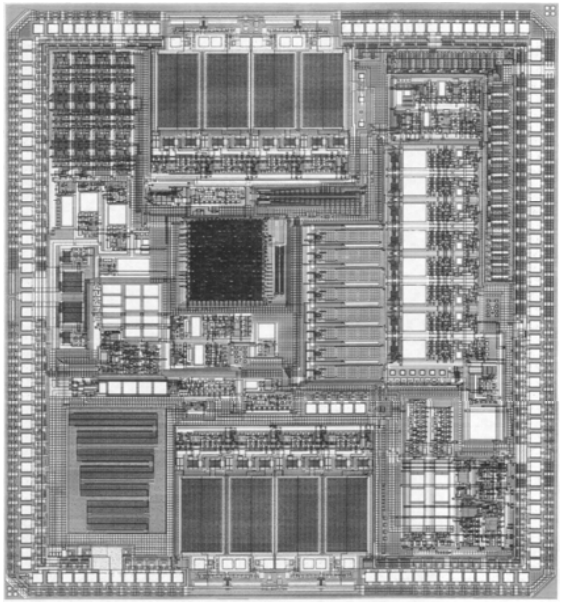
Figure 11 shows a system on chip level power management chip for wireless communications device.

バッテリーチャージャー
Voiceband CODEC
WCDMA & GSM baseband converters
オーディオアンプ
パワー周りをすべて集積化した
携帯電話パワーシステムLSI



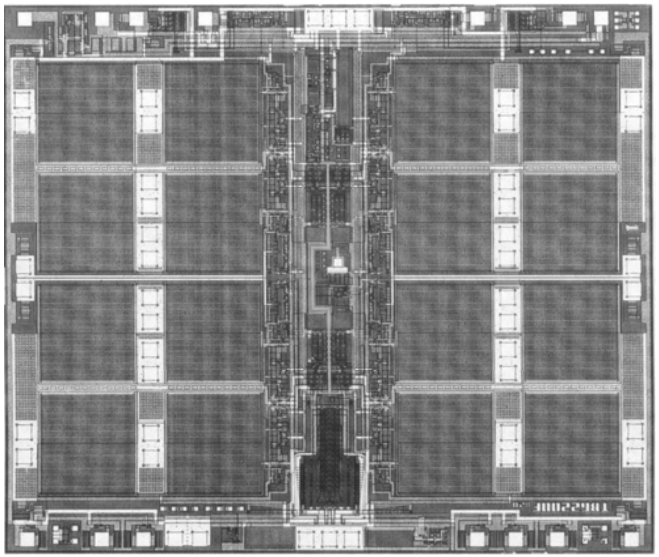
超小型モバイルHDD
モータードライバ

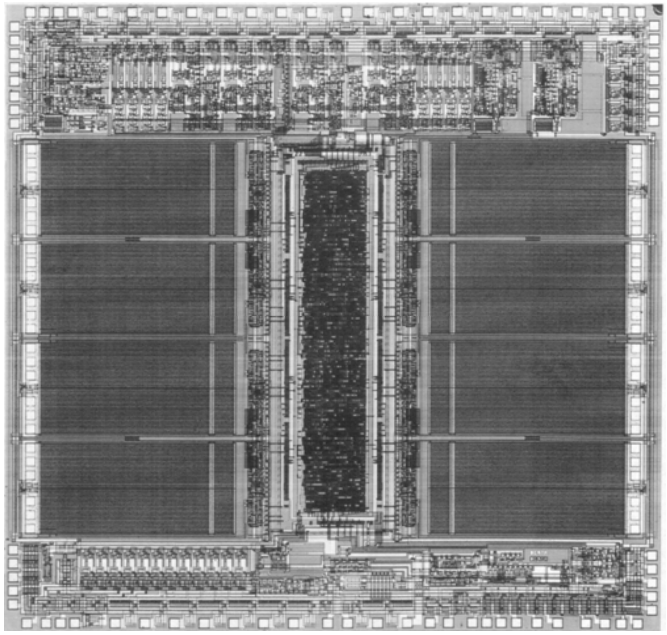
Low voltage Power ICs (BiCD) 2000



Engine control

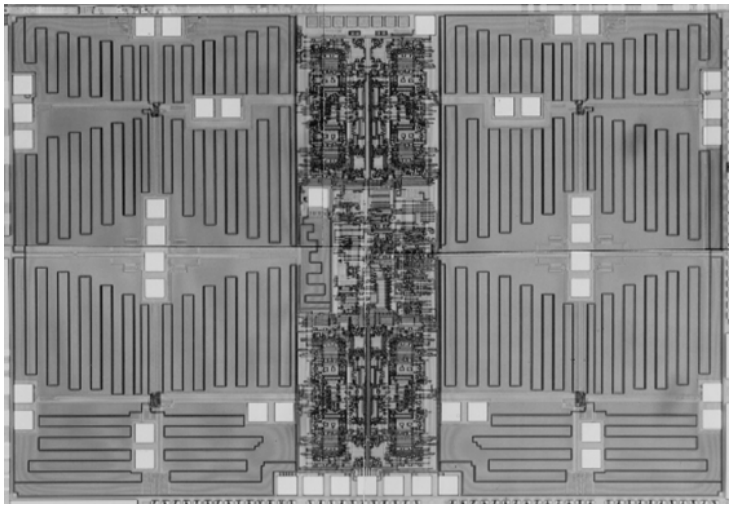
Stepping motor driver





ABS

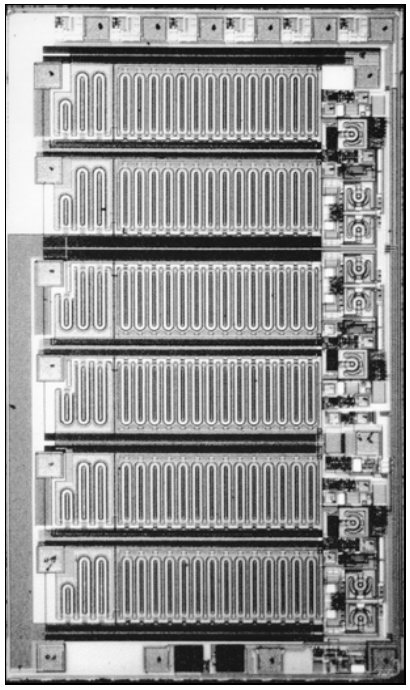
40W Audio amplifier



High Voltage Power ICs

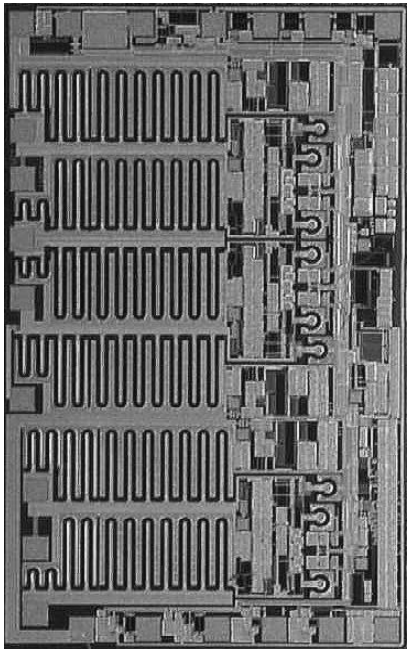
1 Chip Inverter ICs

500V,1A(1994)



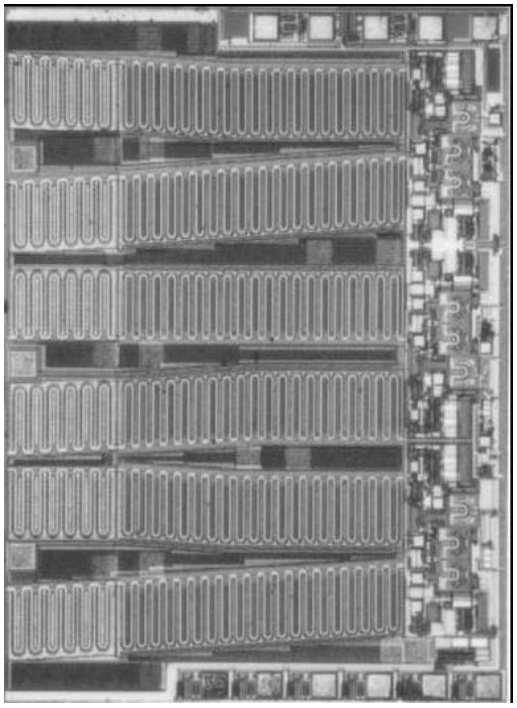
7 x 4.2
15μmSOI,
Trench Isolation,
1.5μm 5V BiCMOS

500V, 1A(2002)



6.6 x 4.1
15μmSOI
Trench Isolation,
2μm 30V CMOS Analog

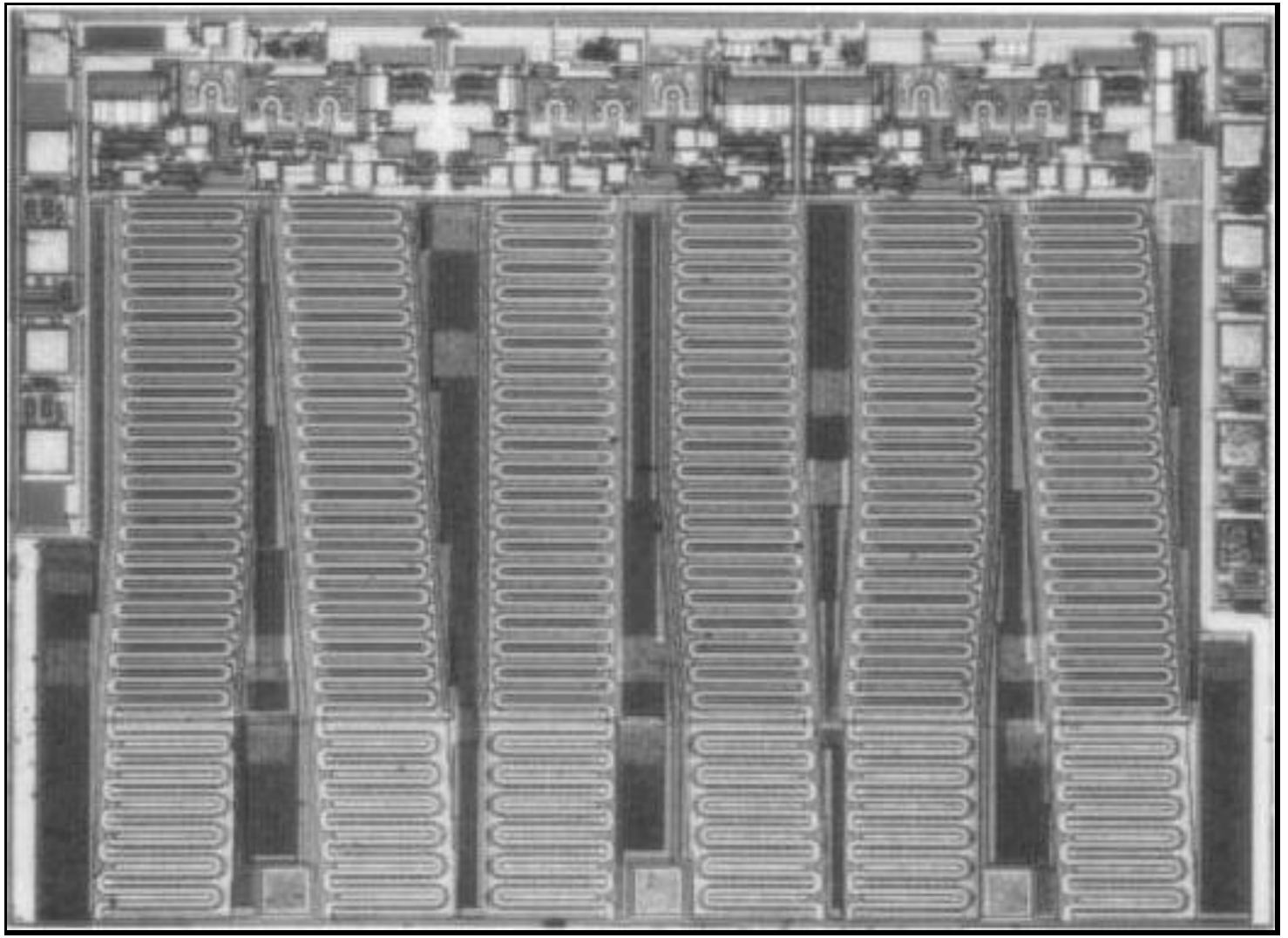
500V, 3A(1997)



7.1 x 5.2
15μmSOI,
Trench Isolation,
1.5μm 5V BiCMOS

500V/3A 1chip Inverter IC

1999



Highly Efficient Motor Control

Industry Motors

1 Chip Inverter

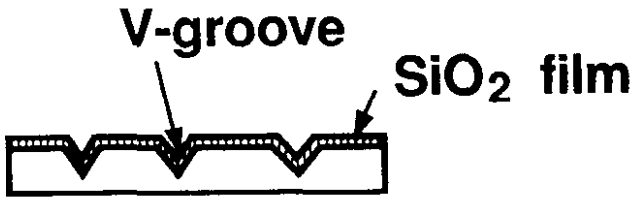
Refrigerators

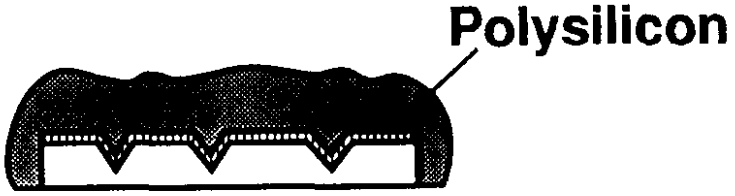
Air conditioner

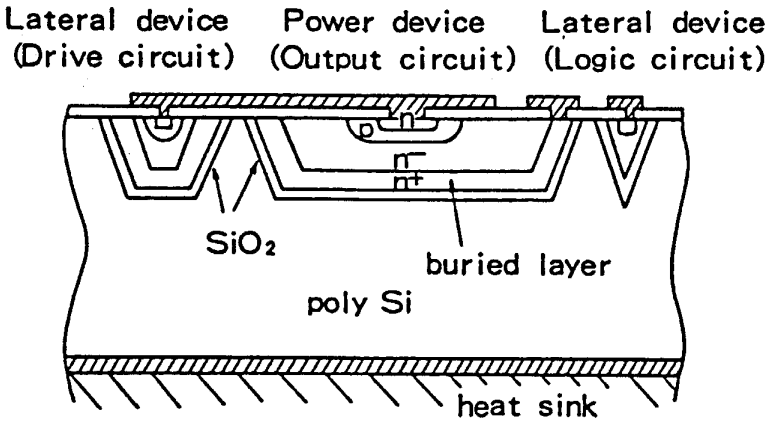
Washing Machine

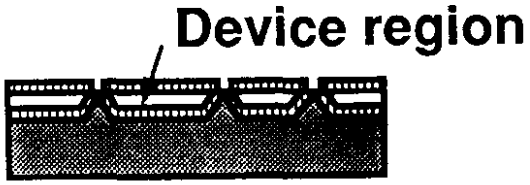
高耐圧SOIパワーＩＣ技術

•Dielectric Isolation (DI)
EPIC







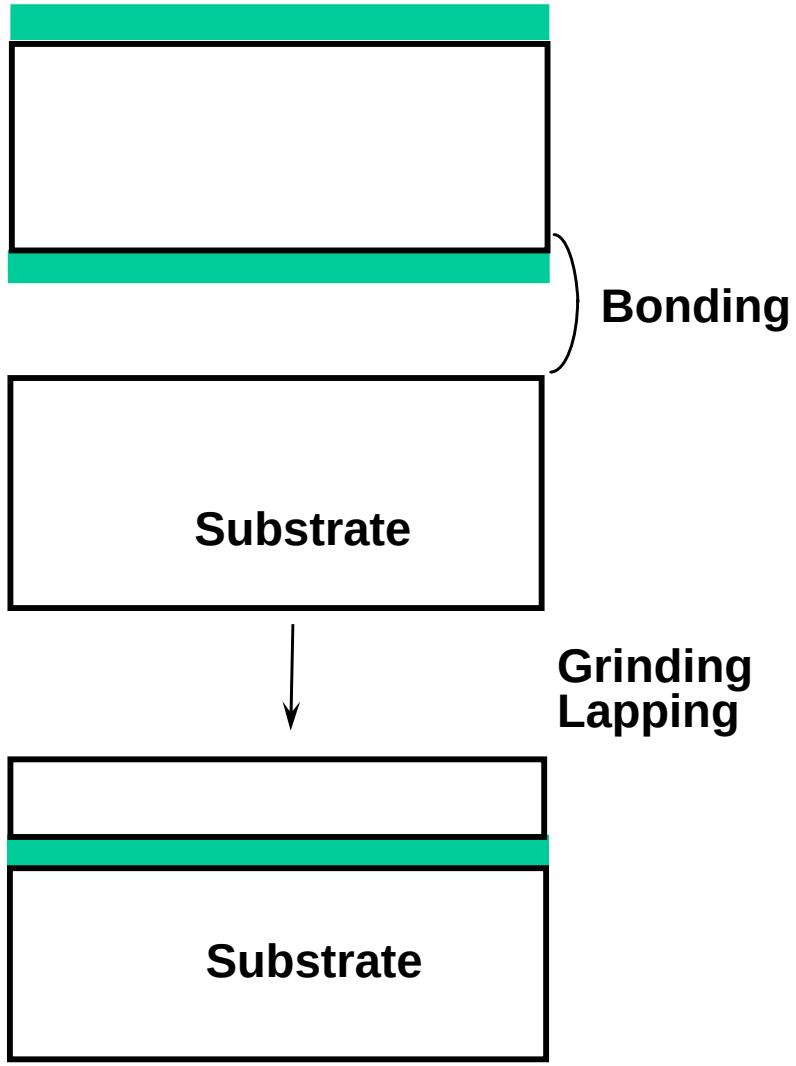


Dielectric Isolation

EPIC

Wafer Direct-Bonding (1986)

- **Low cost SOI wafers**
- **Large diameter (8 inches)**
- **Fine lithography**
- **High Voltage**

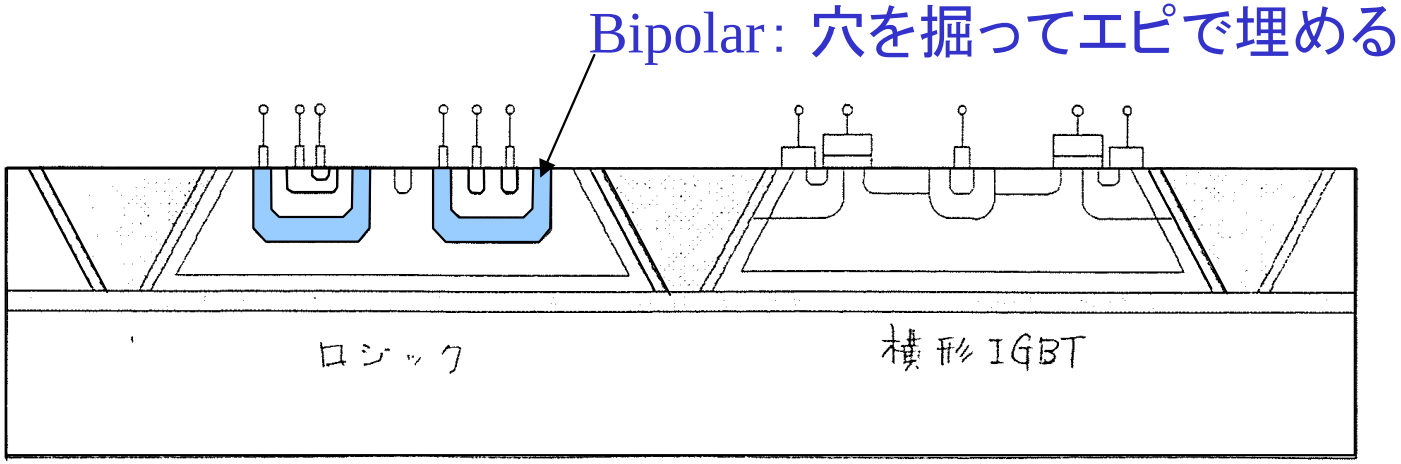


研究開発方針策定　@1986年12月

今後はパワーICが伸びる!!

ターゲット：インバータの１チップ集積化

第一Step： EPICの置き換え

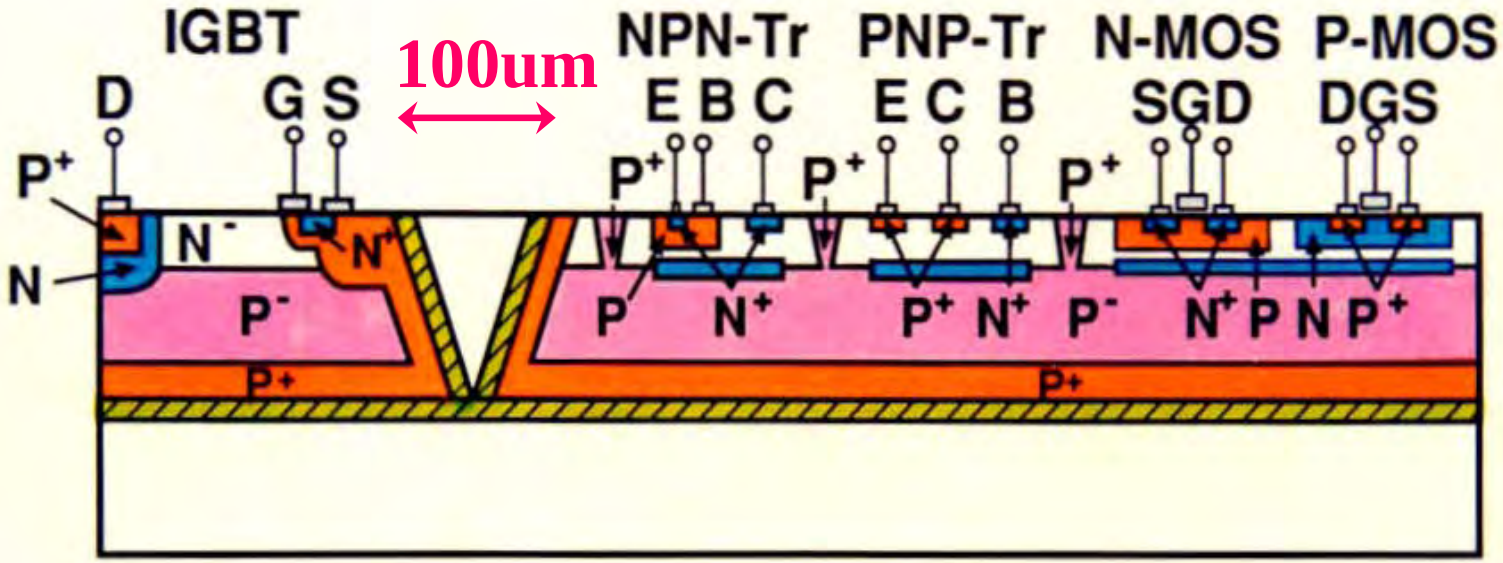


第二Step: 薄膜SOI

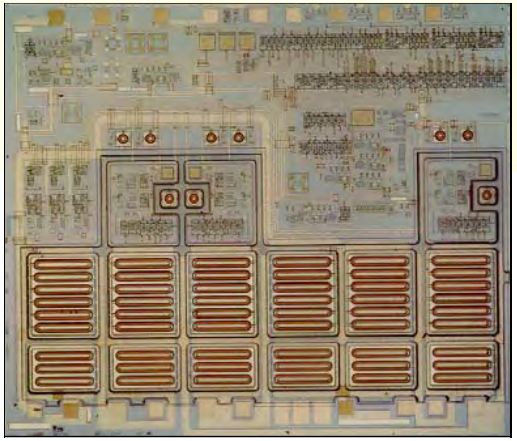
誘電体分離 power ICの課題

- High voltage large current devices
  - ***500V 5-10A***
  - ***CMOS compatible process***
  - ***No lifetime control***
- High voltage interconnection

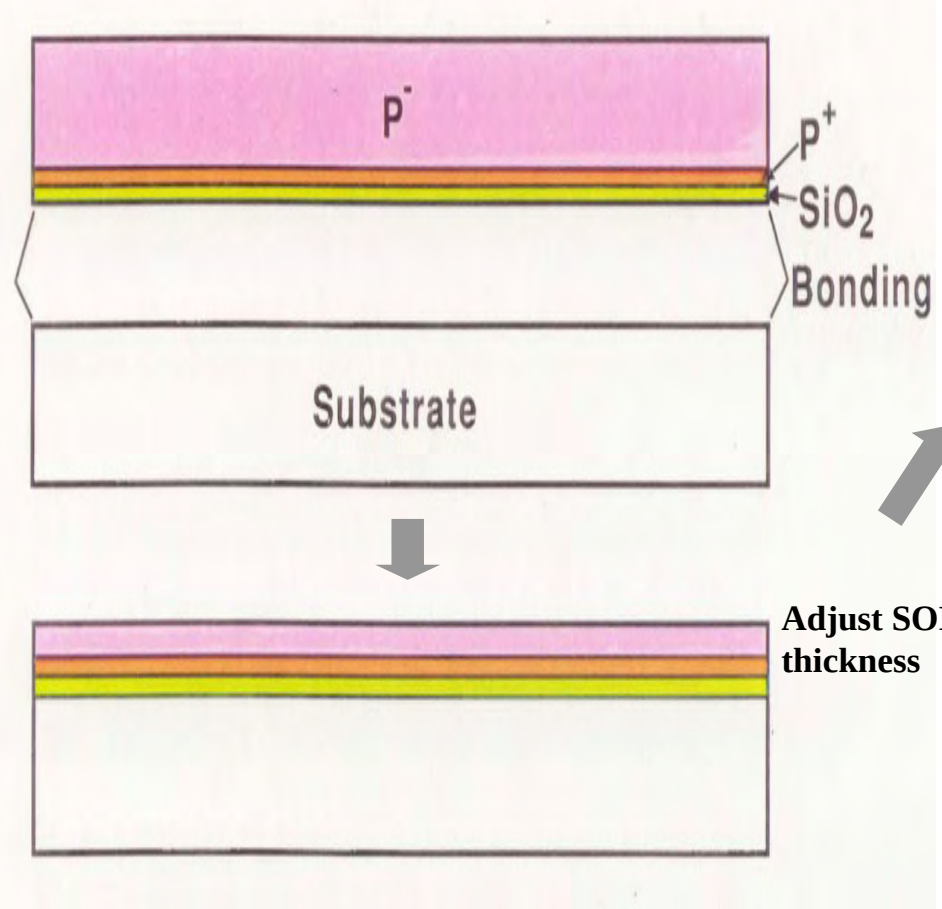
Cross Section of First Generation Chip in 1989

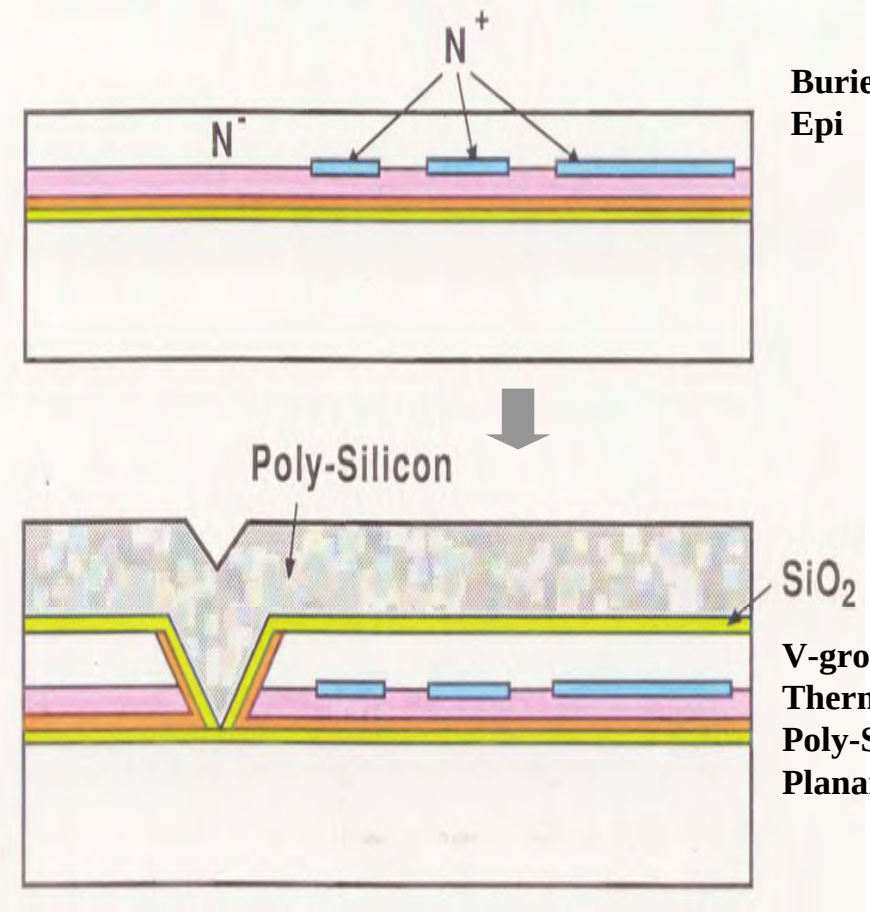


- DI for HV Devices
- JI for LV Devices



Fabrication process of 1st generation ICs





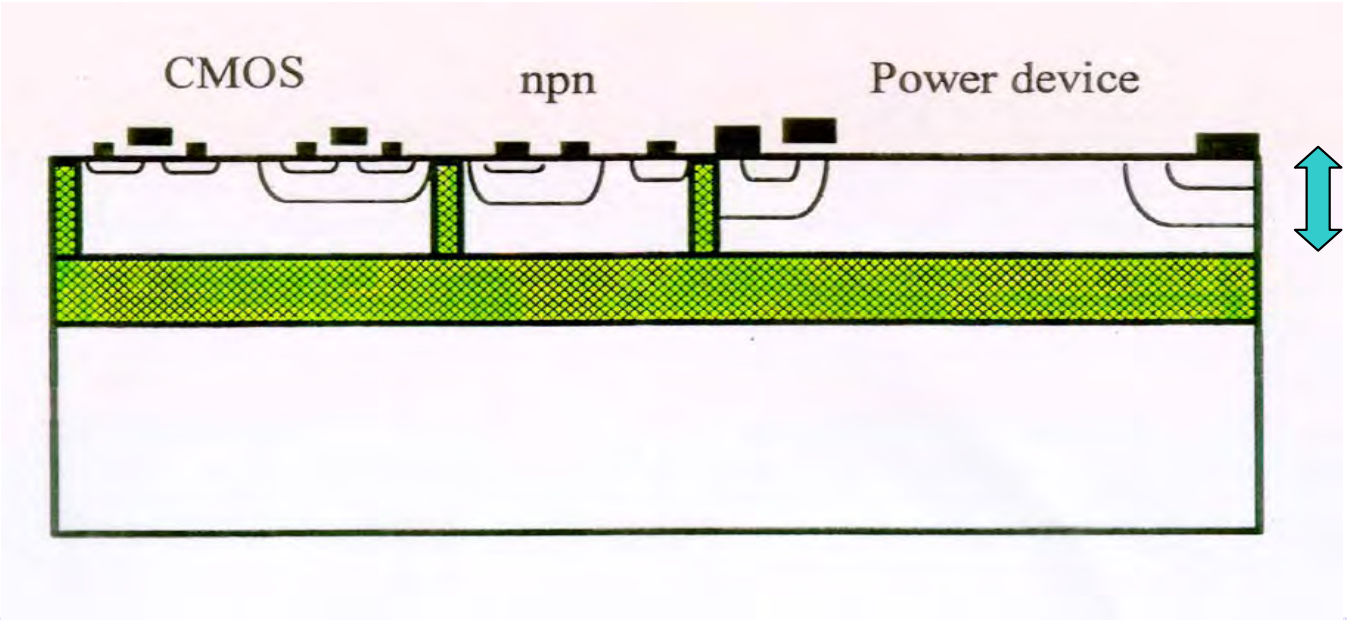
High Voltage SOI Technology

, proposed in 1990

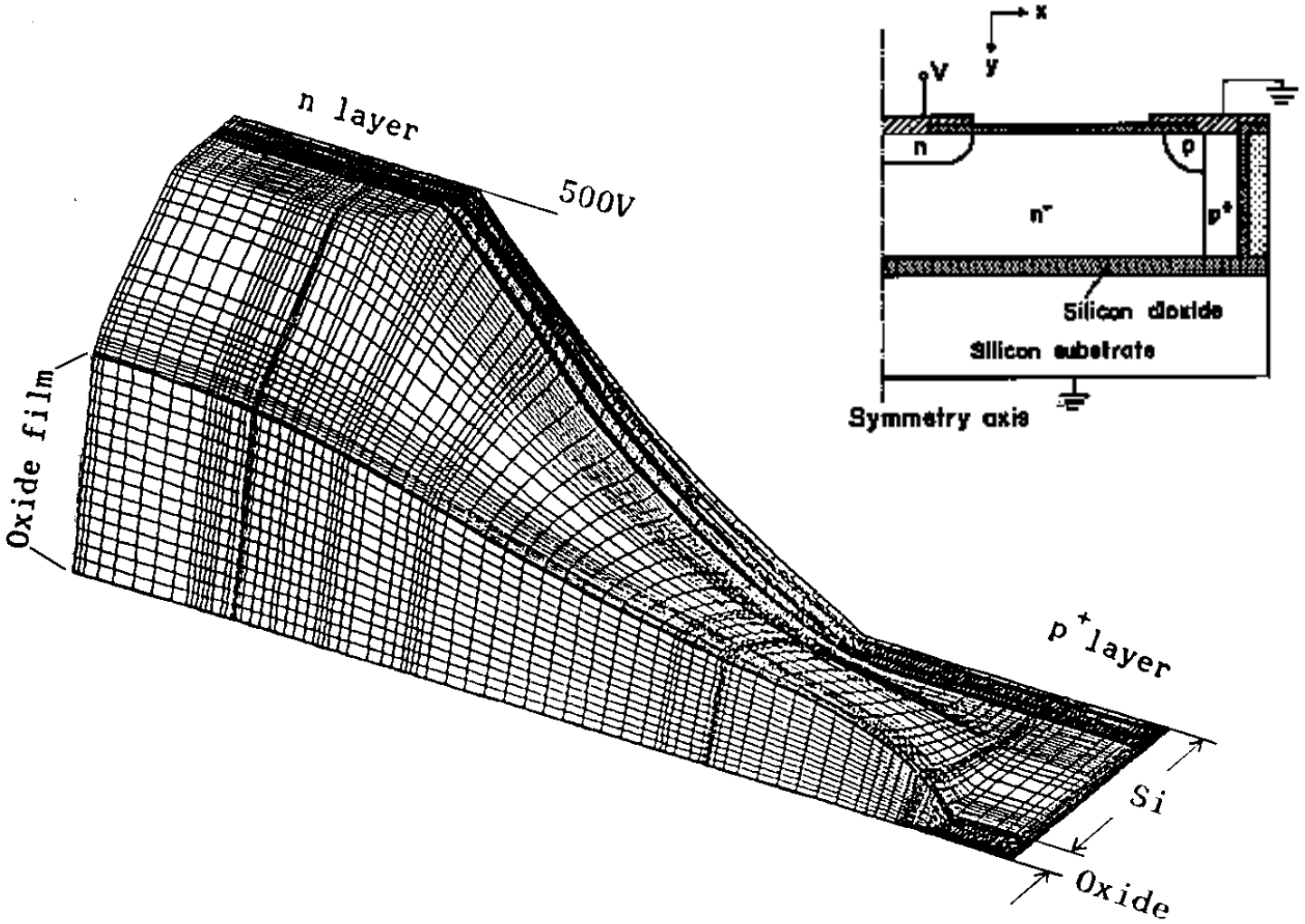
Trench Isolation & Thick buried Oxide

- ***High density device*** *integration by* ***trenches***
- ***High voltage device*** *is realized by* ***thick buried oxide****.*
- *Small wafer warpage & large diameter bonded wafers allows* ***fine lithography.***

従来の誘電体分離は酸化膜は分離の目的のみ
新SOI技術では酸化膜は素子の一部



20μmのシリコン層で500V　→トレンチ分離可能



A. Nakagawa ISPSD'90

高耐圧SOI技術の歴史

1. 最初の高耐圧SOIの論文　1990

A.Nakagawa et al., Proc. of ISPSD, pp.97-101 (1990)
"New 500V output device structure on silicon oxide film",

2. SOI Resurf　1991

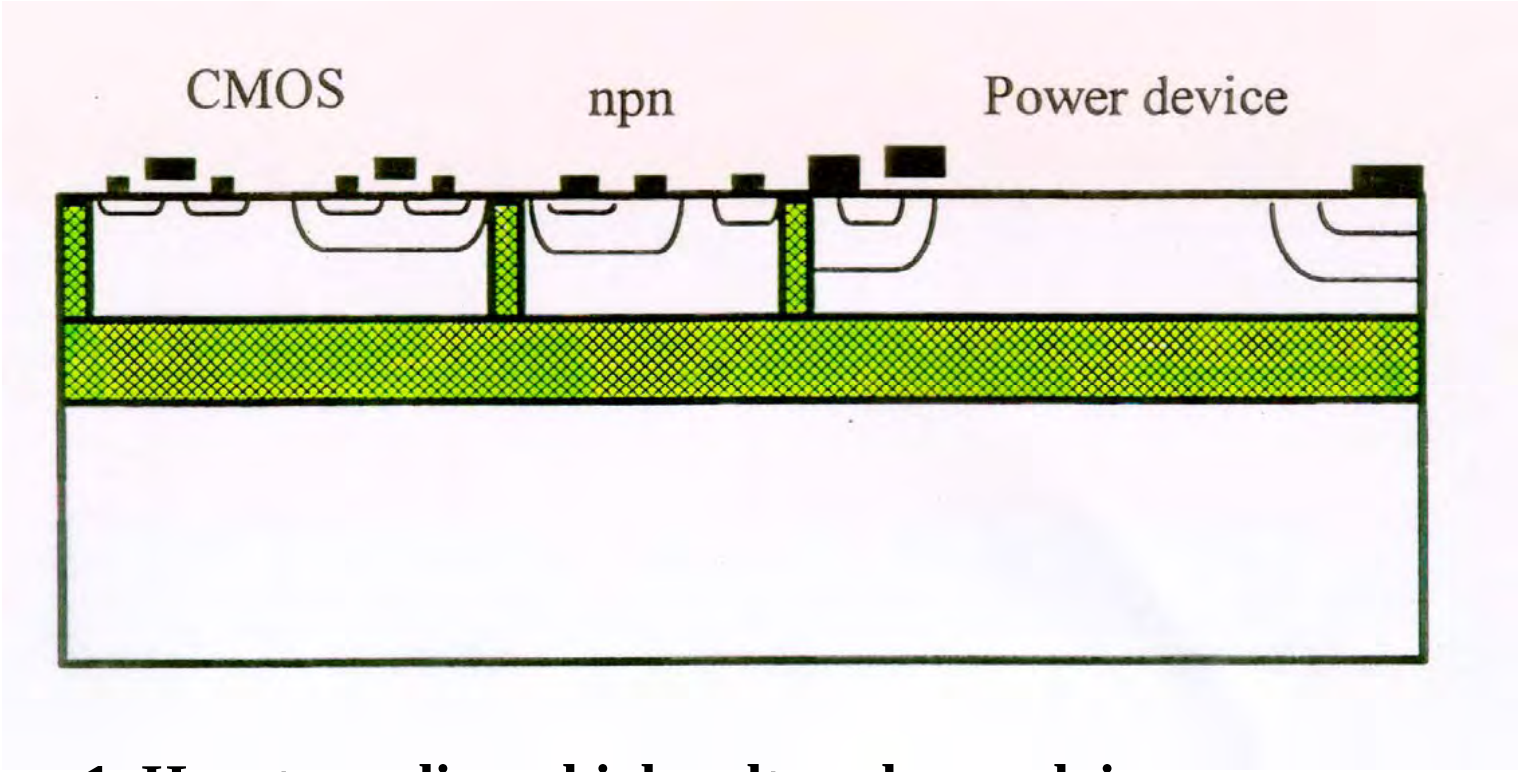
Y.S.Huang & B.J.Baliga
“Extention of Resurf Principle to Dielectrically Isolated Power Devices”

3. 薄膜高耐圧SOI　1991

S.Merchant et al., Proc. of ISPSD’91, p.31
“Realization of High Breakdown Voltage (>700V) in Thin SOI Devices”

Issues for High Voltage ICs on SOI

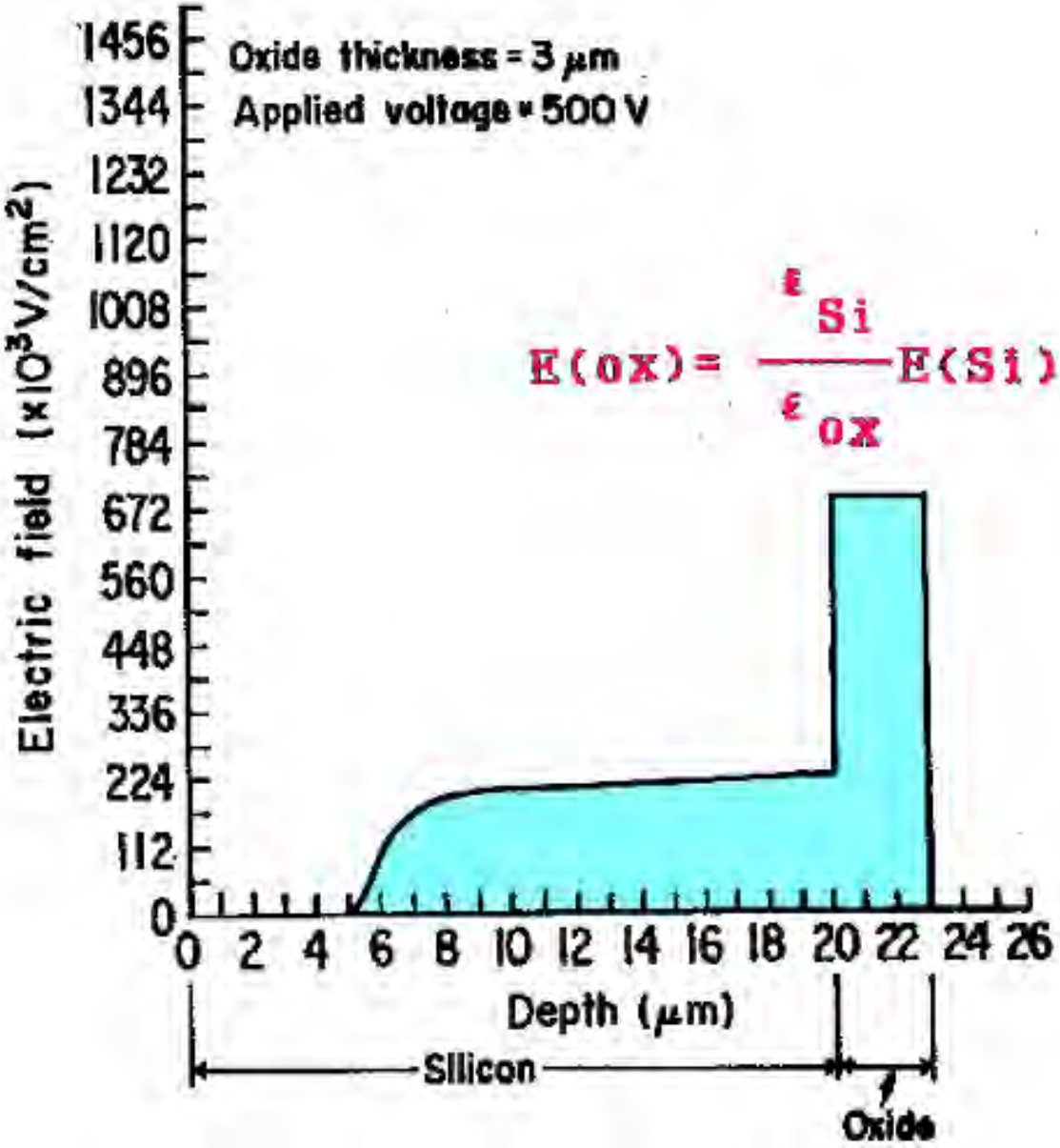
Combination of SOI and trenches



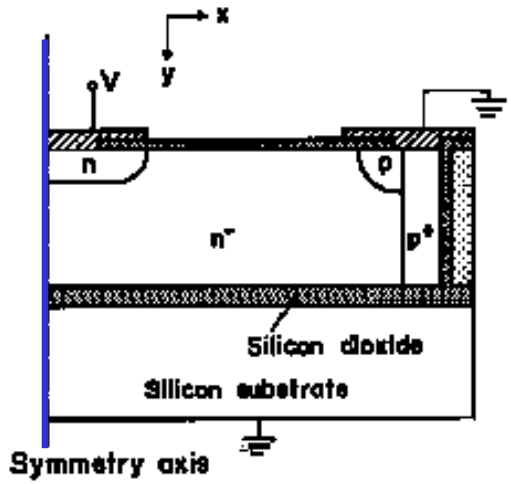
1. How to realize a high voltage by applying a large share of the voltage across the buried oxide

2. How to realize a large current device on a thin SOI

埋め込み酸化膜に電圧を負担させる



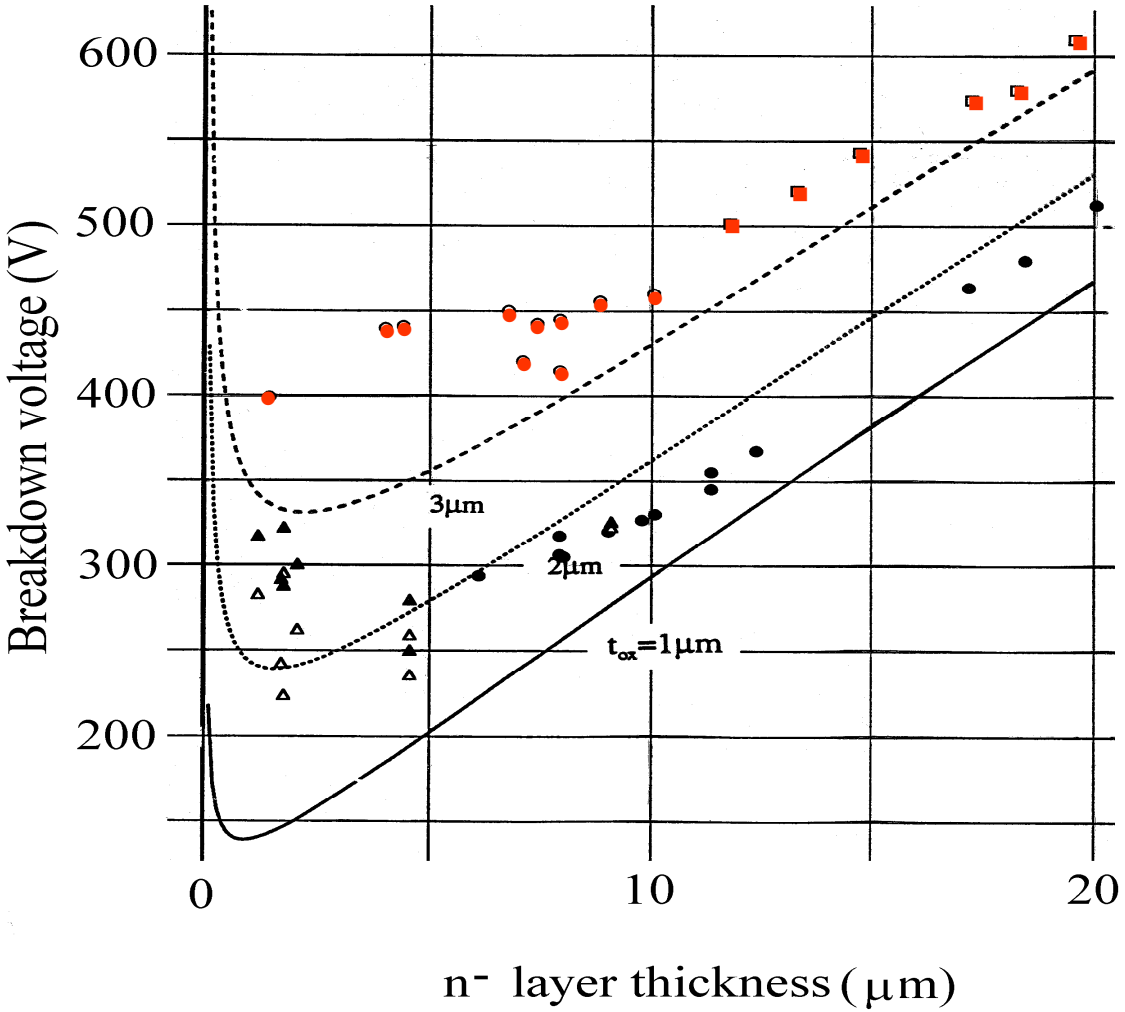
$$E(ox) = \frac{\varepsilon_{Si}}{\varepsilon_{ox}} E(Si)$$

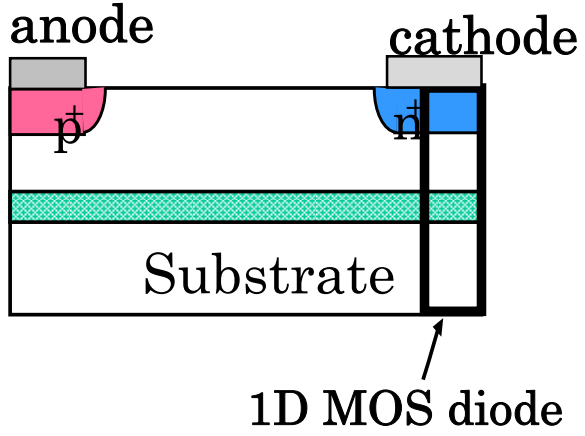


A. Nakagawa ISPSD' 90

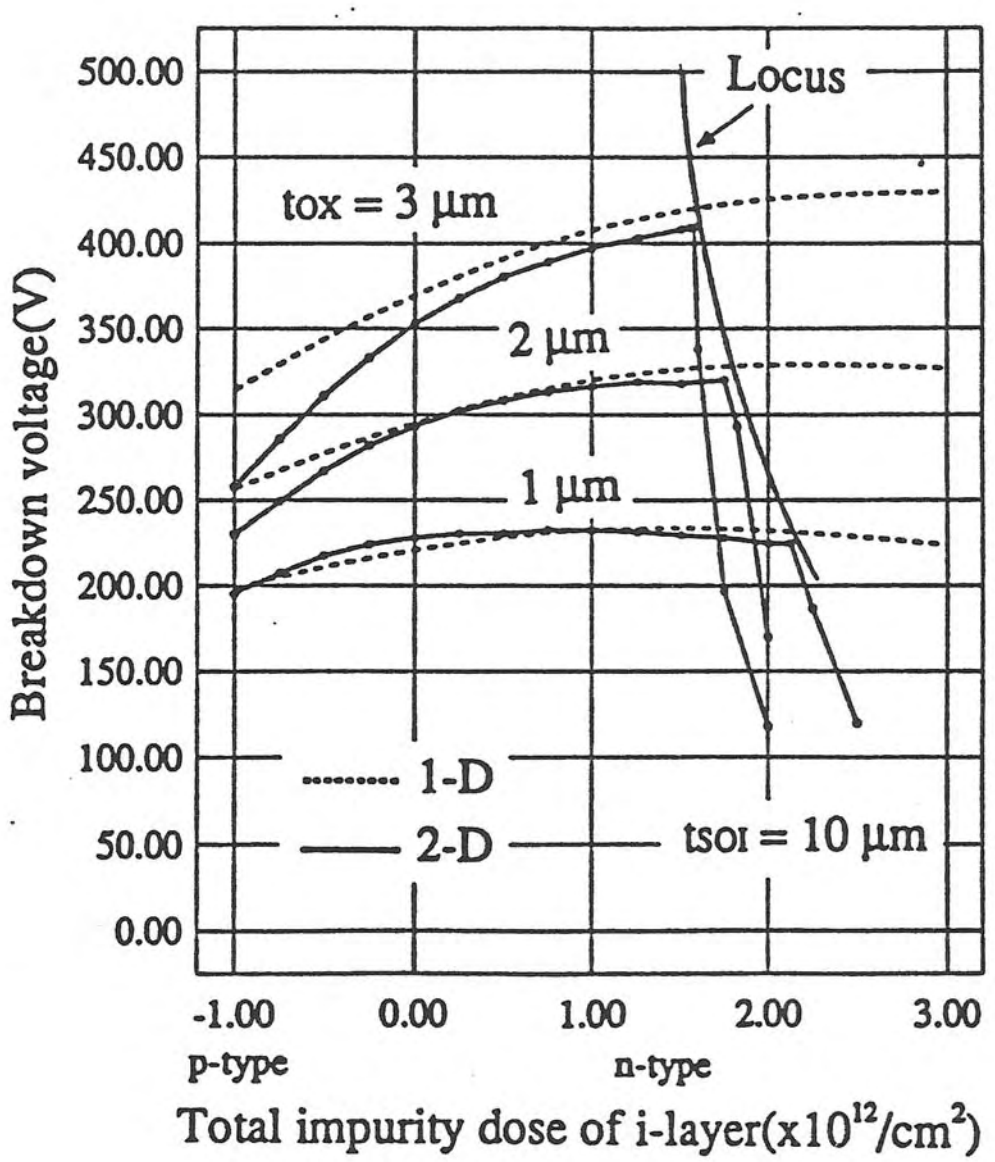
SOI device breakdown voltage vs. SOI thickness

Breakdown voltage is limited by MOS Diode

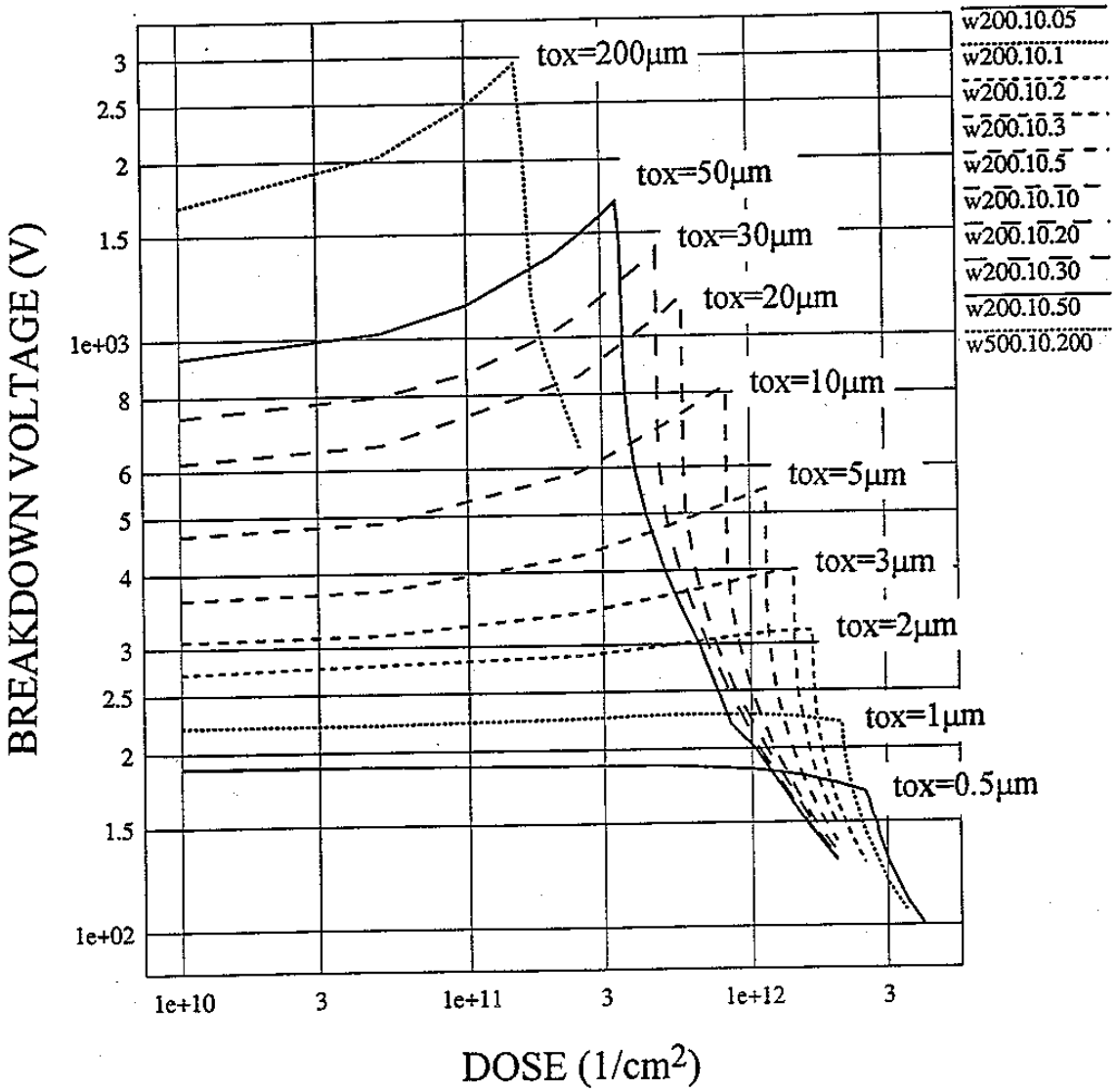


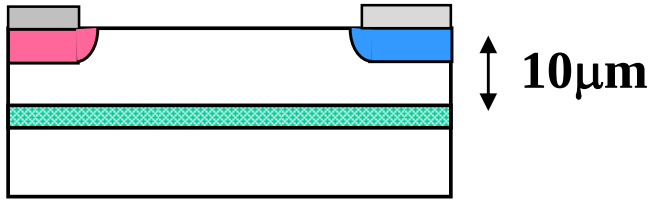


耐圧は1次元のMOSダイオードの耐圧で決定



Diode Breakdown Voltage on SOI with Very Thick Oxide





Box膜上にn型不純物拡散層を設けて高耐圧化

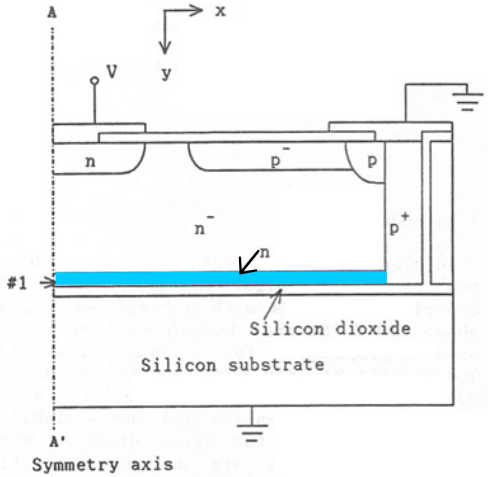


Fig.3B

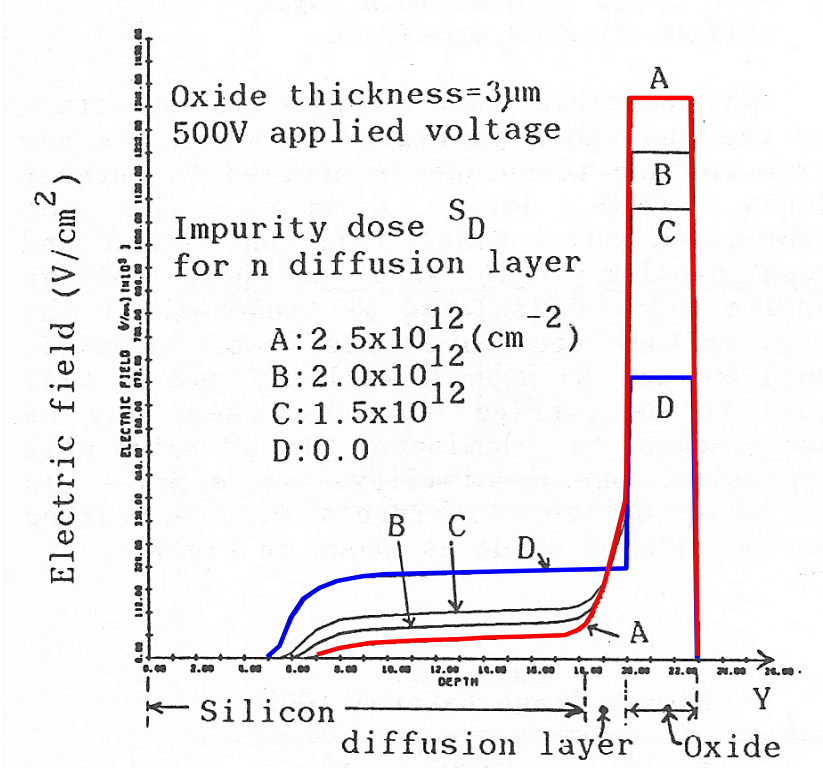
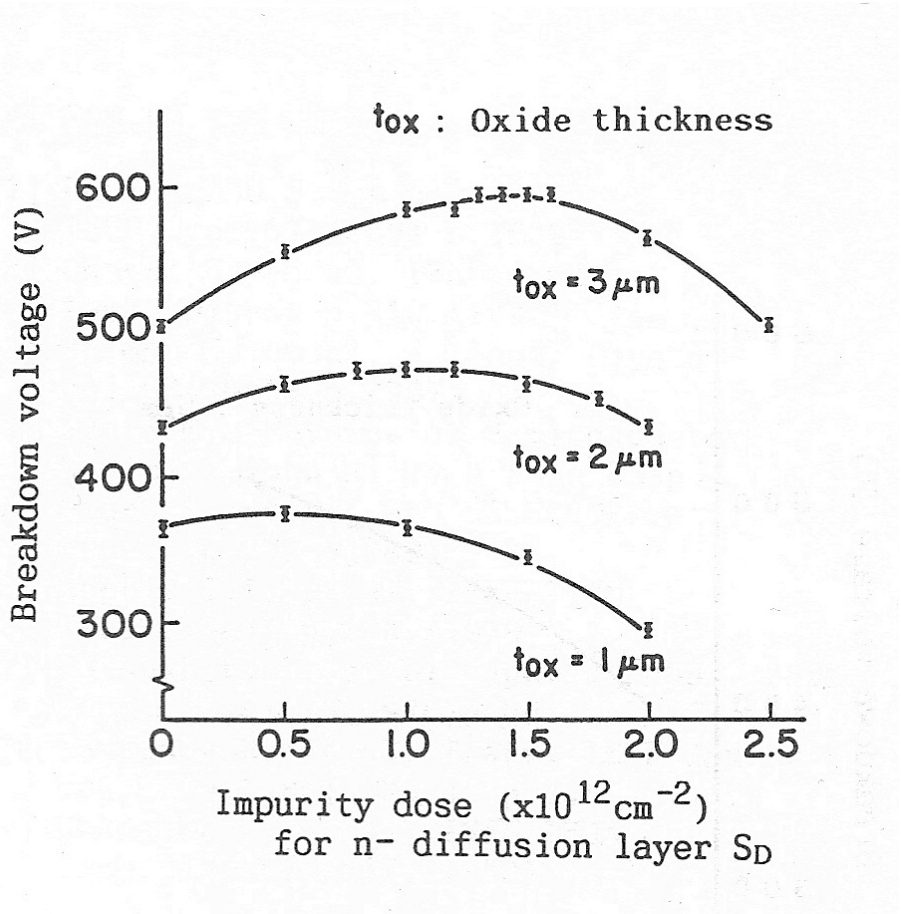


Fig.5 Electric field distribution along the symmetry axis. A high electric field is successfully applied in the oxide film.



Box界面電荷で耐圧向上

1-d MOSダイオードの耐圧を計算

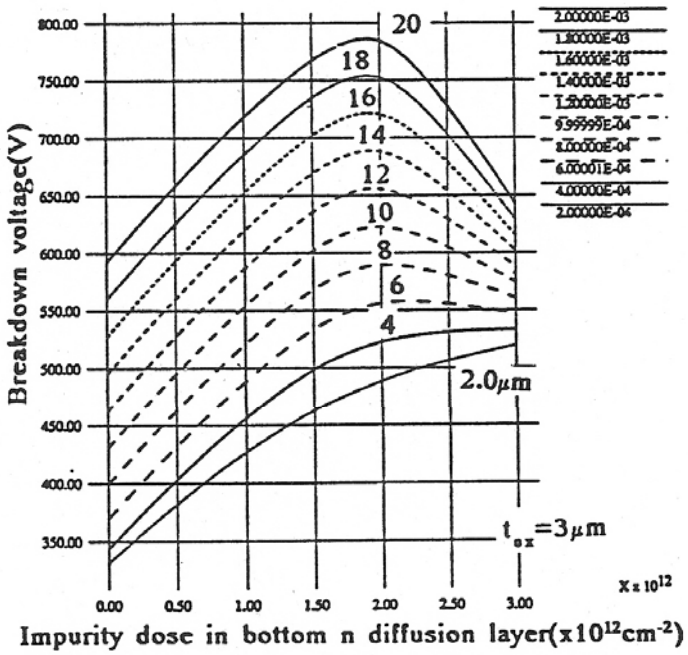


Fig.3 Calculated $n^+/n^-/n$/oxide/substrate diode breakdown voltage as a function of n diffusion layer impurity dose with n^- layer thickness as a parameter

Gaussian impurity profile($2\sqrt{Dt}=1\mu m$) is assumed for bottom n diffusion.

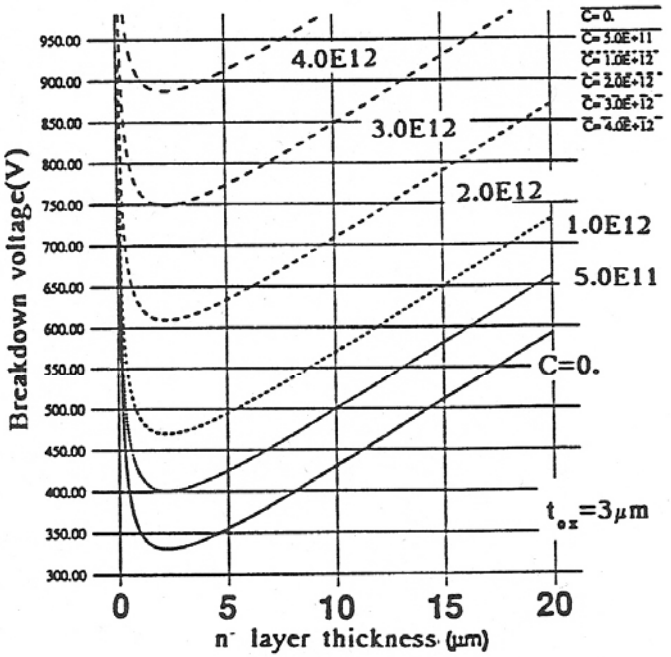
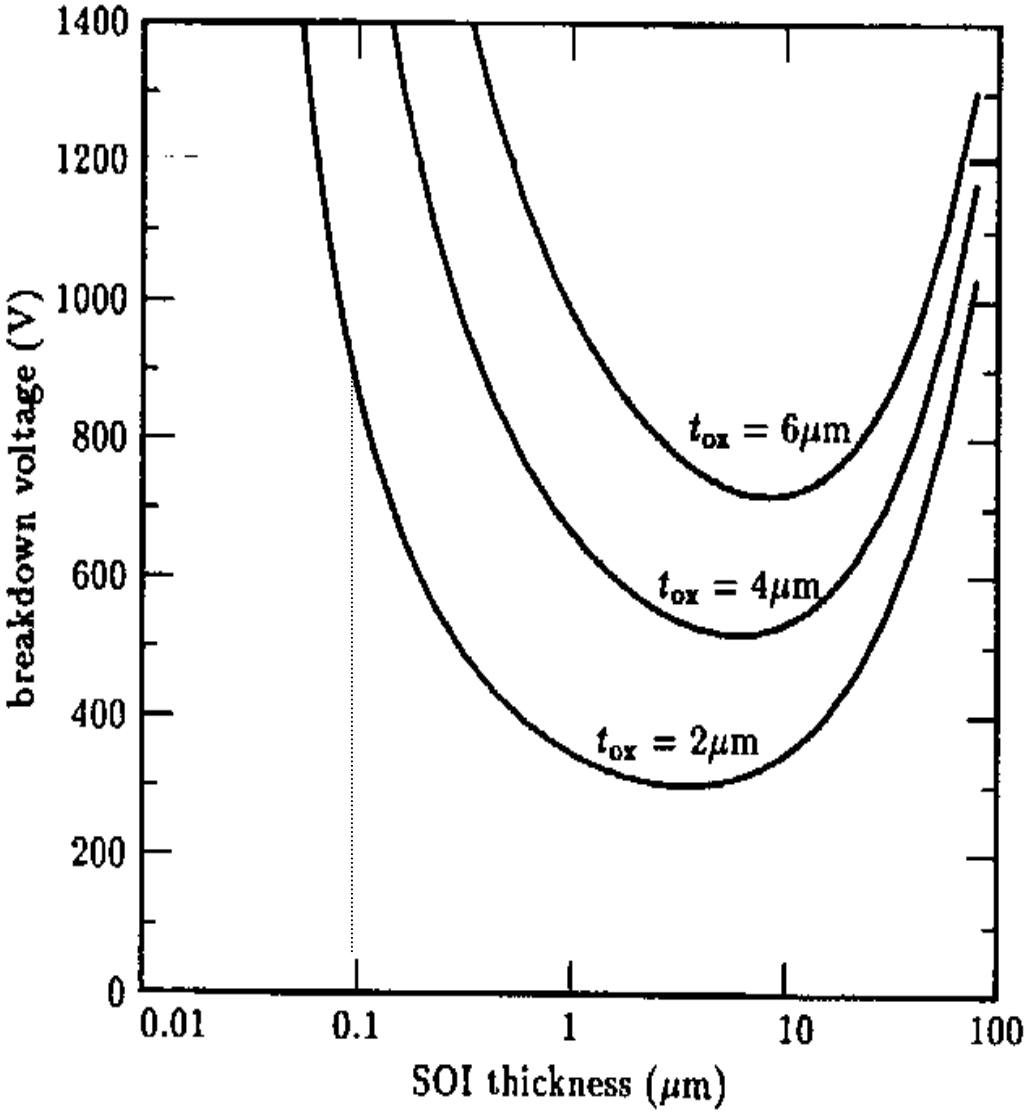
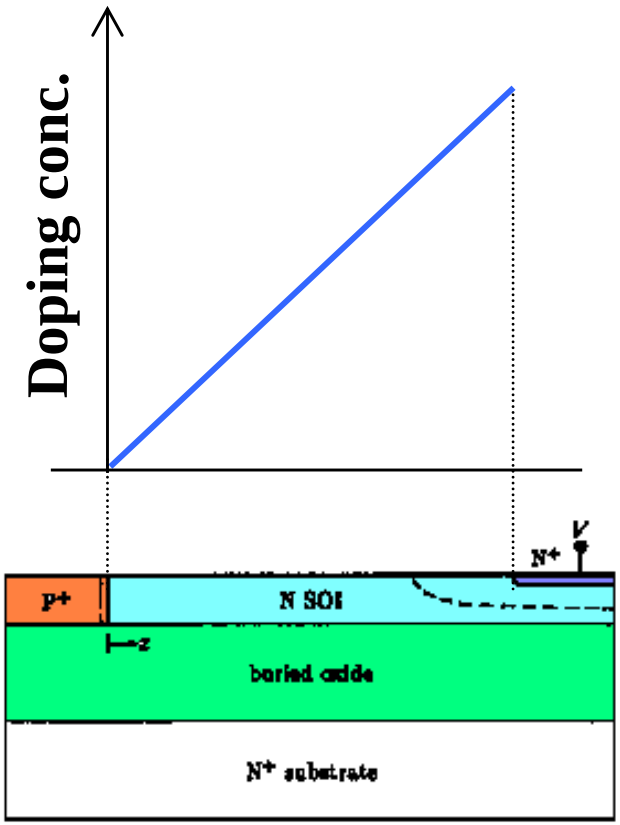


Fig.2 Calculated 1-d n^+/n^-/oxide/substrate diode breakdown voltage as a function of SOI layer thickness with interface charge density C as a parameter

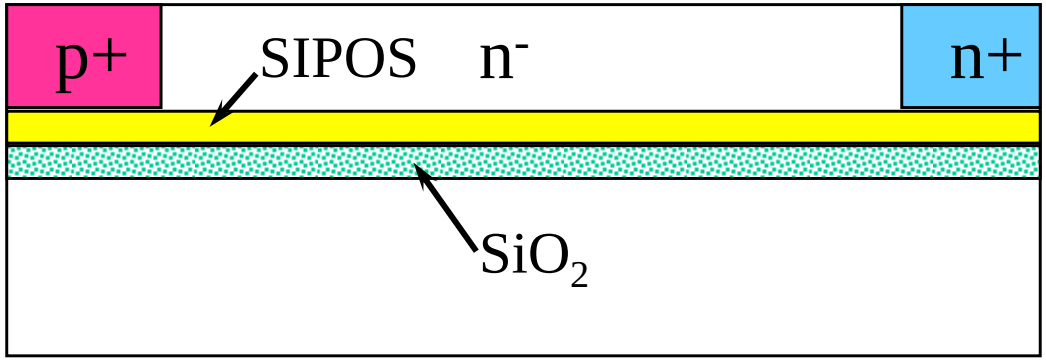
超薄膜SOIで高耐圧が可能

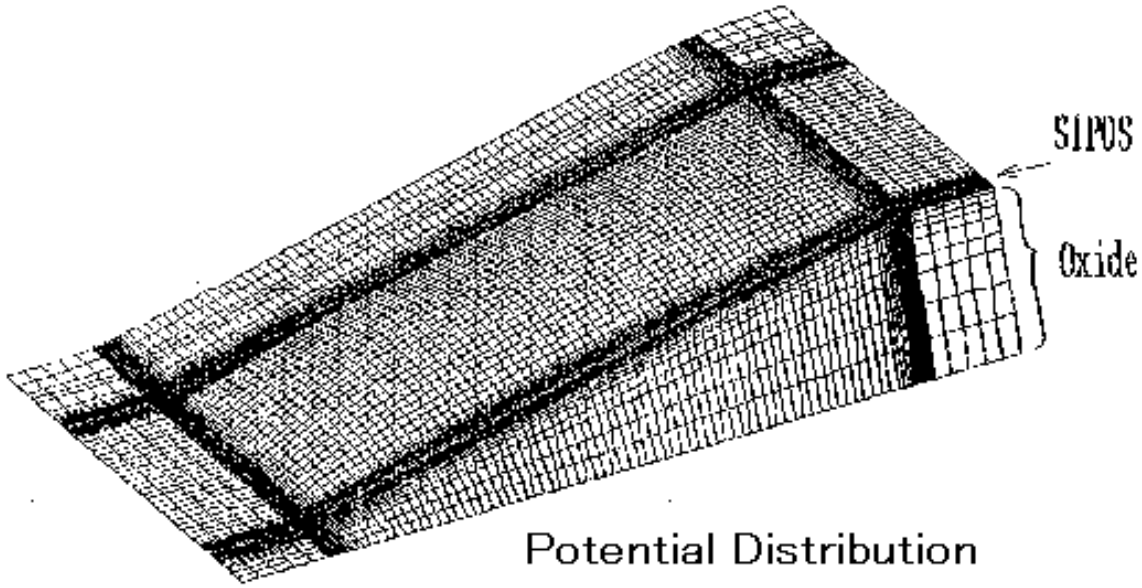




S.Merchant et al., ISPSD'91

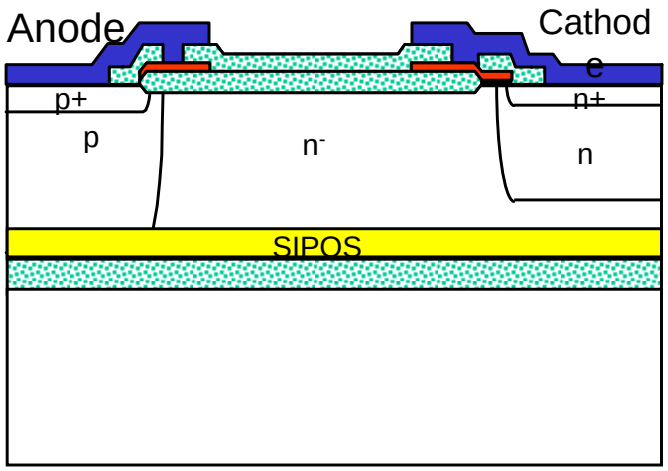
New SOI Diode Structure
proposed in 1991 ISPSD



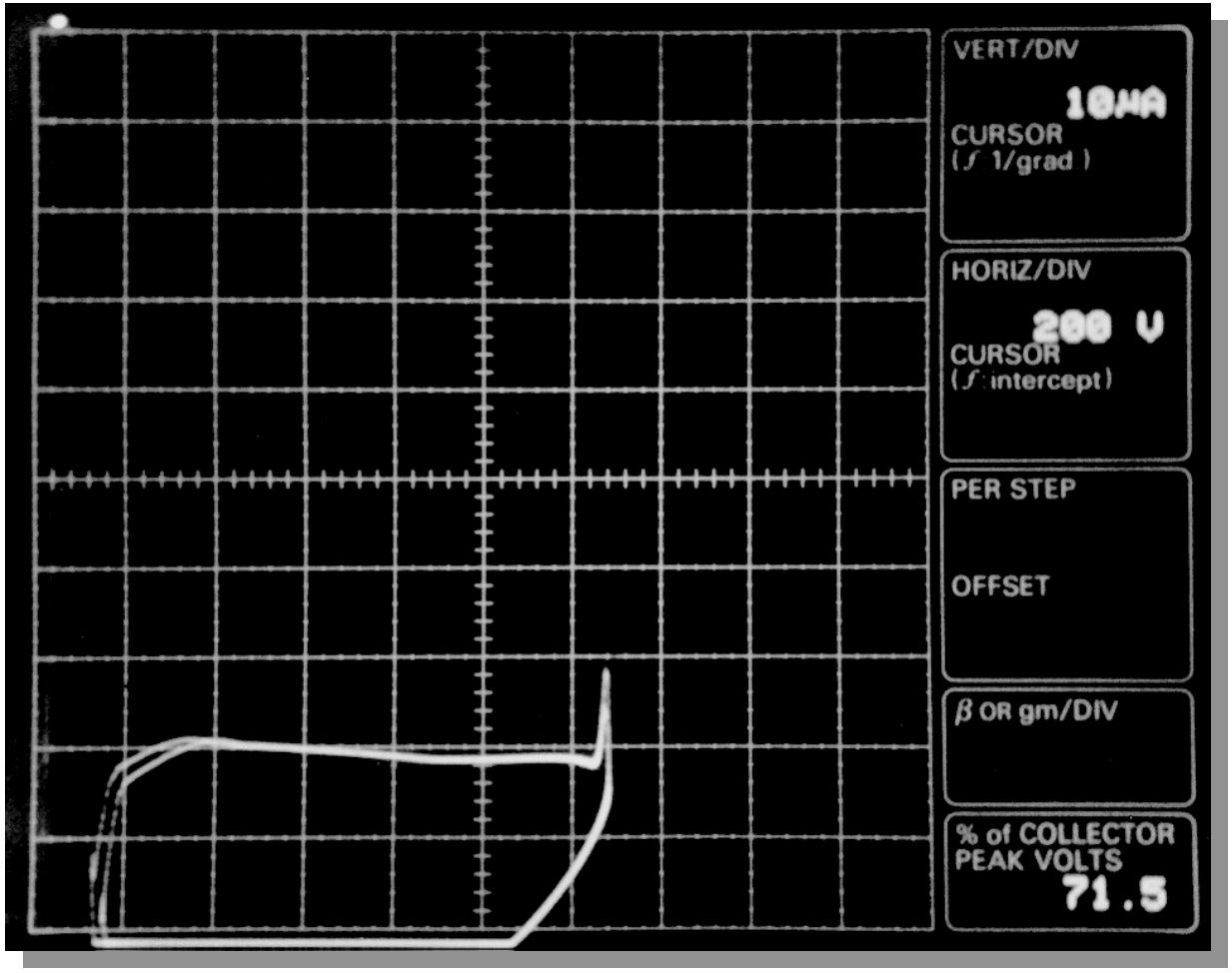


A.Nakagawa et al, ISPSD'91 & IEDM'96

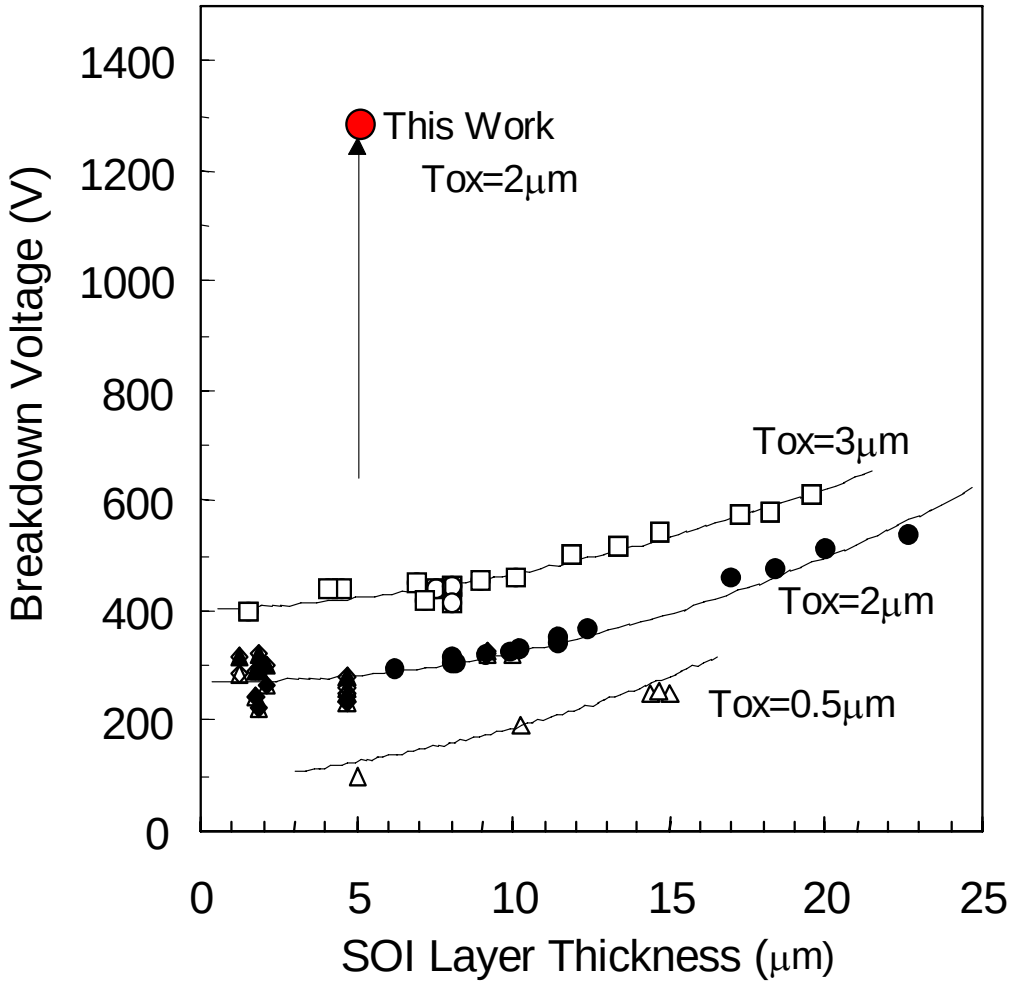
Reverse *I-V* curve for the diode on SOI with SIPOS layer



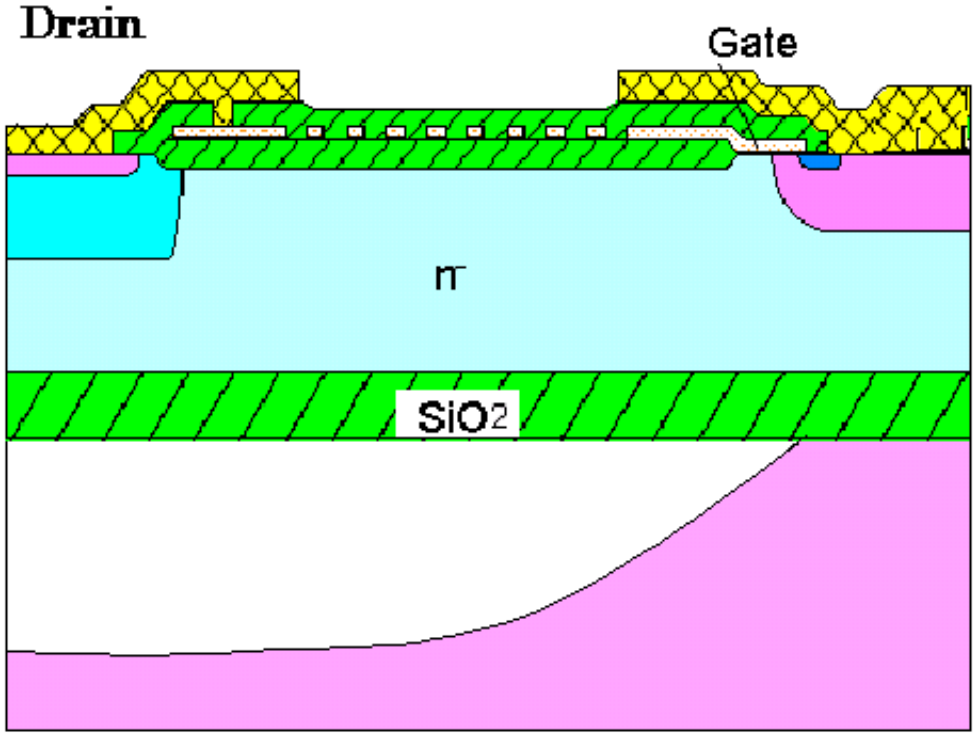
New Diode Structure

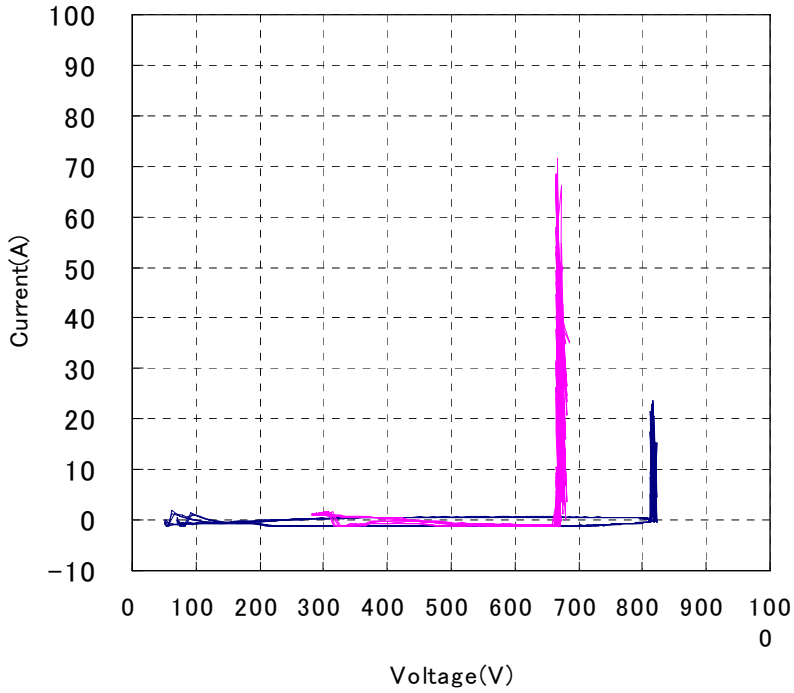


Diode breakdown voltage vs. SOI layer thickness with buried oxide thickness as a parameter

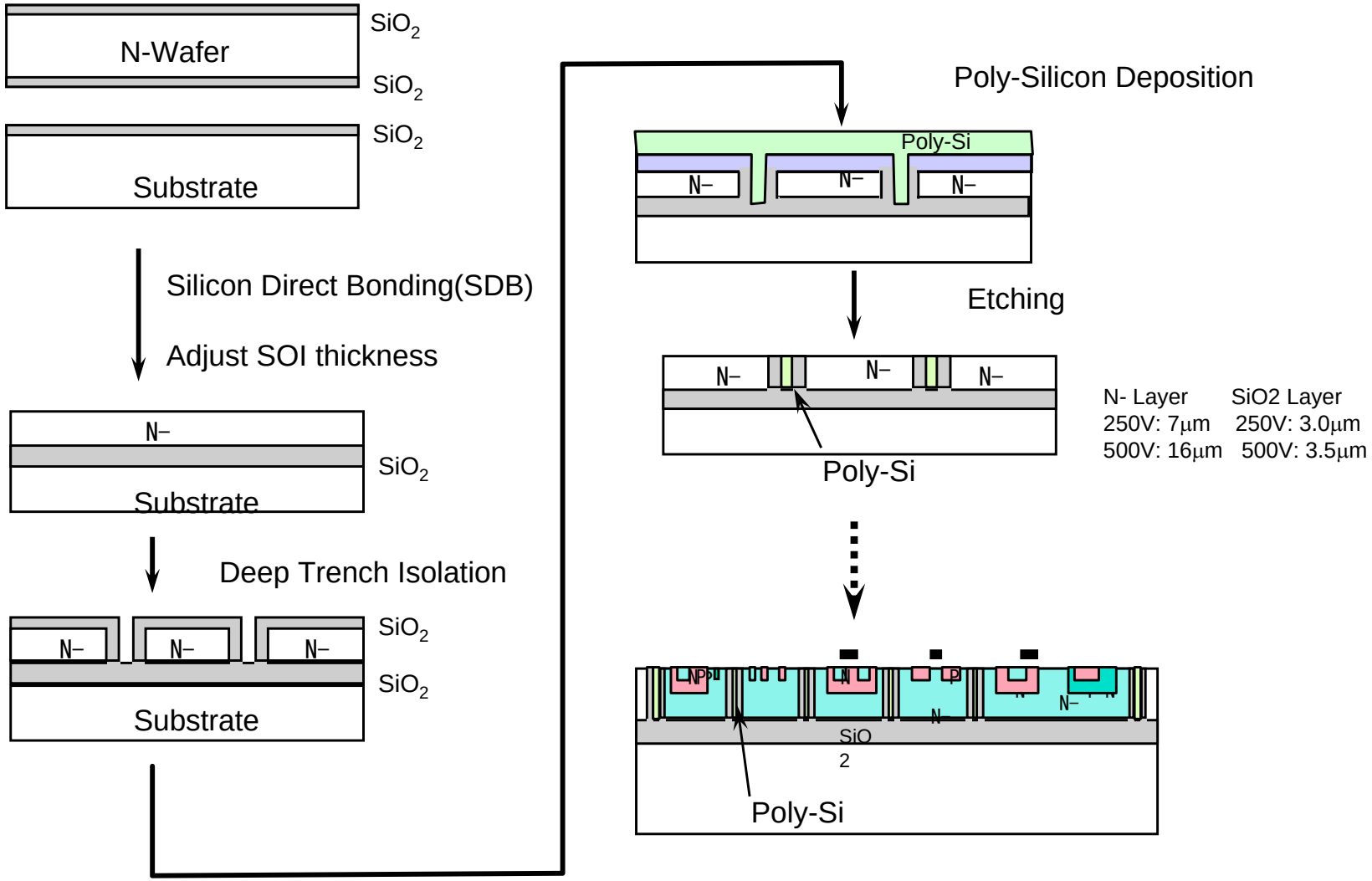


P⁻ 基板の効果


Drain
Gate
n⁻
SiO2

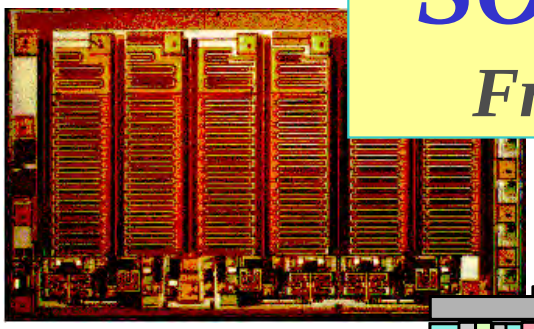

100
90
80
70
60
50
40
30
20
10
0
−10
Current(A)
0
100
200
300
400
500
600
700
800
900
1000
Voltage(V)

Process Flow of SOI Power IC



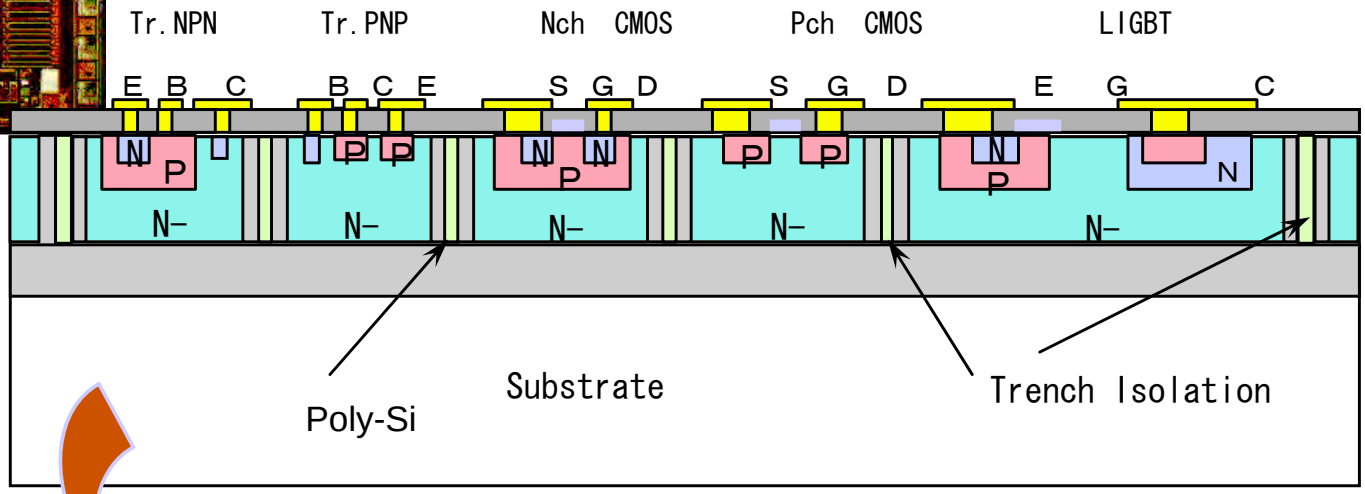
SOI Process Evolution

From BiCMOS to Full CMOS



2nd Gen.Process

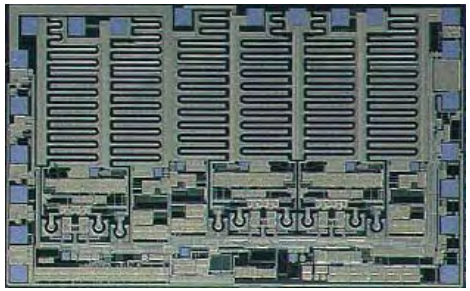
(1.5μm、5V BiCMOS)

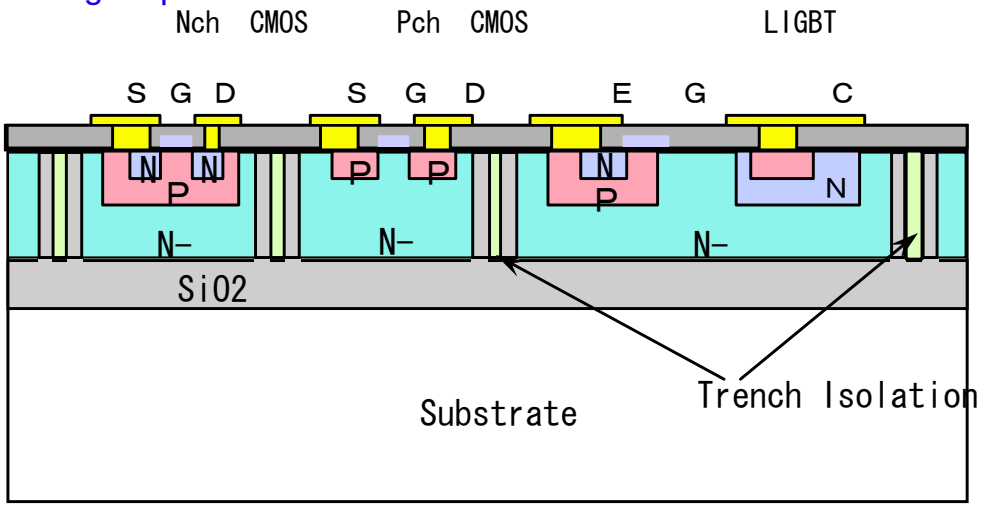


32 masking steps

3rd Gen. Process

(30V CMOS)

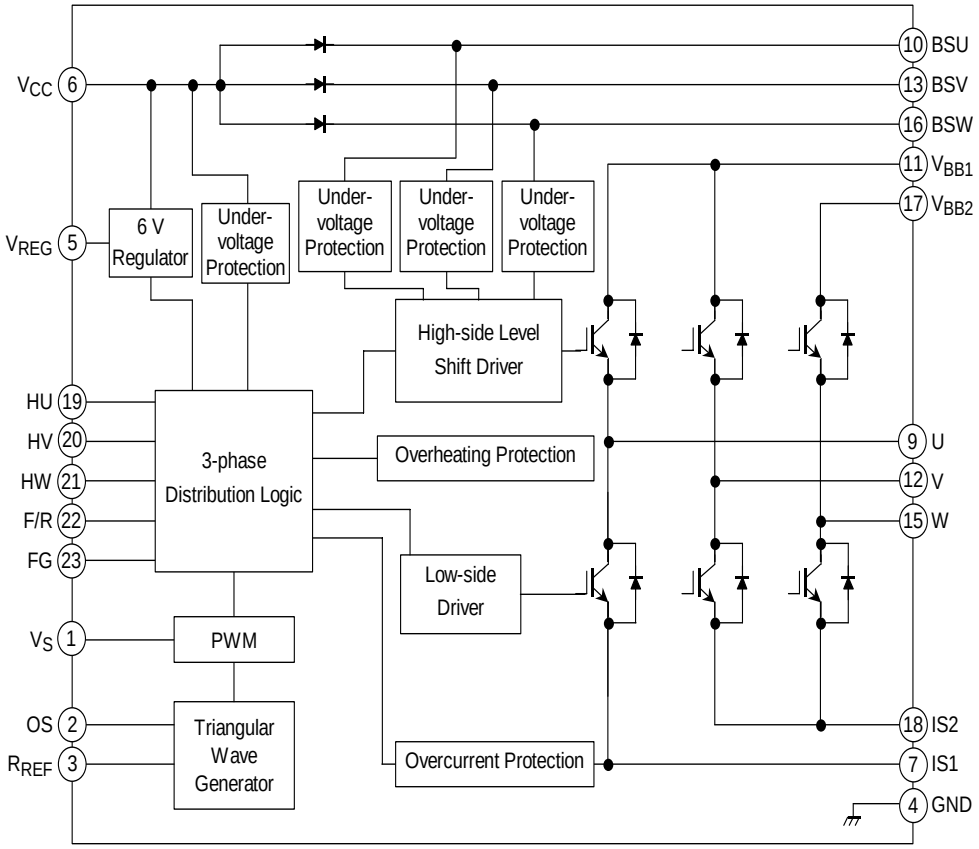


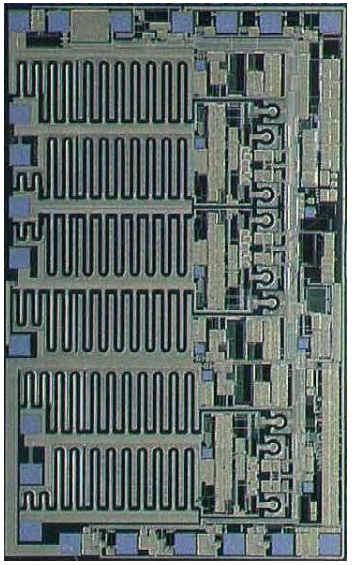


23 masking steps

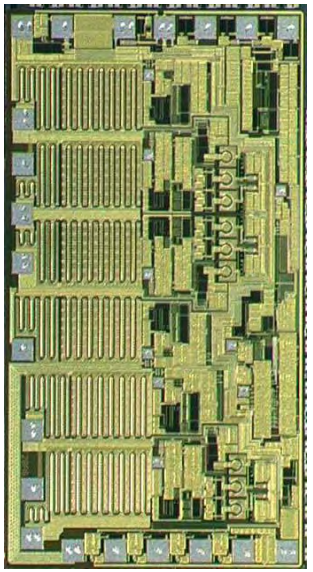
Low Cost 500V/250V 1A 1 Chip Inverter IC

30V CMOS + DMOS + LIGBT



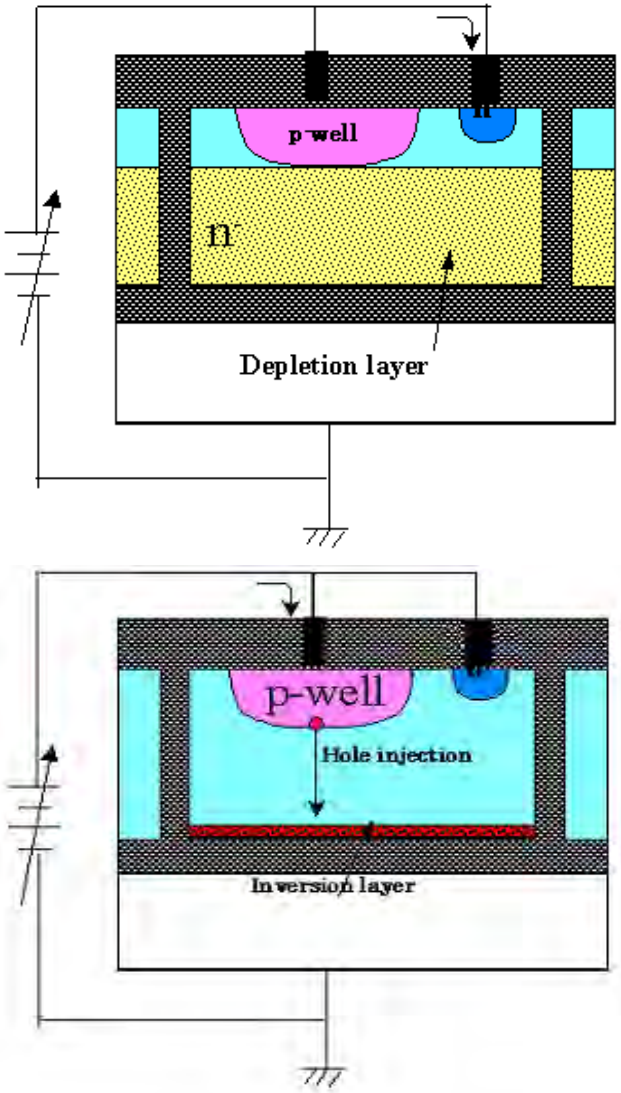


500V1A

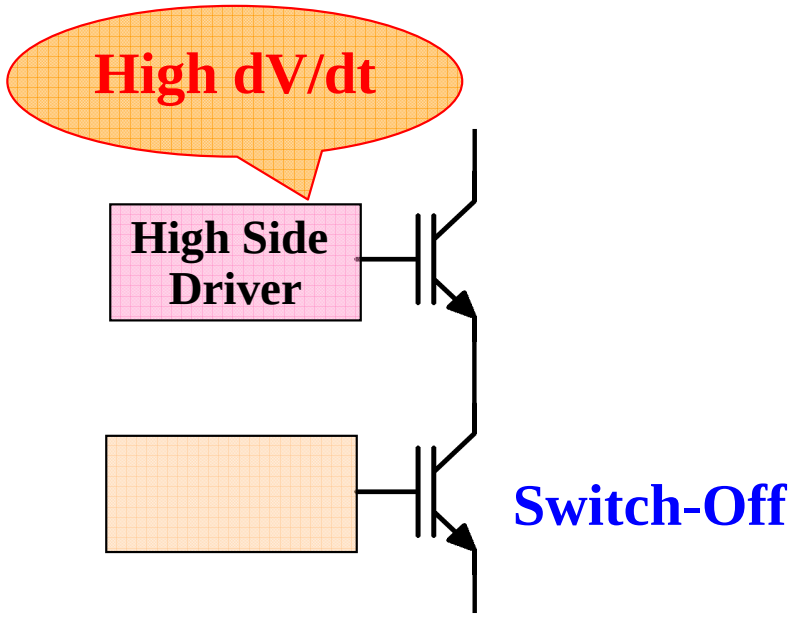


250V1A

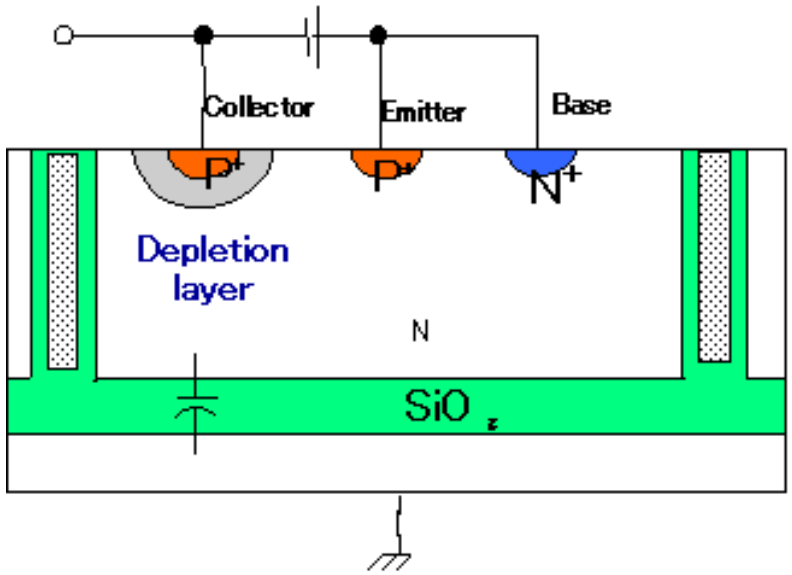
Why Btr's were eliminated?



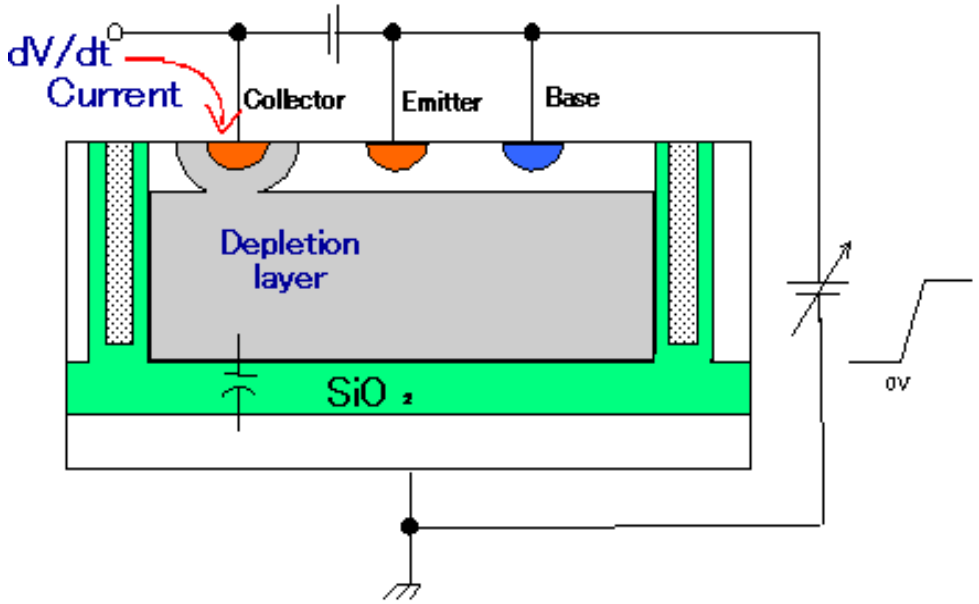
1. *To simplify process.*
2. *Displacement current !*



How bipolar transistor malfunction



Off state



Wrong signal is created by dV/dt

List of SOI Devices

	Conventional Process (BiCMOS)	New Process (30V CMOS)
NMOS	Vgs=5V,BVdss=7V	Vgs=15V,BVdss=30V
PMOS	Vgs=5V,BVdss=7V	Vgs=15V,BVdss=30V
NPN	Vceo=30V	
PNP	Vceo=7V	
Nch LDMOS	Vgs=5V,BVdss=30V	
Pch LDPMOS	Vgs=5V,BVdss=30V	
HV-NMOS	BVdss=500V	
IGBT	BVdss=500V	
FWD	BV=500V	
BSD	BV=500V	

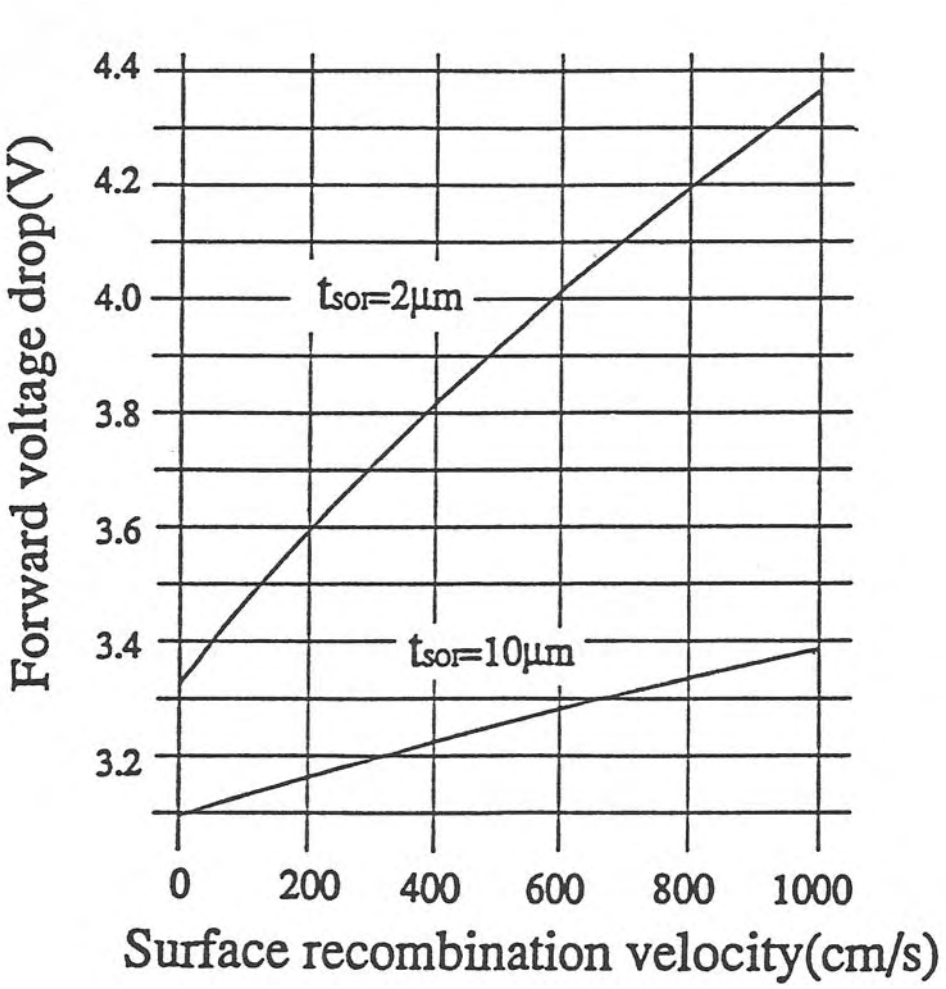
Other : zener diode, resistor, capacitor

LIGBT

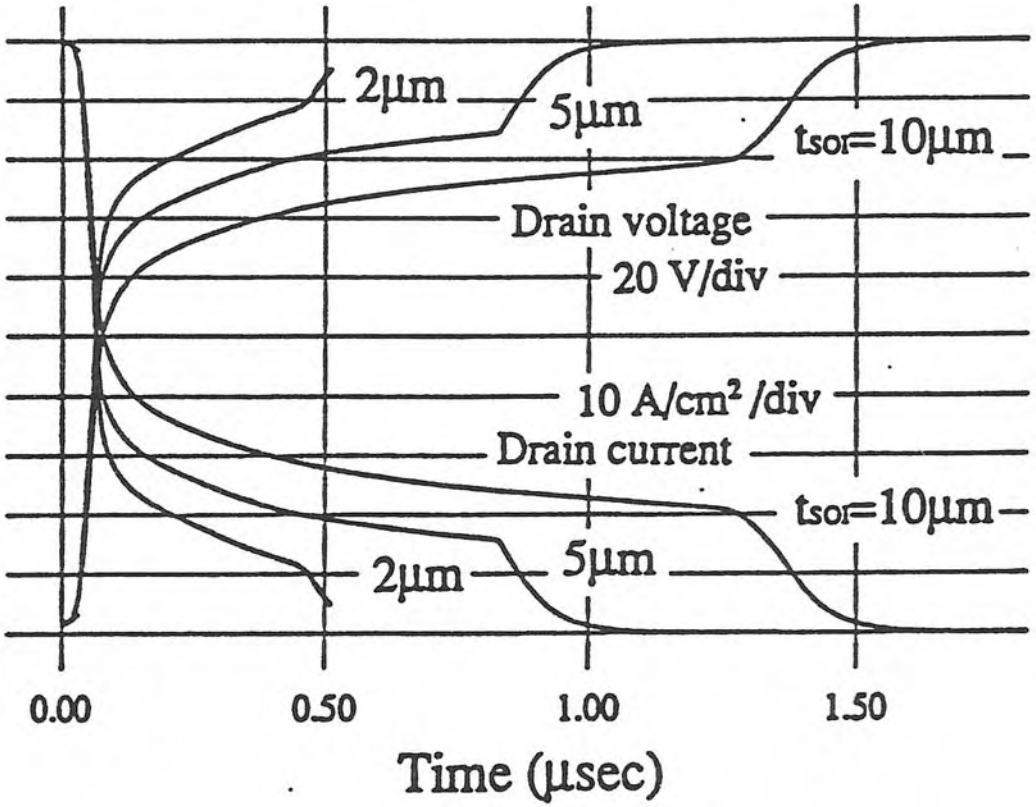
SOI power ICの課題

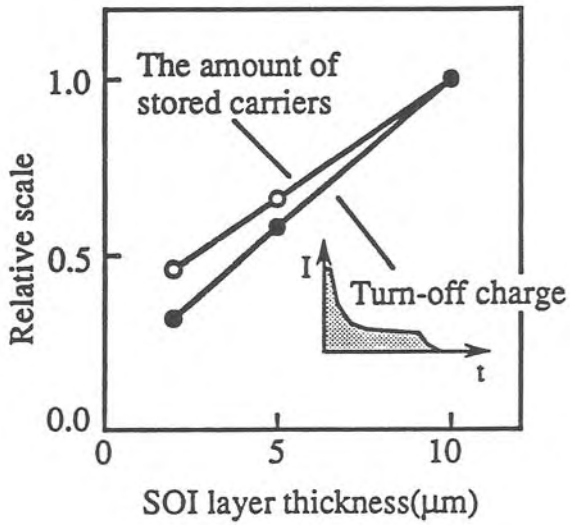
- High voltage large current devices
  - ***500V 3A multi-channel Lateral IGBT***
  - ***CMOS compatible process***
    - ***No lifetime control***
- High voltage interconnection

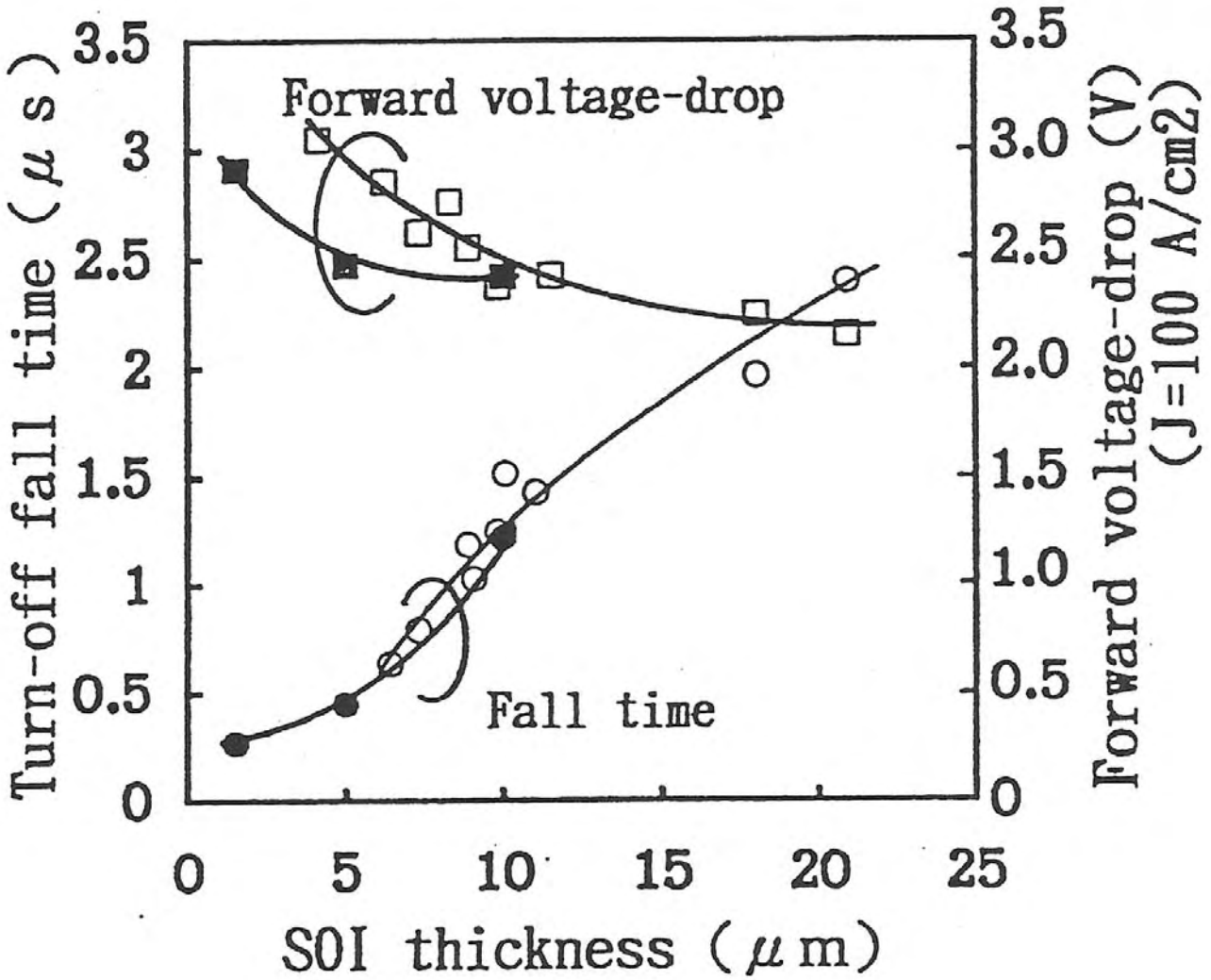
薄いSOIと厚いSOI



薄いSOIの方がスイッチングスピードが速い!!

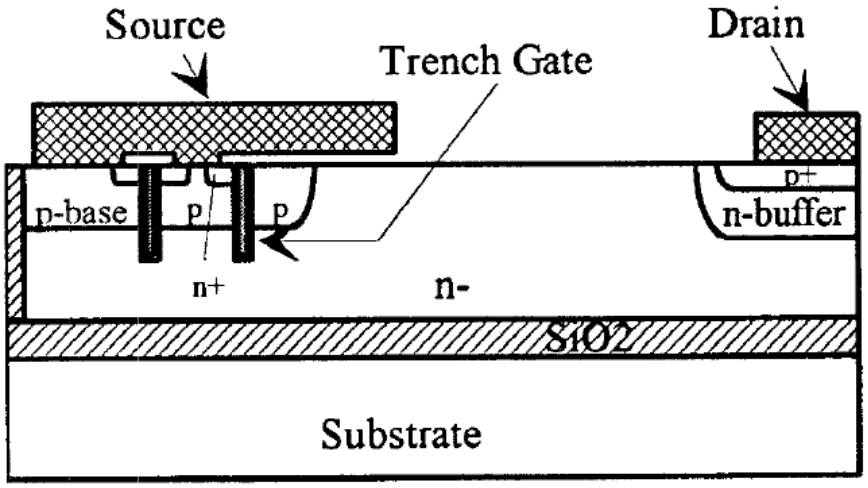


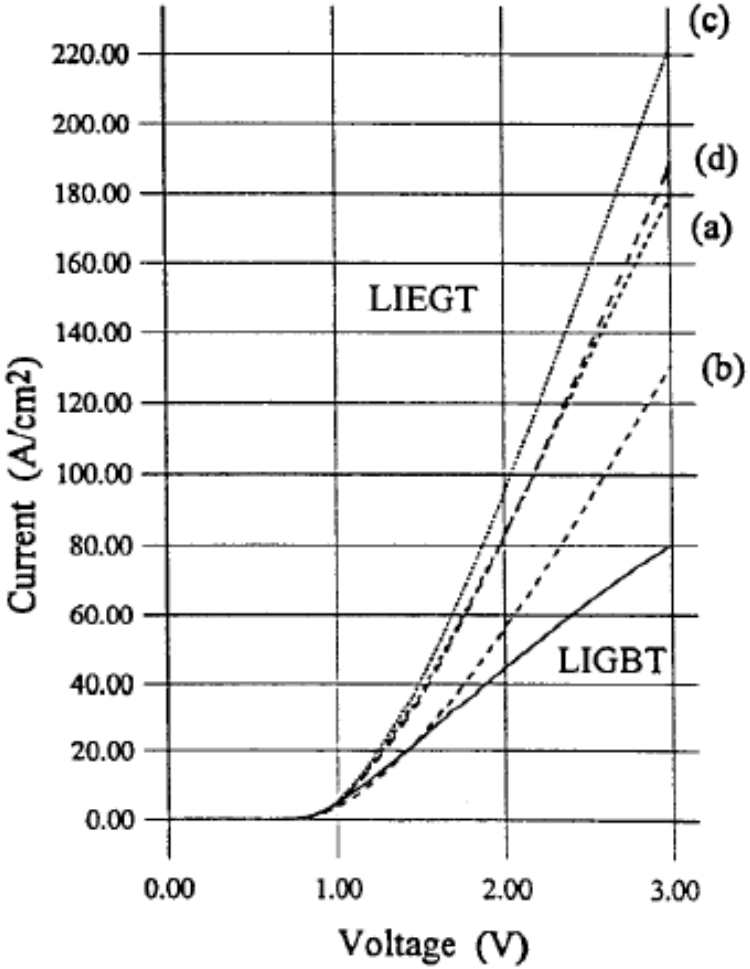



Forward voltage-drop
Fall time
Turn-off fall time (μs)
Forward voltage-drop (V)
(J=100 A/cm2)
SOI thickness (μm)
0
0.5
1
1.5
2
2.5
3
3.5
0
5
10
15
20
25

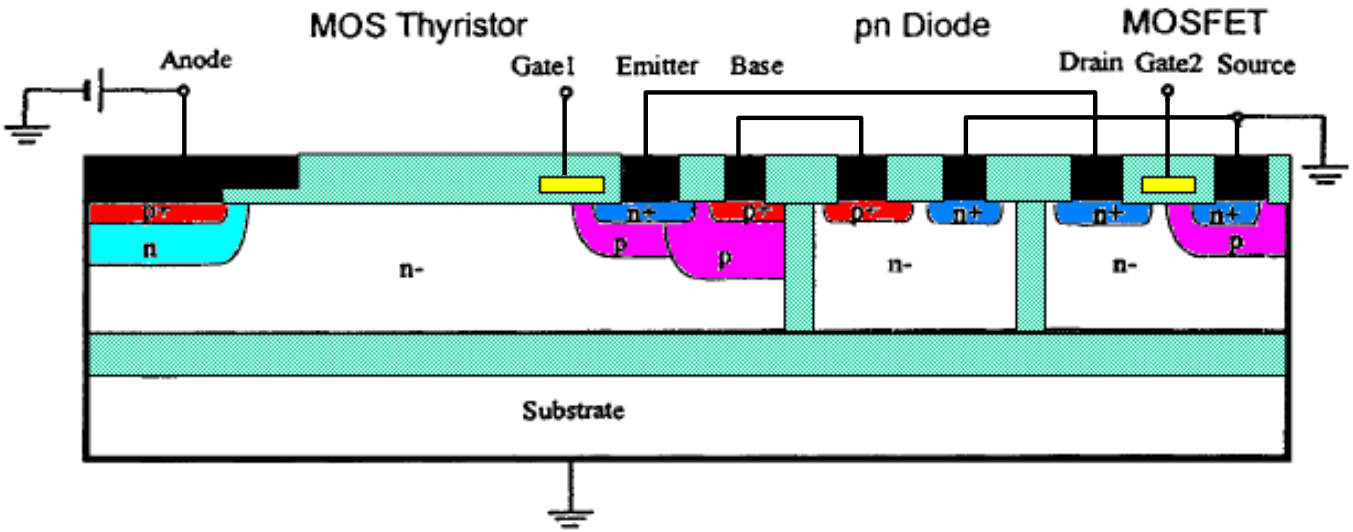
1995 ISPSD

横型IEGT

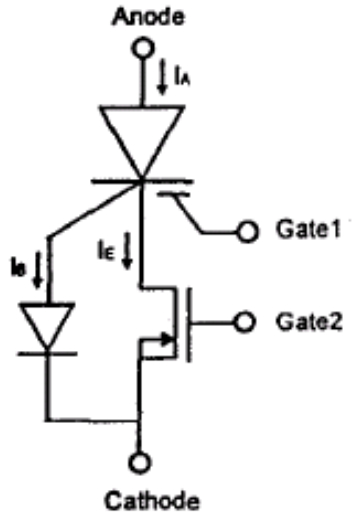




エミッタオープンMOSサイリスタ



Cross sectional-view of a high voltage lateral MOS thyristor cascode switch on SOI.



Equivalent circuit of the hybrid device.

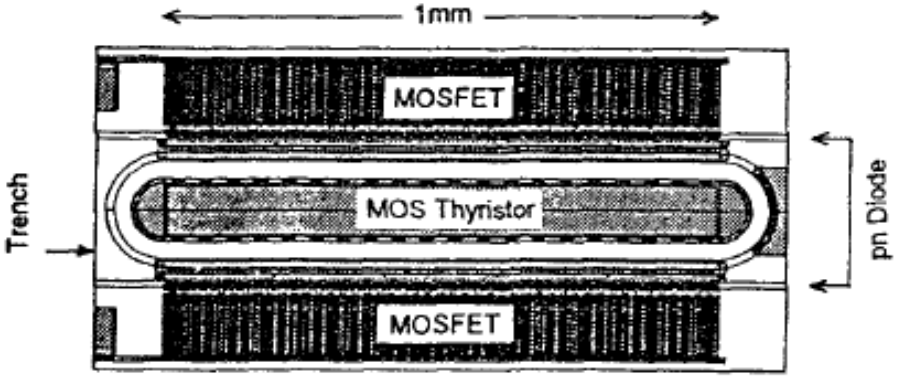
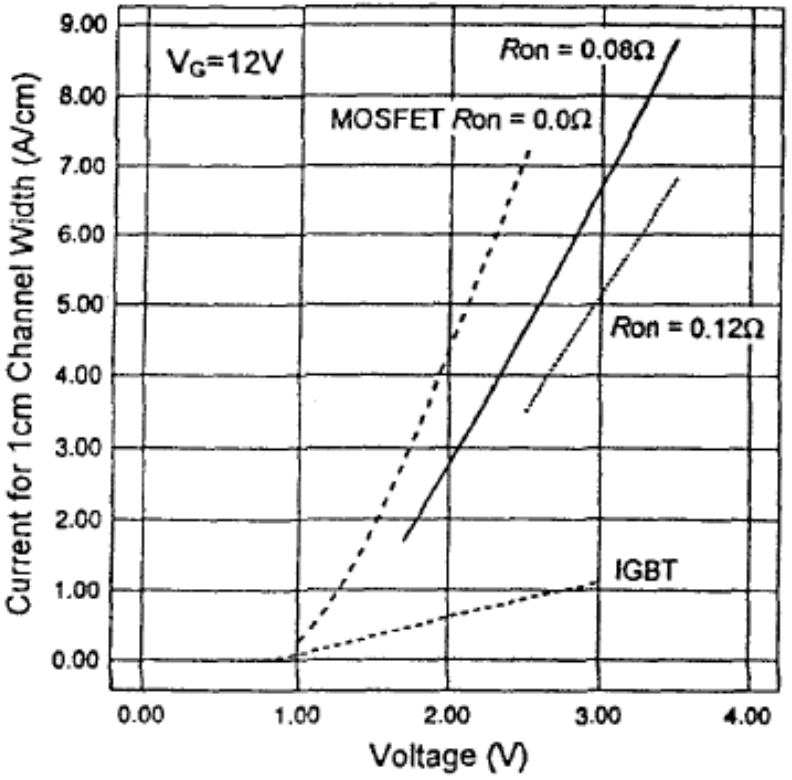
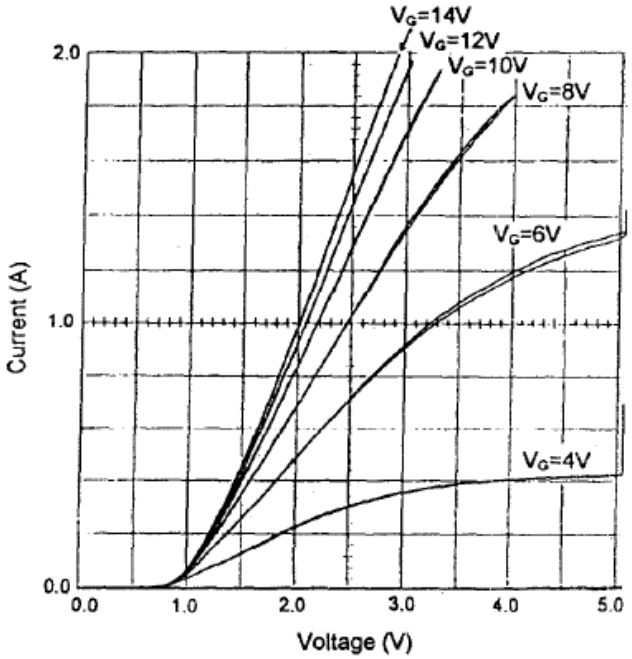


Fig. 3 Schematic layout of the hybrid device.





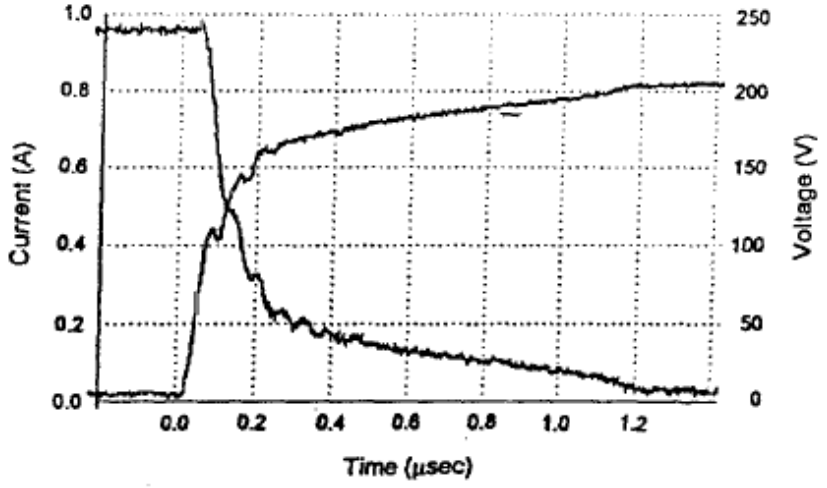
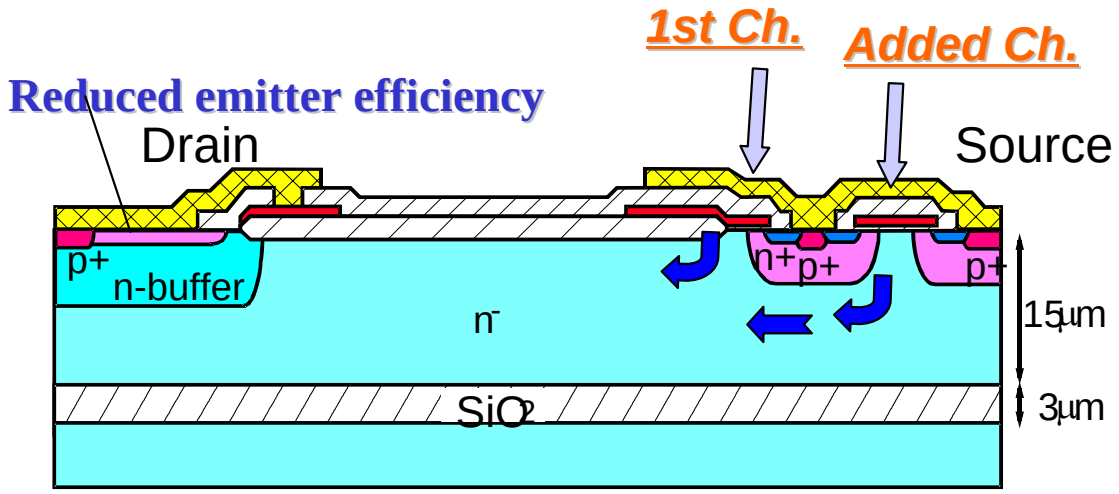
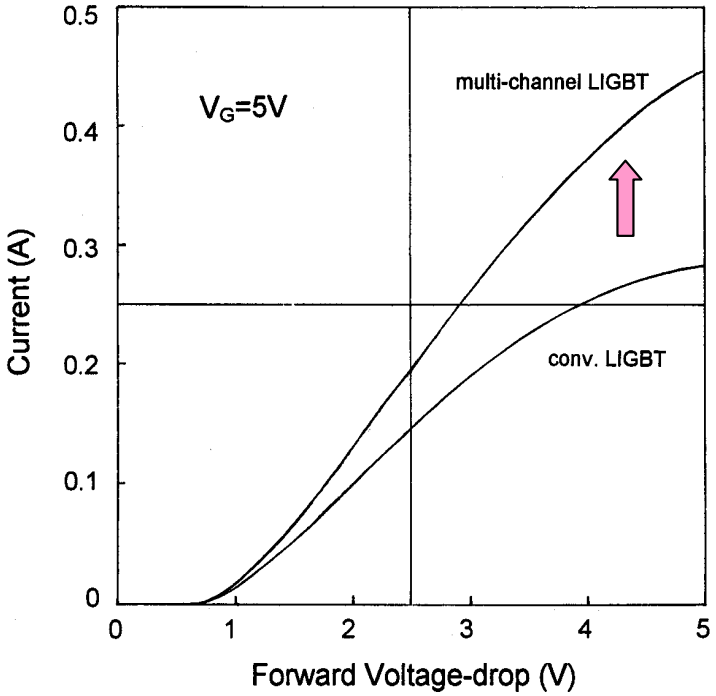


Fig. 9 Measured turn-off waveform.

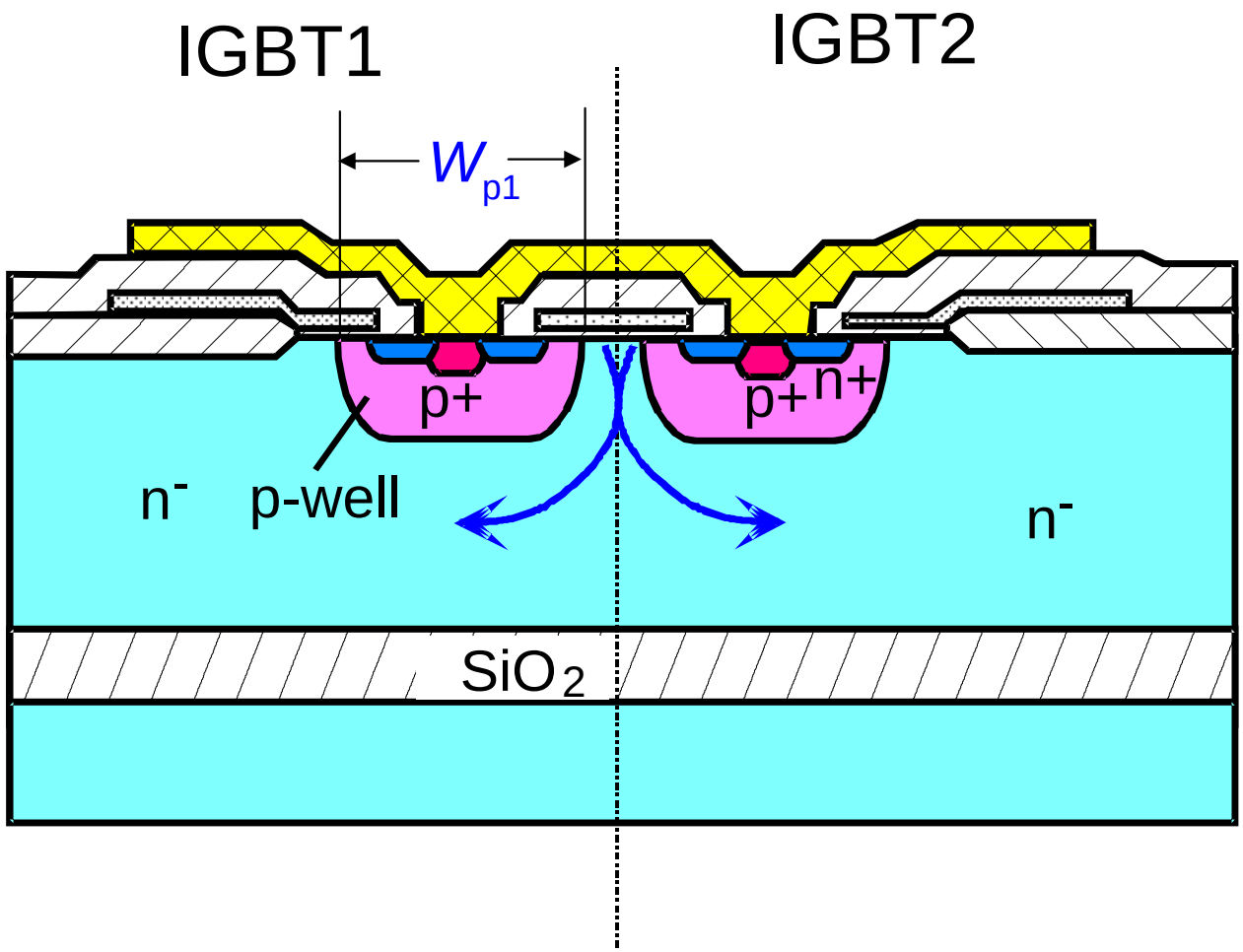
マルチチャネル 500V LIGBTs　1997 ISPSD

- **Large Current Capability**
  Multiple planar surface channels
- **Switching speed is controlled by p-emitter efficiency**
  No lifetime control: CMOS compatible

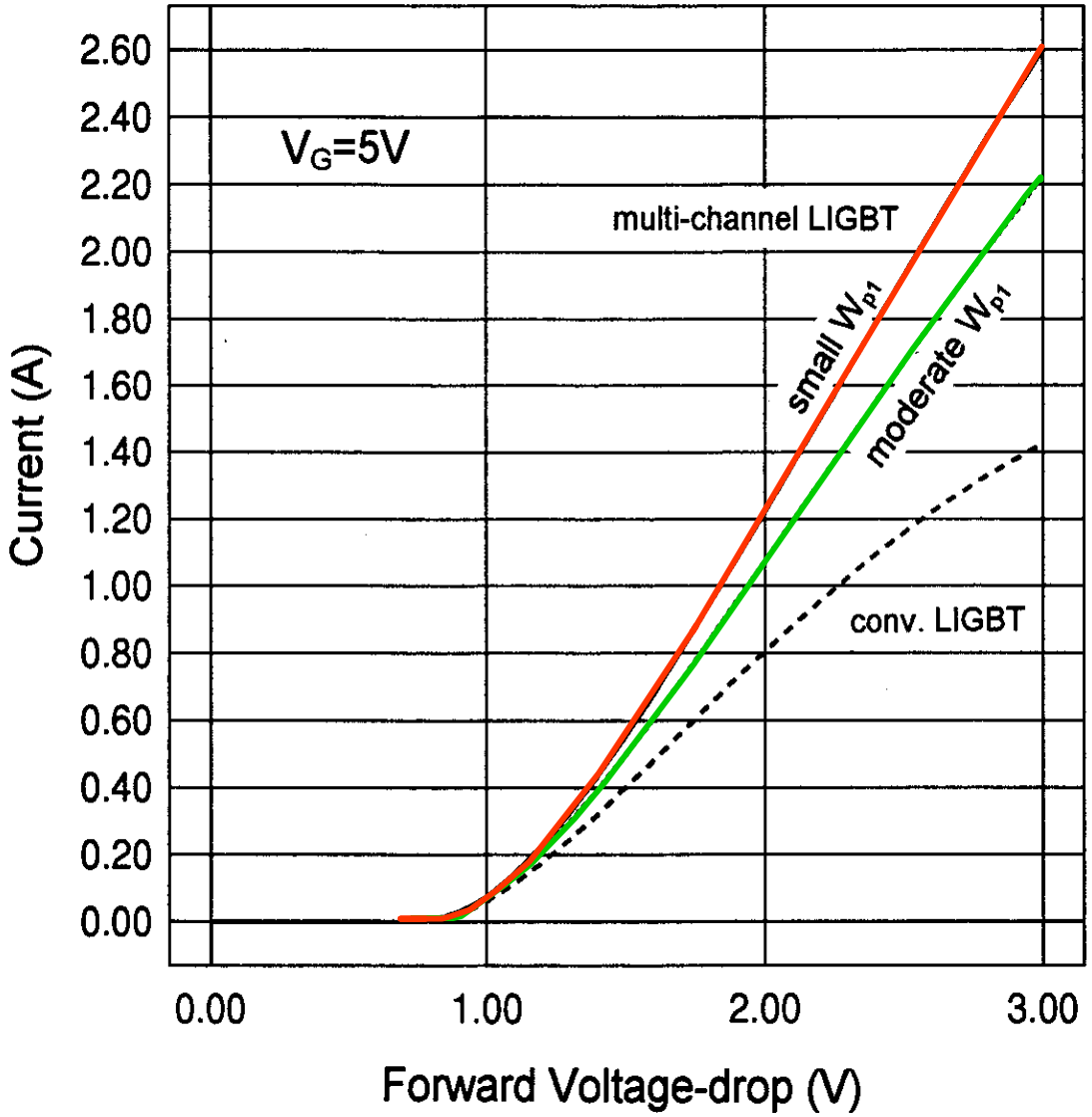




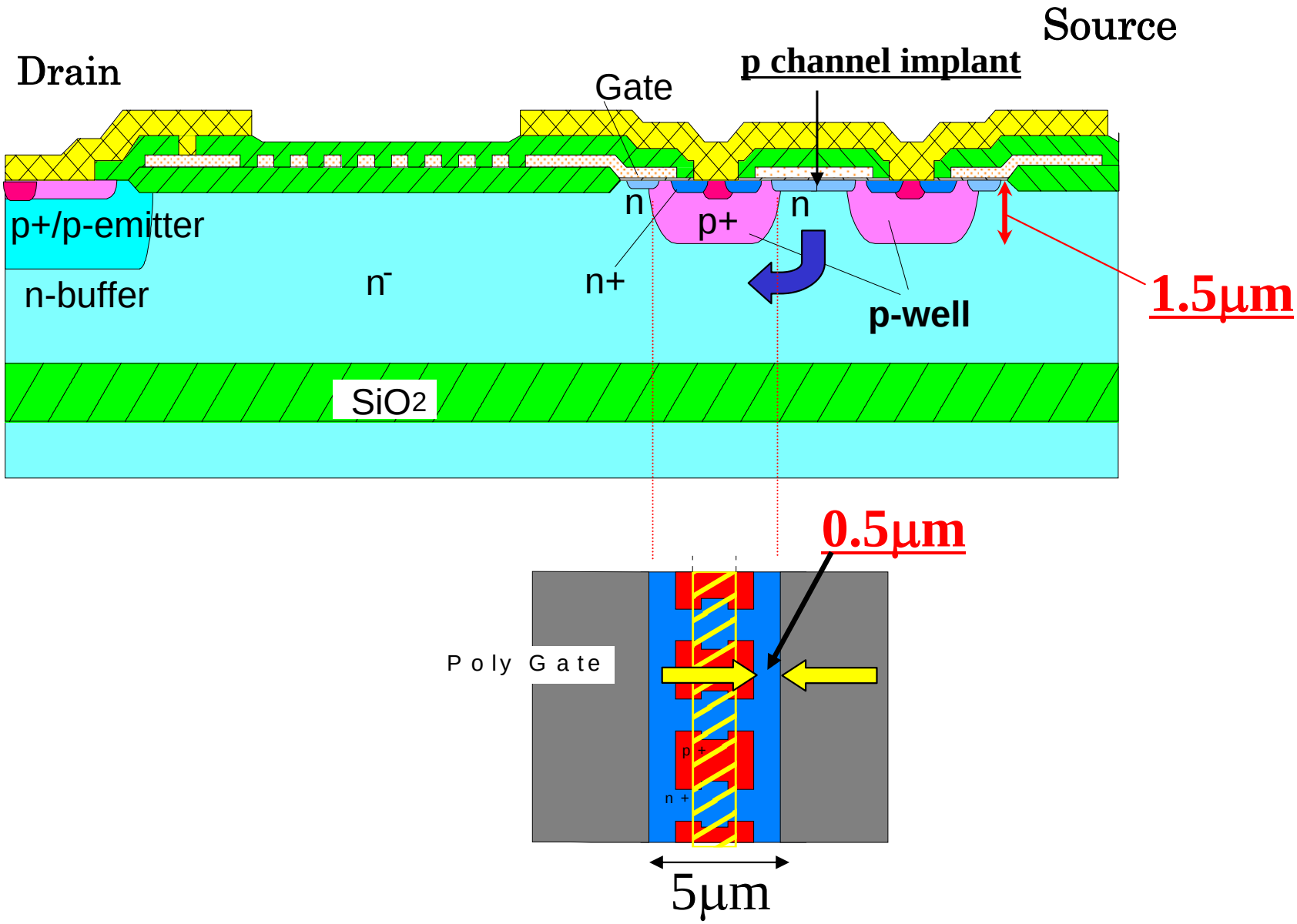
Shared source structure of multi-channel LIGBTs for trade-off improvement



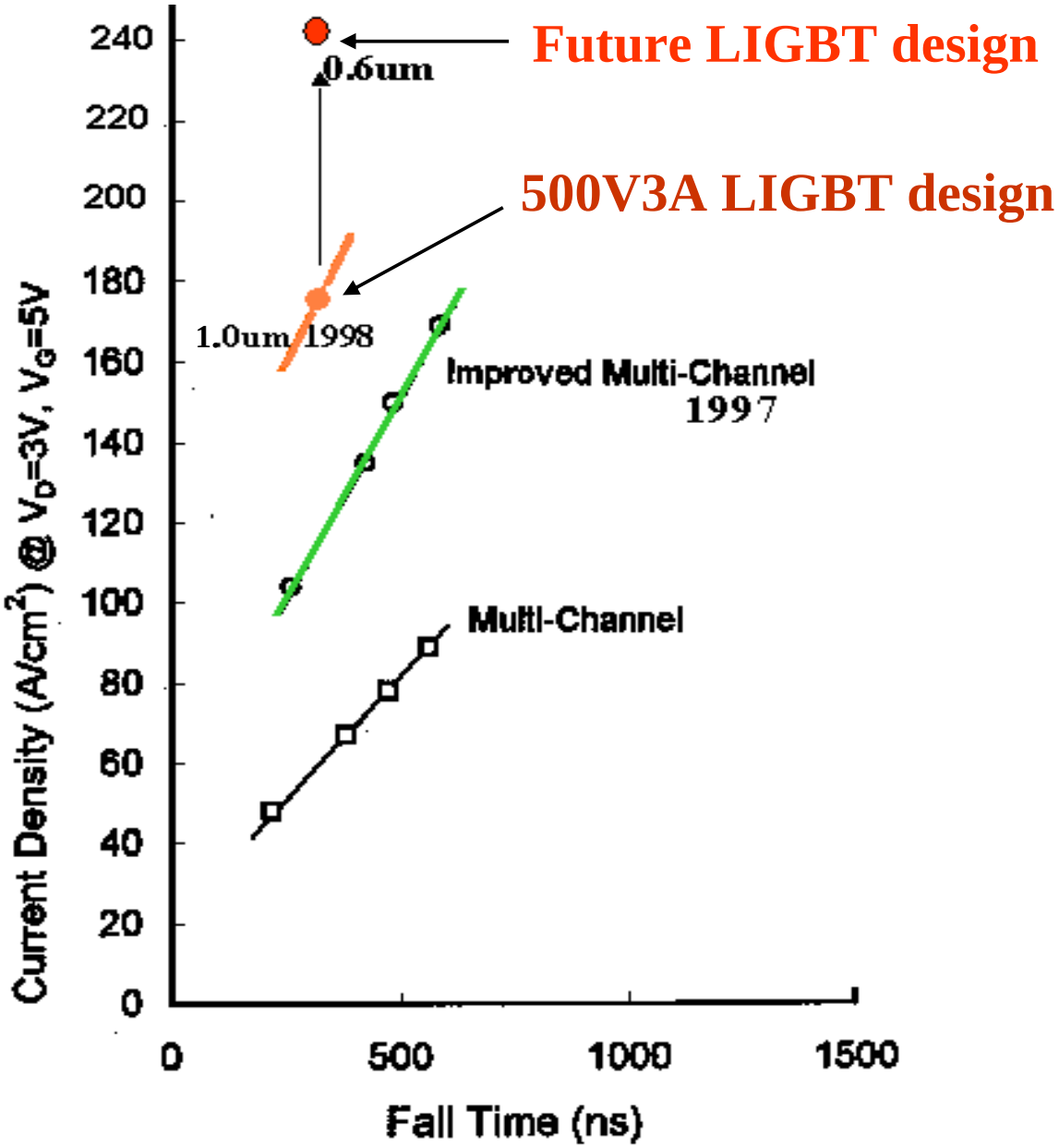
Calculated current-voltage curves of conventional and multi-channel LIGBTs



Finer p-well design enhancing inner electron channel current

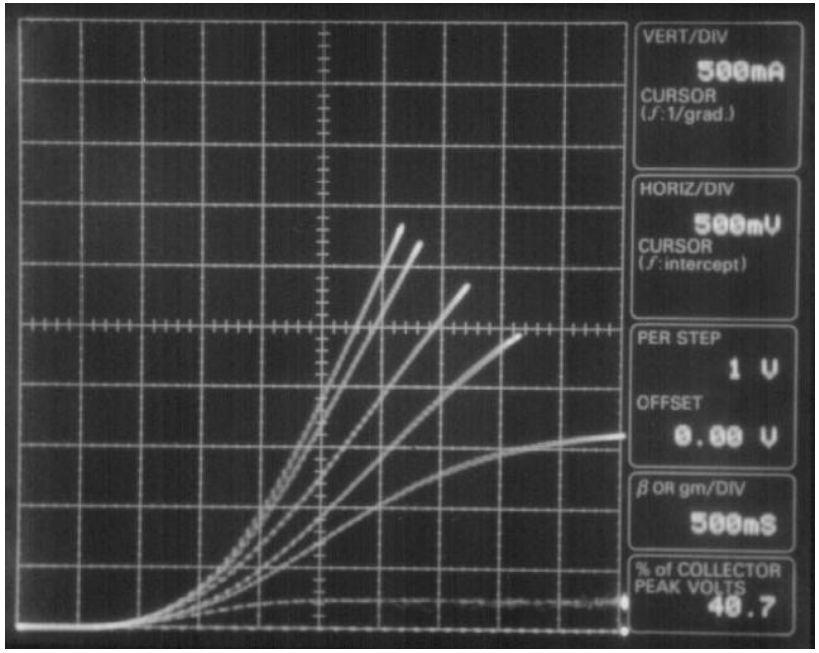


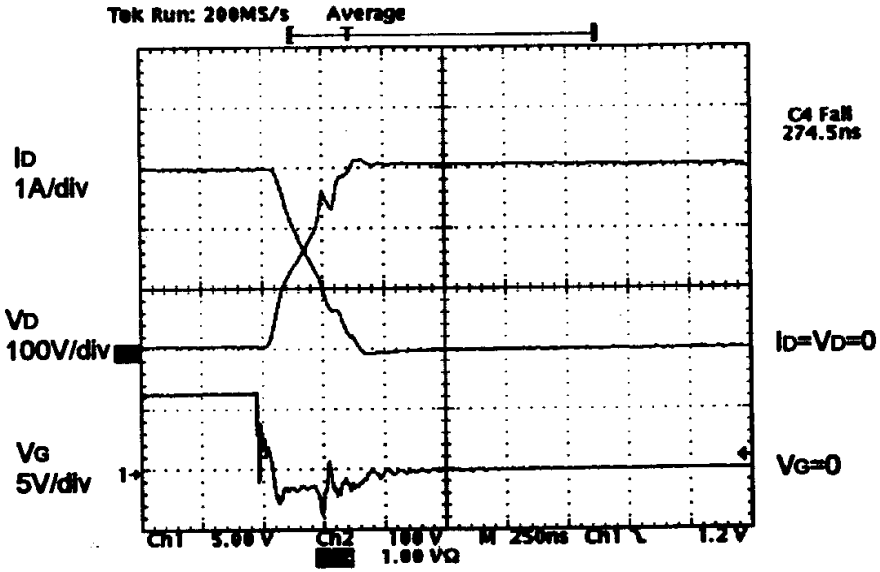
Improvement in Trade-Off relation



500V 3A LIGBT

@1999 ISPSD



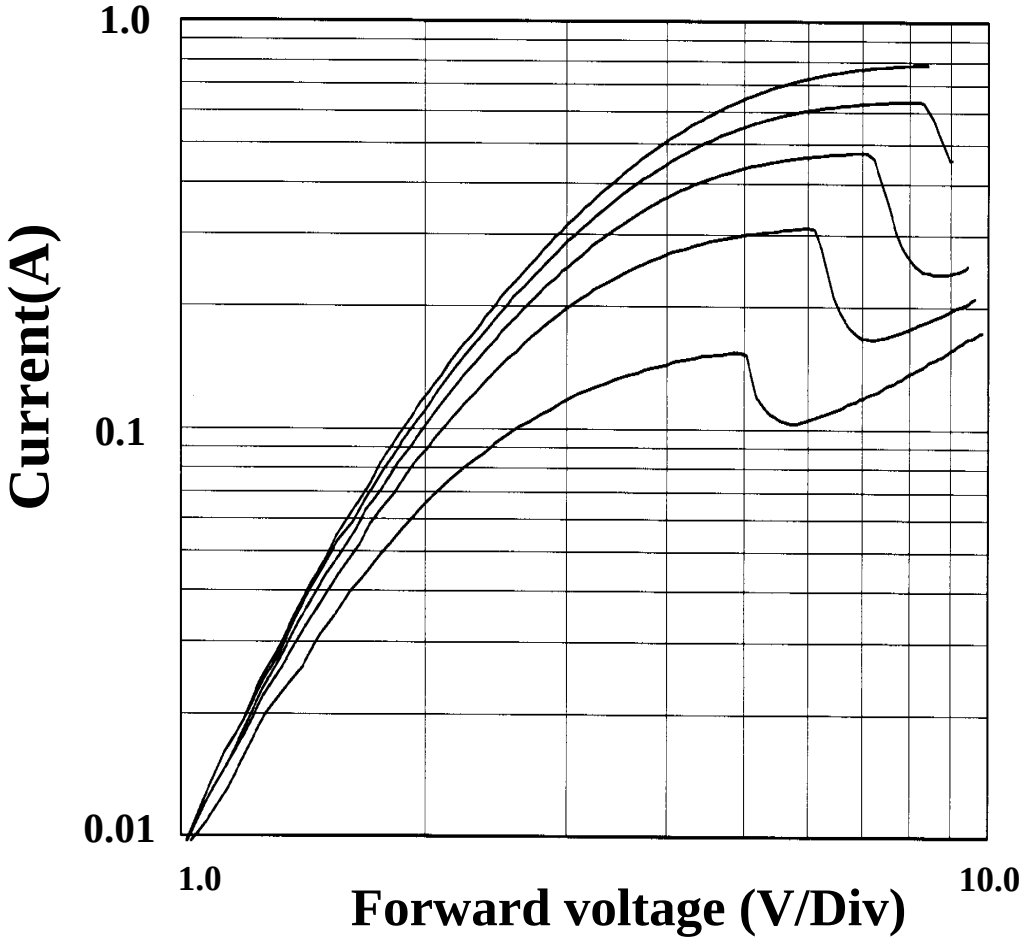


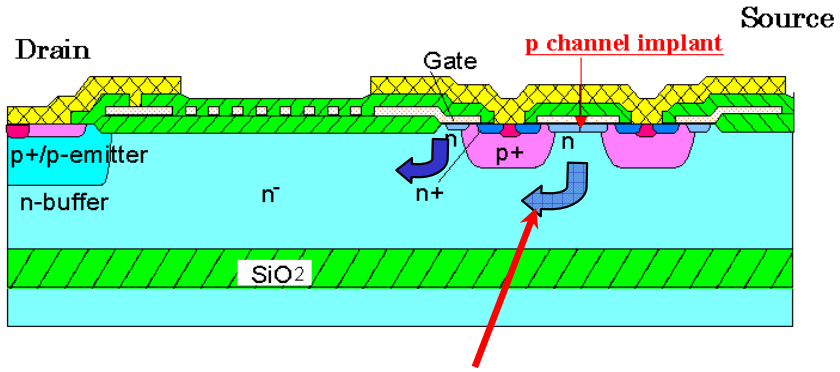
New Multi-chanel IGBT
Vf=3.0V for Drain current of 2.6A(Vg=5.0V)
Device area:1.48mm^2
Vertical axis: 0.5A/Div Horizontal axis: 0.5V/Div

Time: 200nsec/Div
Drain current: 1A/Div

Unique feature of multi-channel LIGBTs

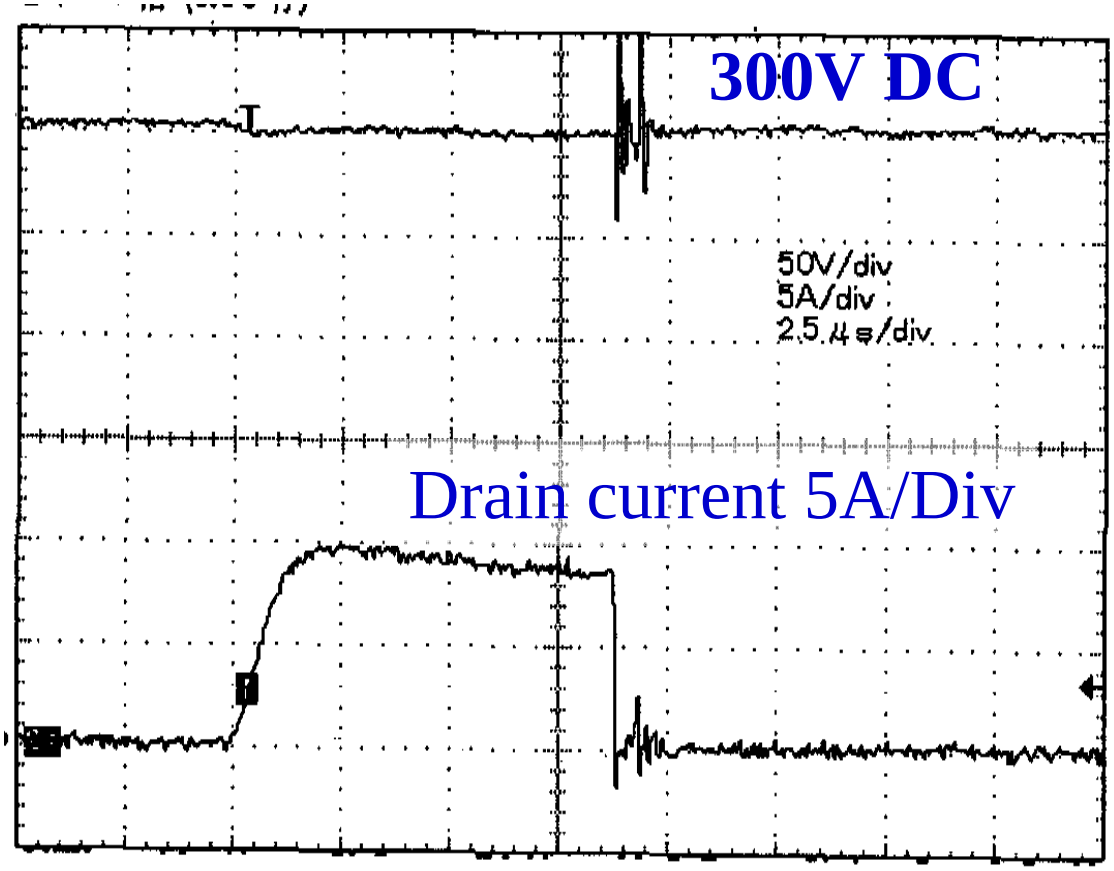
--- Suppressed drain current for high drain voltage due to JFET effect.





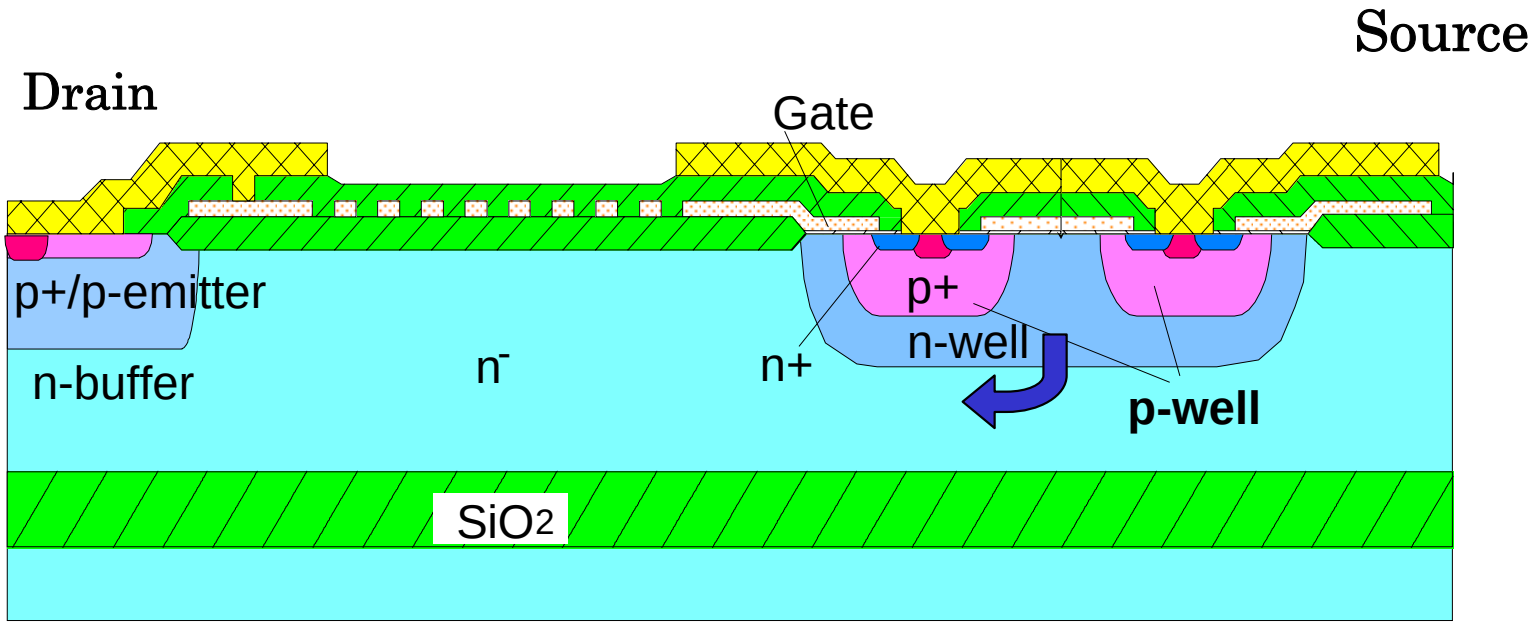
This electron injection is suppressed by formed depletion layer.

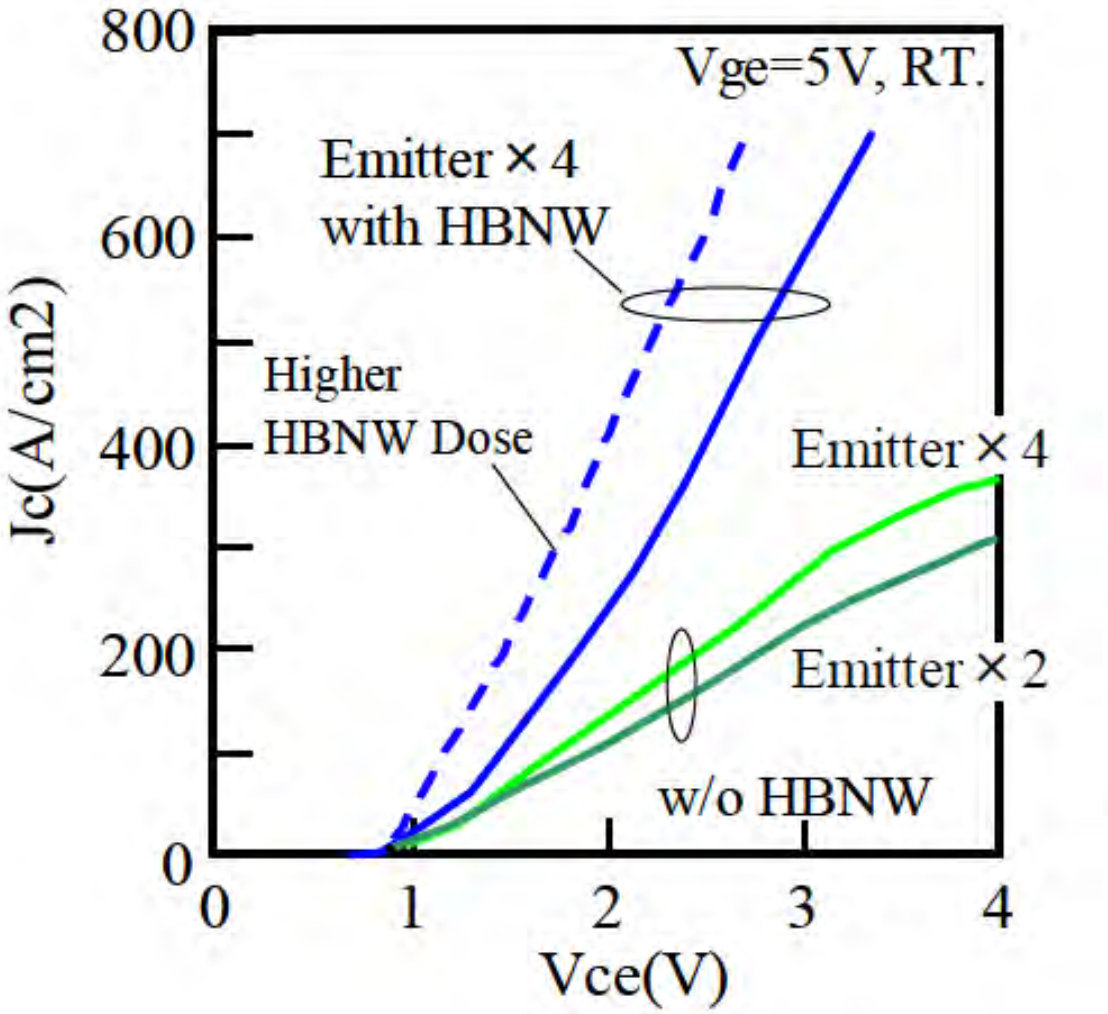
Short circuit withstanding capability of 500V 3A LIGBT

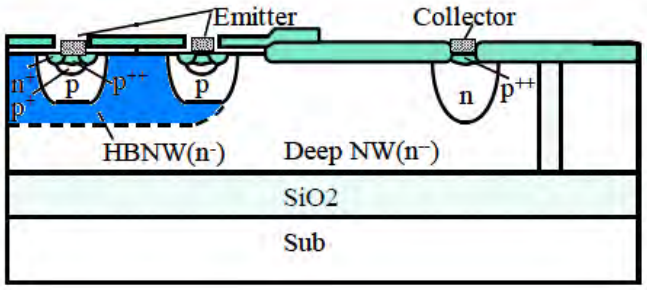


Time (2μs/Div)

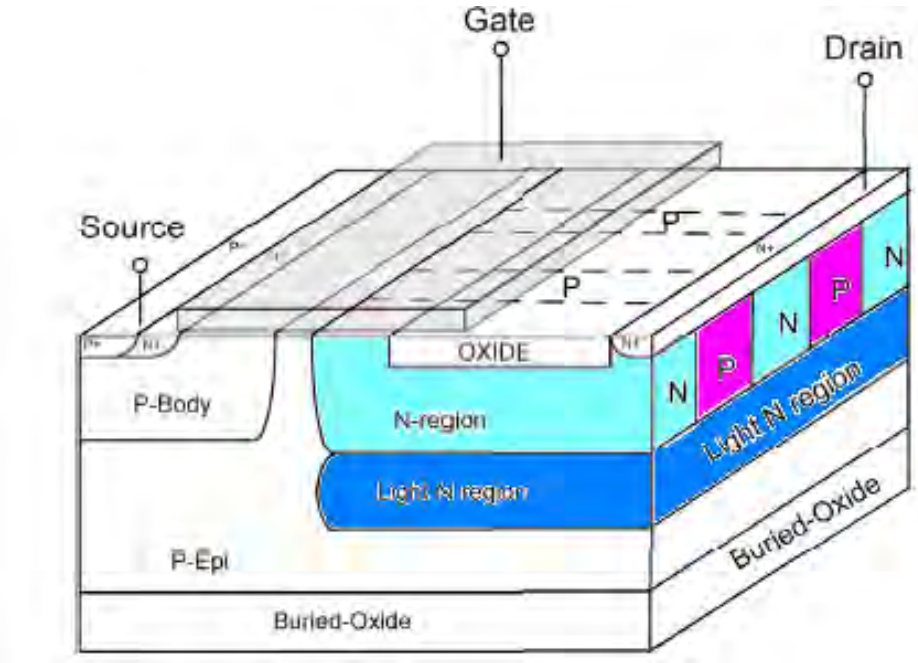
横型IGBTの特性改善
CS-LIGBT



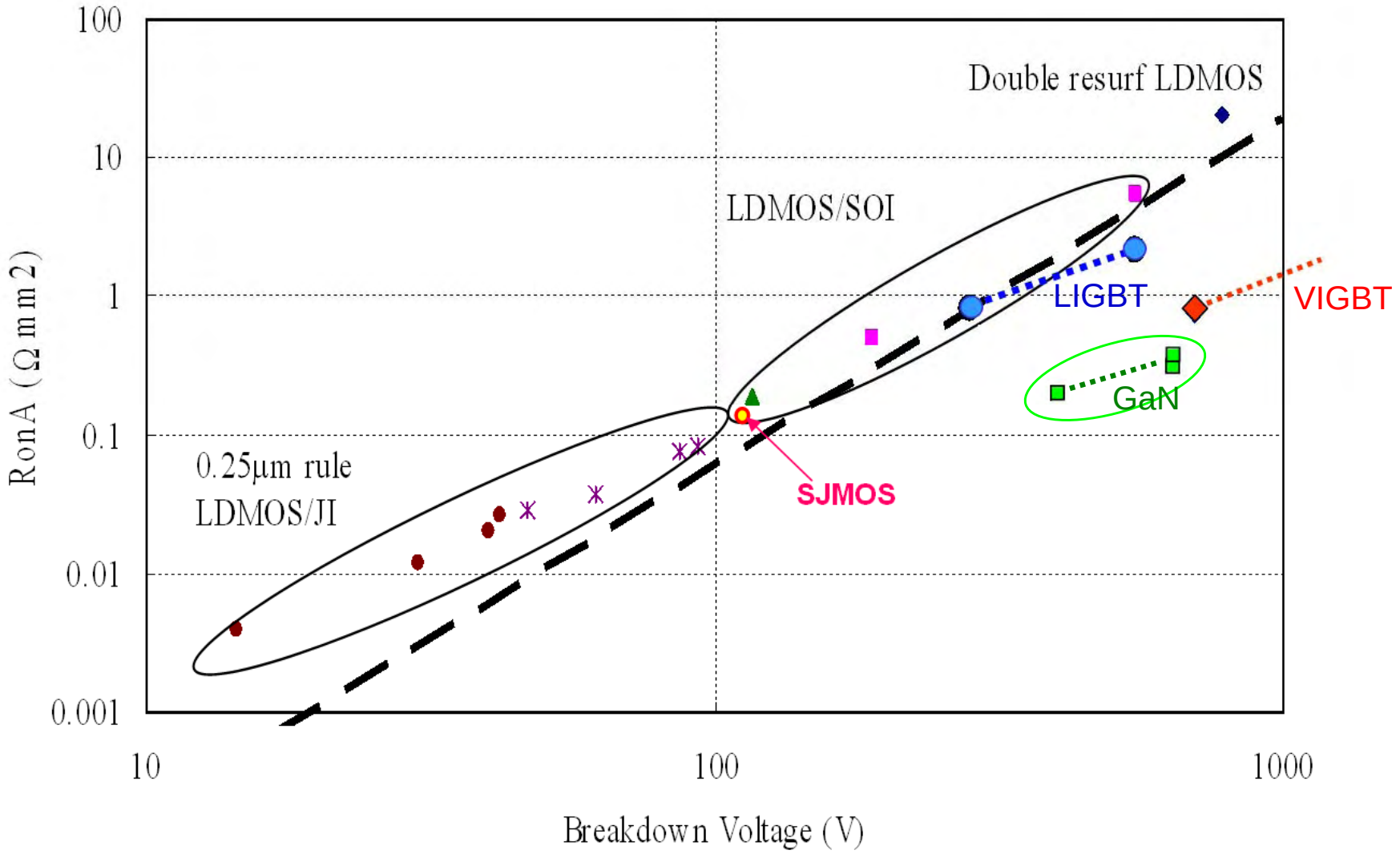

800
600
400
200
0
0
1
2
3
4
Jc(A/cm2)
Vce(V)
Vge=5V, RT.
Emitter × 4
with HBNW
Higher
HBNW Dose
Emitter × 4
Emitter × 2
w/o HBNW


Emitter
Collector
n⁻
p⁻
p
p⁺⁺
p
n
p⁺⁺
HBNW(n⁻)
Deep NW(n⁻)
SiO2
Sub

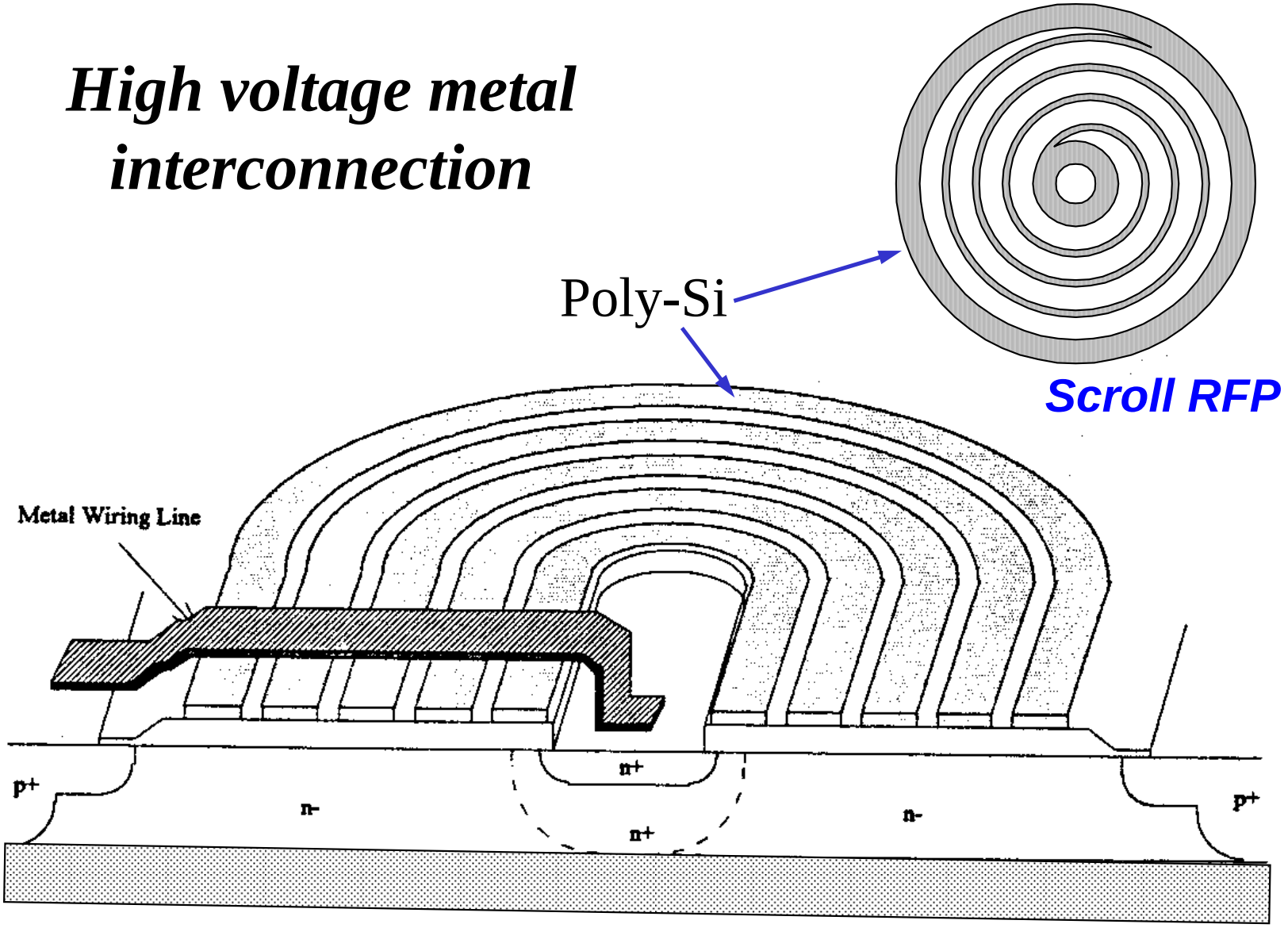
横型素子の改善



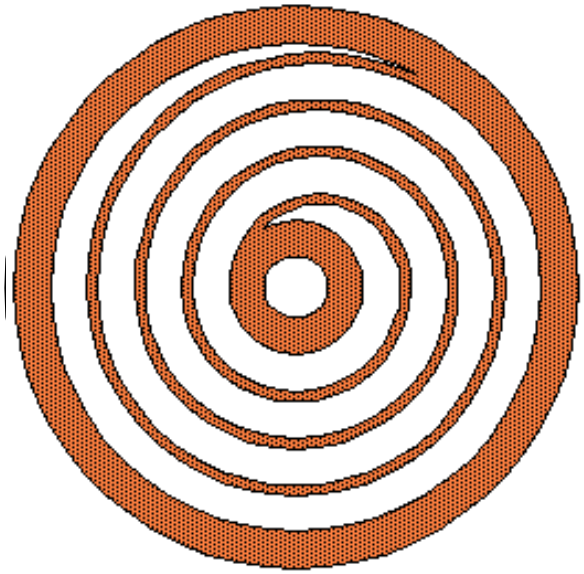
横型SJ素子　　111V,138mΩmm^2


100
10
1
0.1
0.01
0.001
RonA (Ω mm2)
10
100
1000
Breakdown Voltage (V)
Double resurf LDMOS
LDMOS/SOI
LIGBT
VIGBT
GaN
SJMOS
0.25μm rule
LDMOS/JI

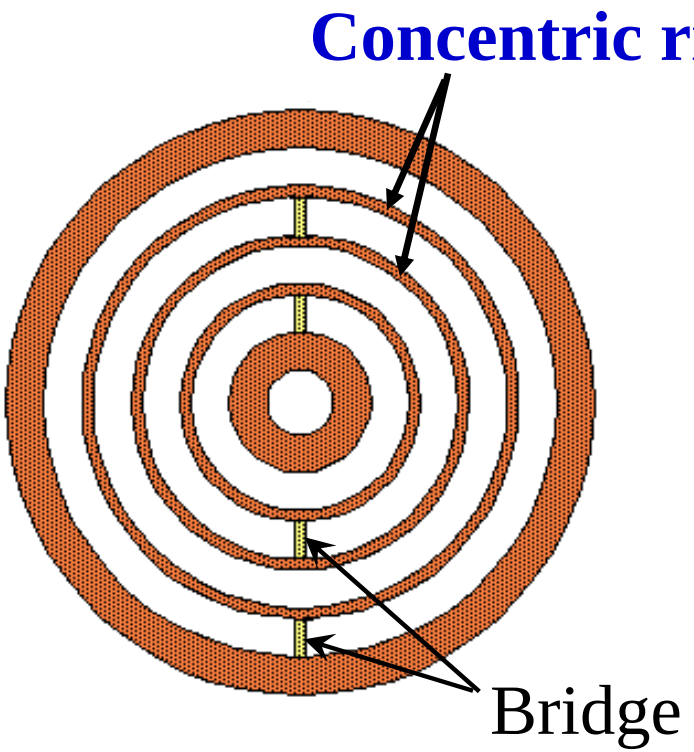
High voltage metal interconnection



Resistive Field Plate (RFP)



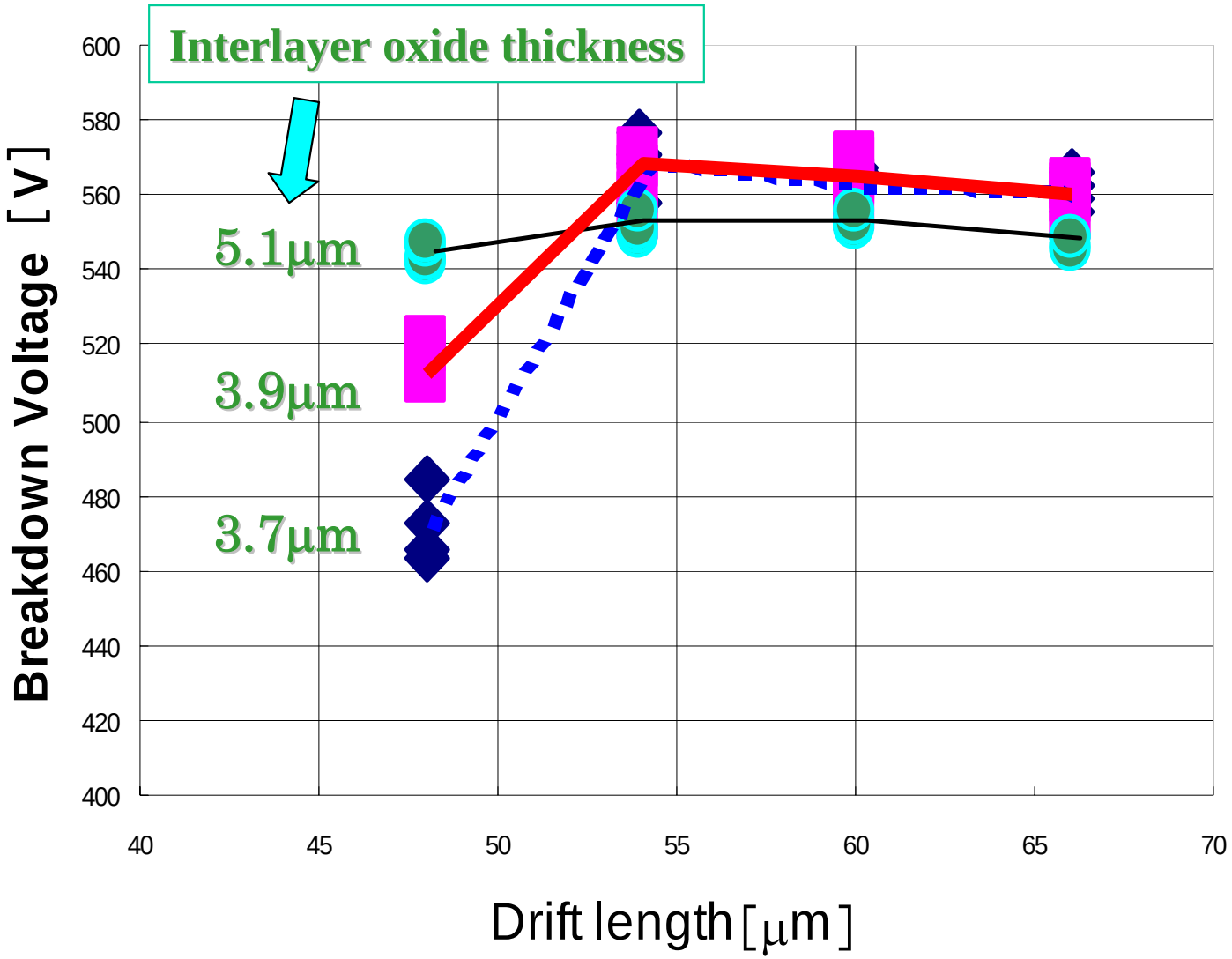
Scroll RFP

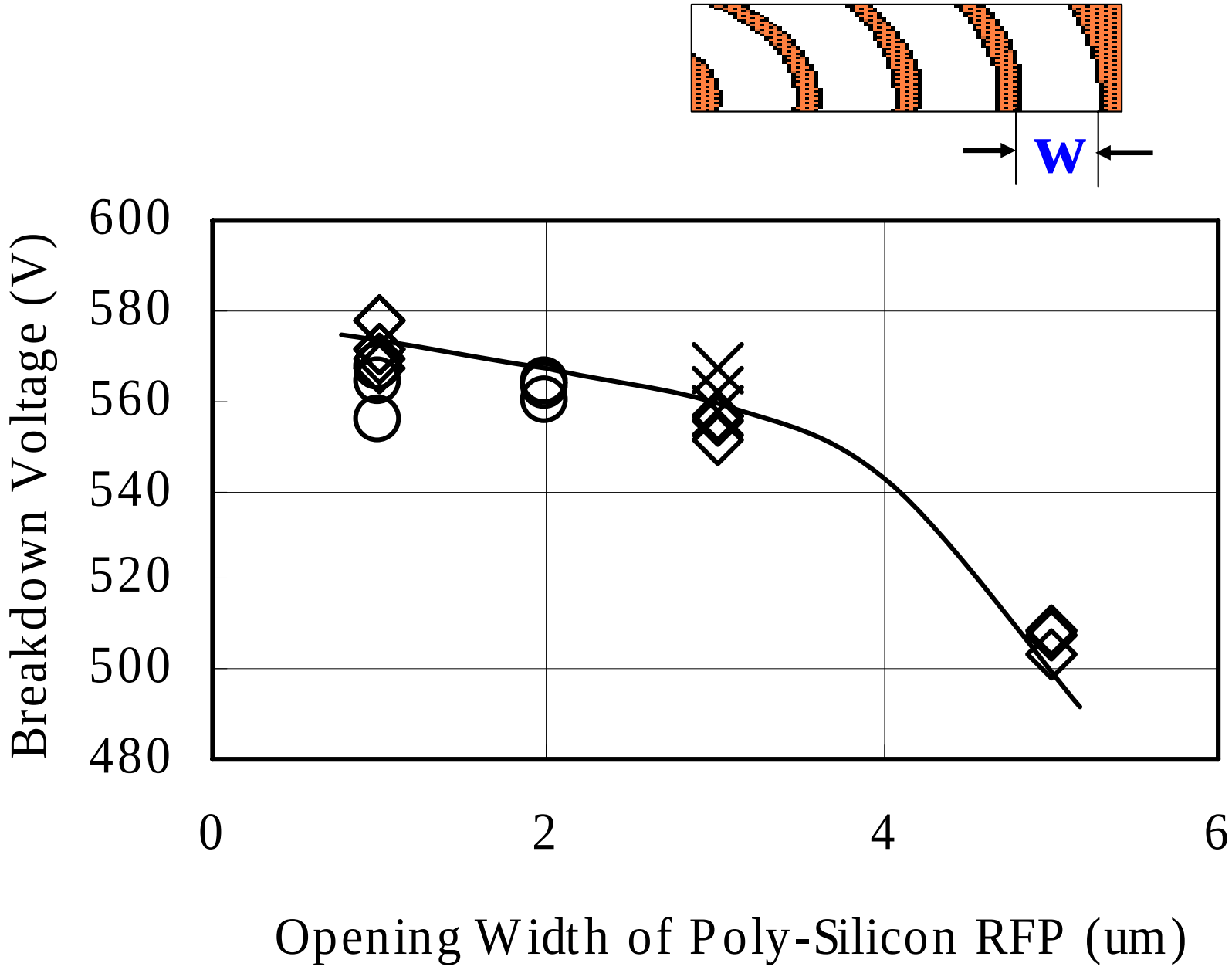


Multi-Ring RFP

Easy to design key parameters
leakage current etc.

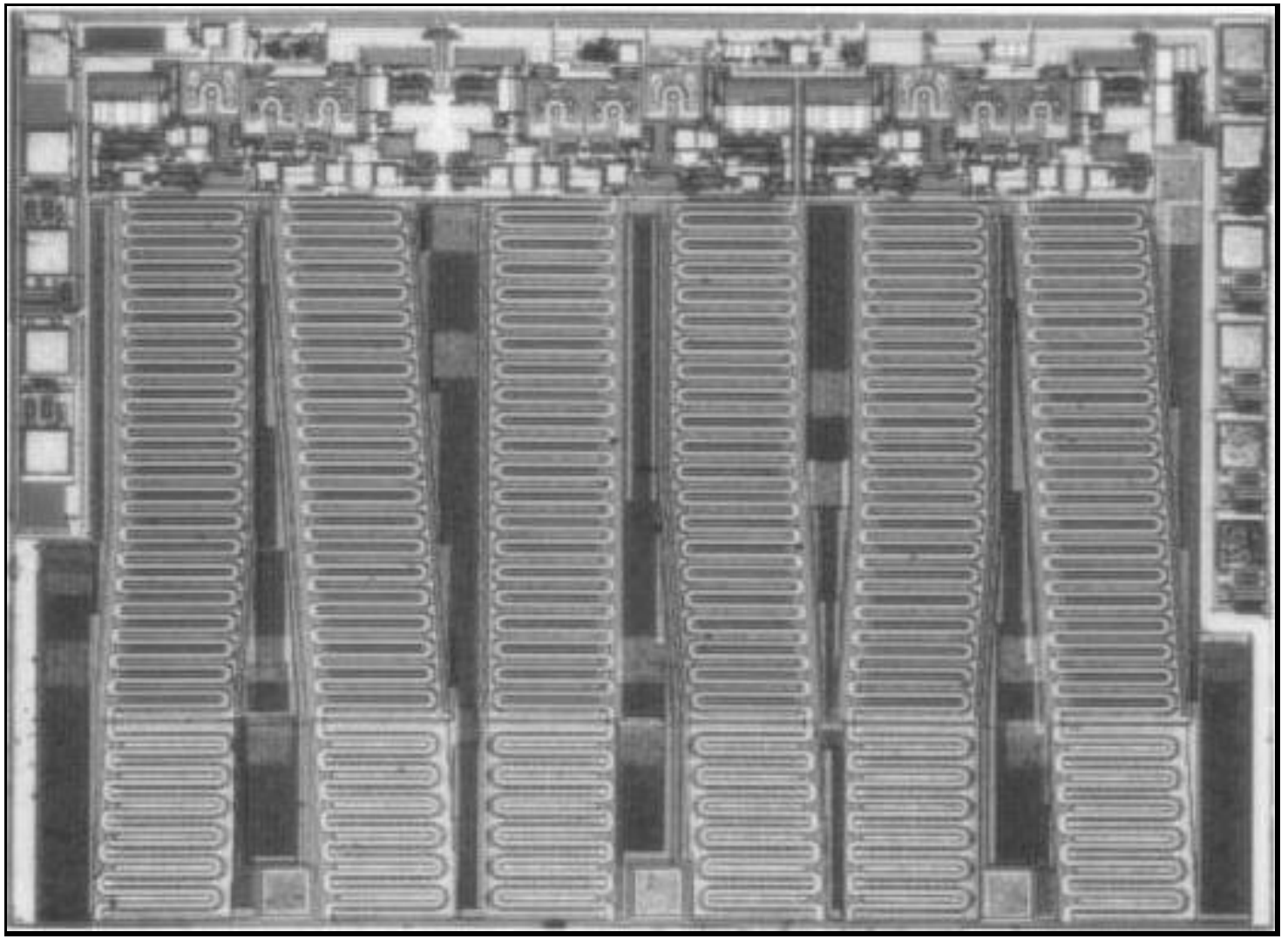
Breakdown Voltage vs. Drift Length



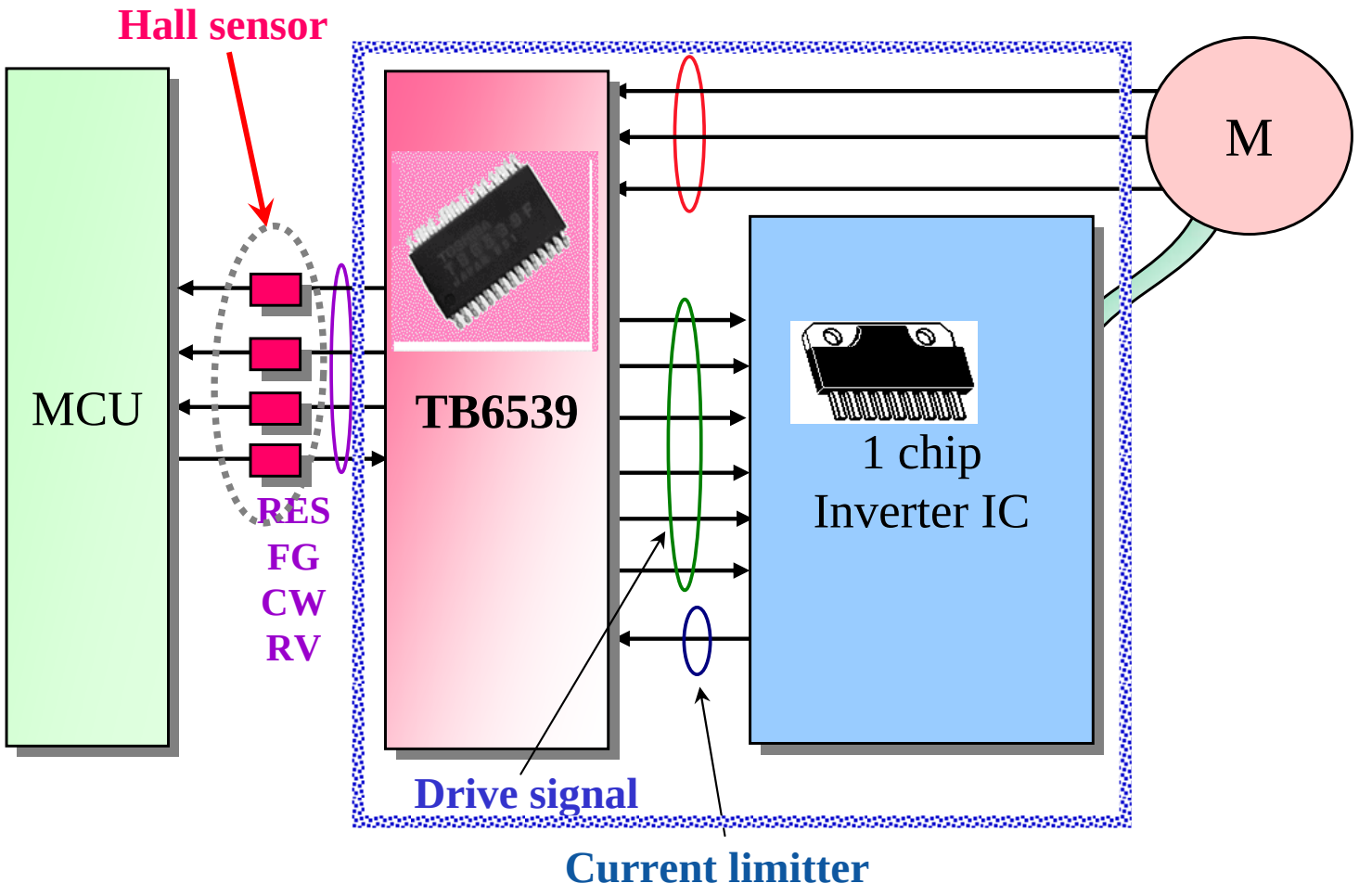

W
600
580
560
540
520
500
480
Breakdown Voltage (V)
0
2
4
6
Opening Width of Poly-Silicon RFP (um)

500V/3A 1chip Inverter IC

1999

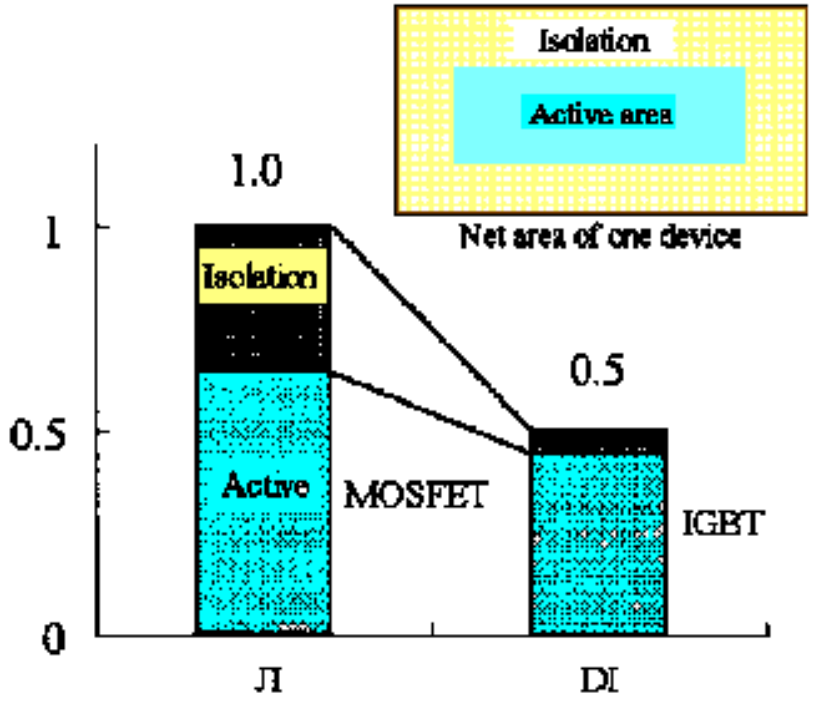


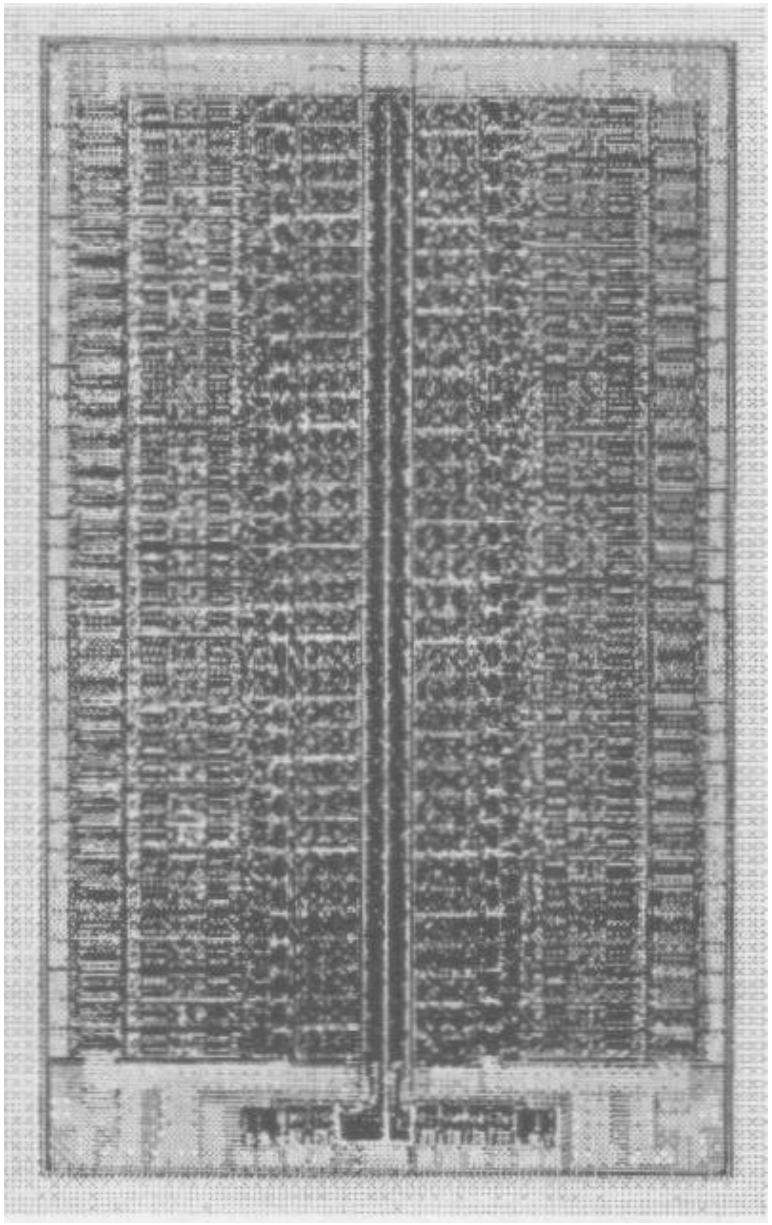
Sinusoidal wave drive is realized by TB6539



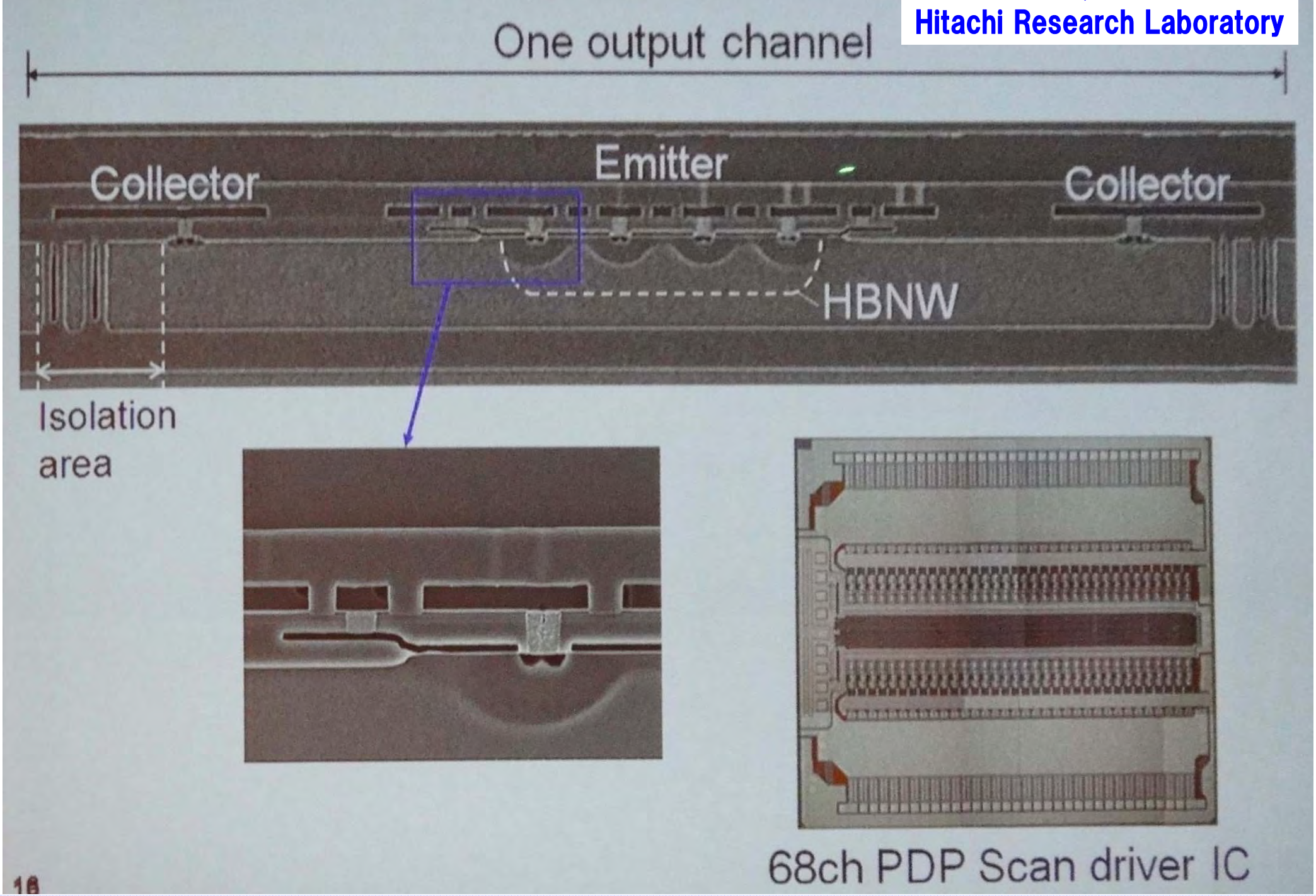
PDP scan driver IC

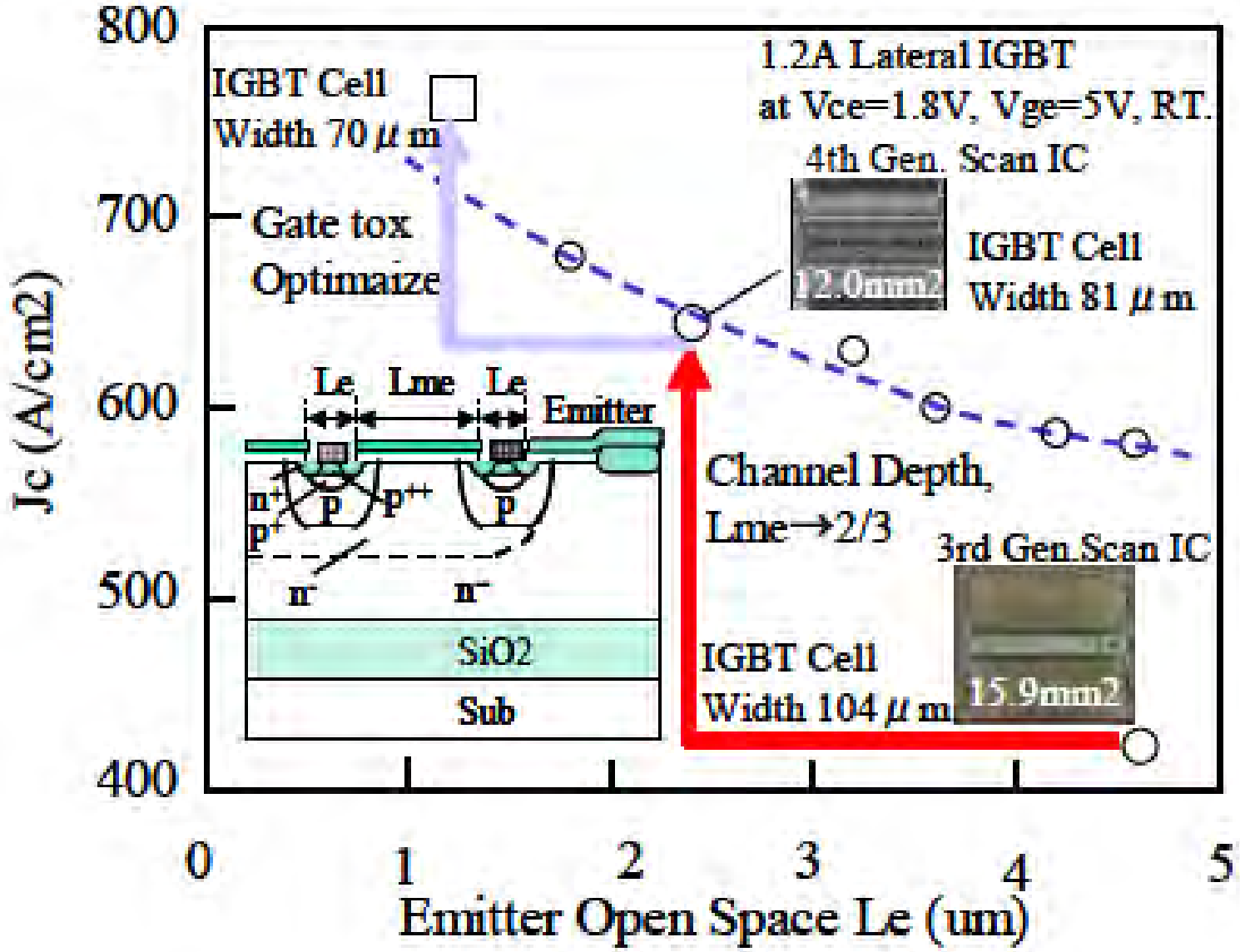
ISPSD'98 (Fuji electric)





ISPSD' 2010, J.Sakano他
Hitachi Research Laboratory

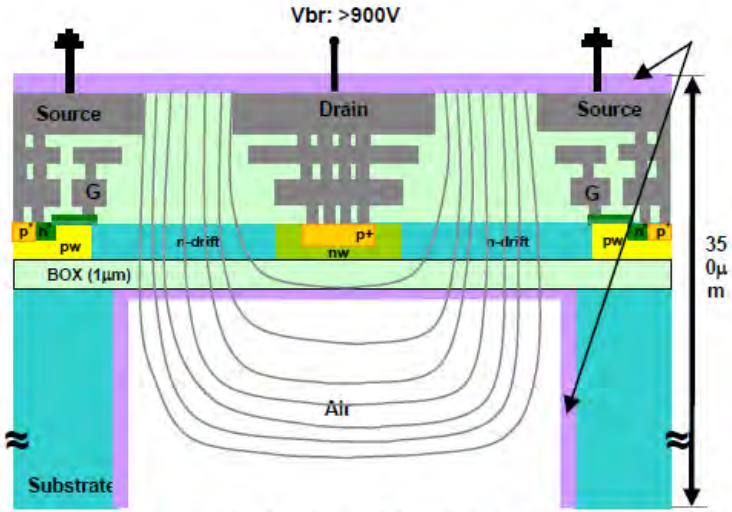



800
700
600
500
400
Jc (A/cm2)
0
1
2
3
4
5
Emitter Open Space Le (um)
IGBT Cell
Width 70 μm
1.2A Lateral IGBT
at Vce=1.8V, Vge=5V, RT.
4th Gen. Scan IC
12.0mm2
IGBT Cell
Width 81 μm
Gate tox
Optimaize
Le
Lme
Le
Emitter
n+
p+
P
p++
P
n-
n-
SiO2
Sub
Channel Depth,
Lme→2/3
3rd Gen.Scan IC
15.9mm2
IGBT Cell
Width 104 μm

Releasing new power semiconductor technology: The start-up company route

Gehan A. J. Amaratunga

ISPSD' 2009



(b) Selective anisotropic back etching of the substrate (in this case with the Buried Oxide acting as an etch stop) removes the substrate earth plane and a allows near ideal potential distribution. It also improves switching performance by minimizing drain-source capacitance C_{oss}.

CamSemi

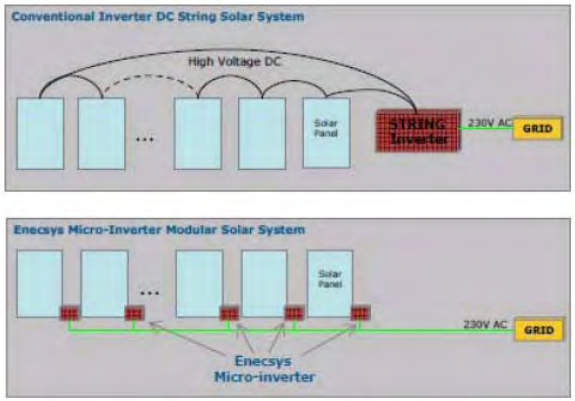


Fig 4. Conventional PV system with central inverter (with PV panels connected in series for HV DC) compared to the micro-inverter PV system(with PV panels connected in parallel with AC output)

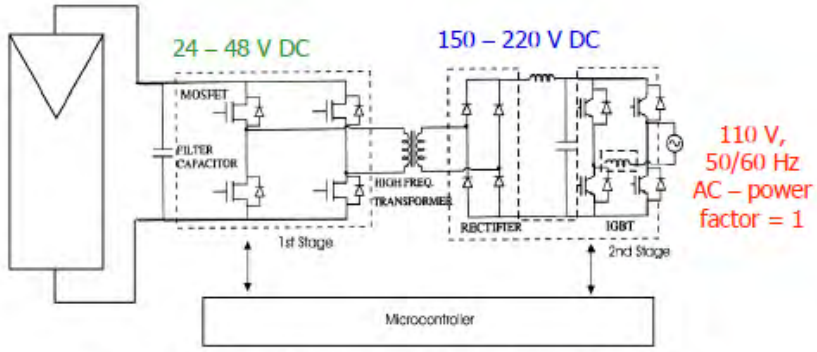


Fig 2. Two H-bridge topology for a solar module inverter

Fig 3 (a) Single chip with all power devices and drive shown enclosed in broken lines in Fig. 2

Enecsys