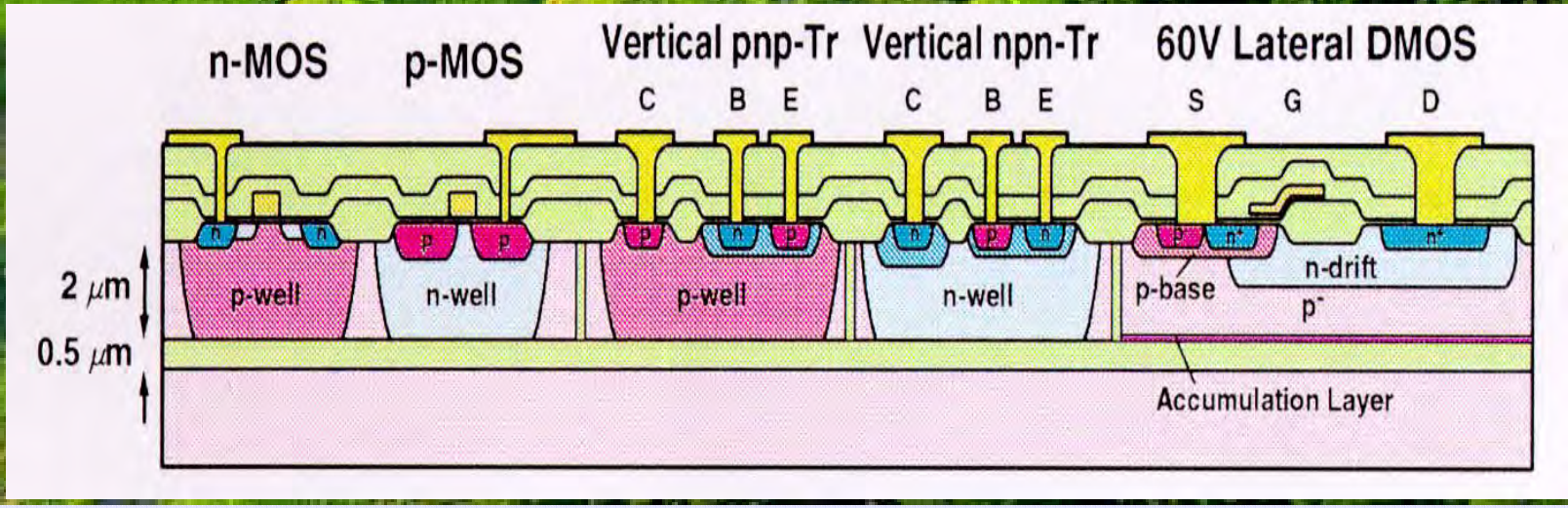
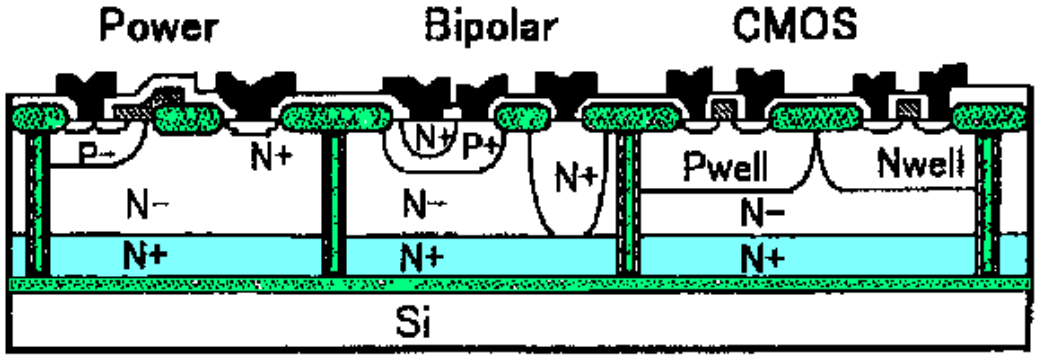
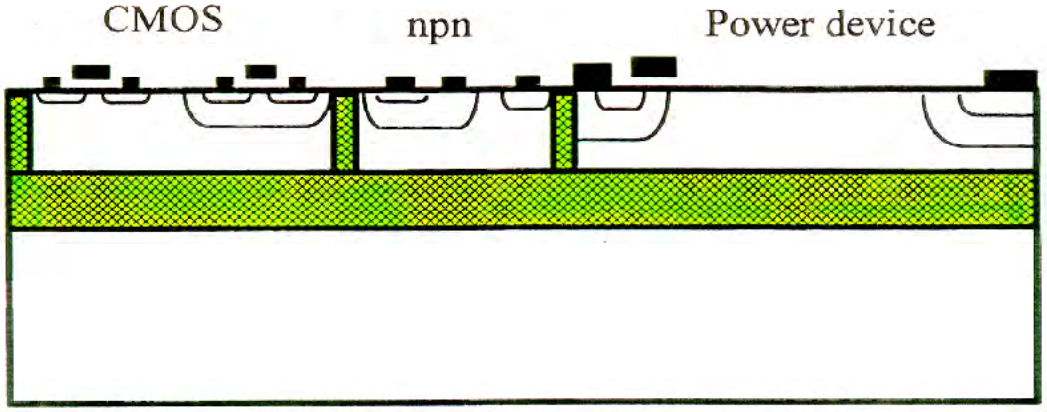
Toward system integration
車載用BCD on SOI



Two SOI wafer structures



（1）SOI with n^+ buried layer（デンソー）



（2）Simple SOI

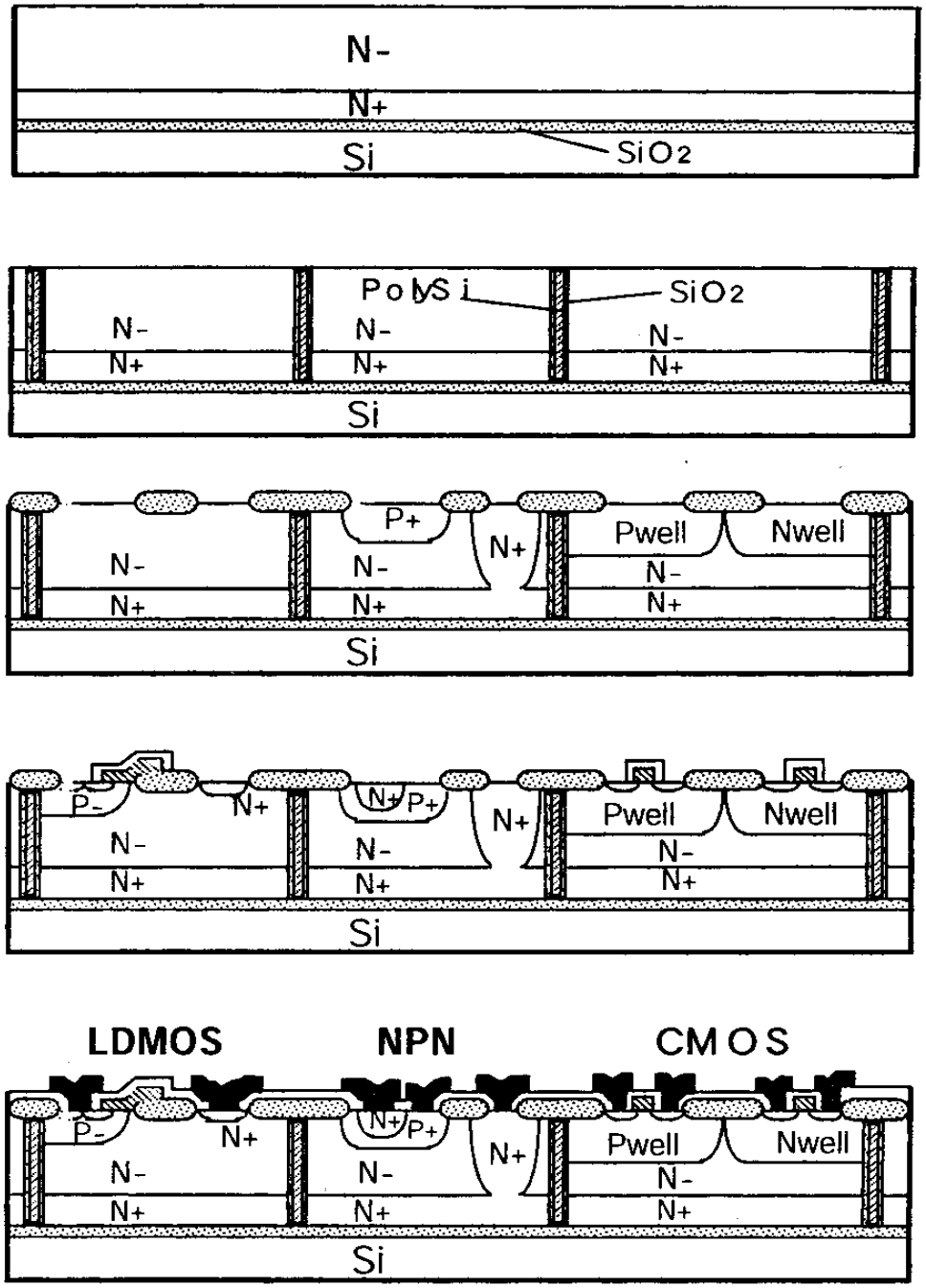

N-
N+
Si
SiO2
PolySi
SiO2
N-
N+
P+
N+
Pwell
Nwell
P-
LDMOS
NPN
CMOS
Si

Table 1 Process flow overview

Process step	notes
SOI wafer	Nsub / buried N+ / SiO_2 / Psub
Trench	16 μ m depth
Pwell / Nwell	relate to all devices
LOCOS	relate to all devices
gate	relate to CMOS, LDMOS
ch P	relate to LDMOS
S.D. (n+/p+)	relate to all devices
Metallization	2 level

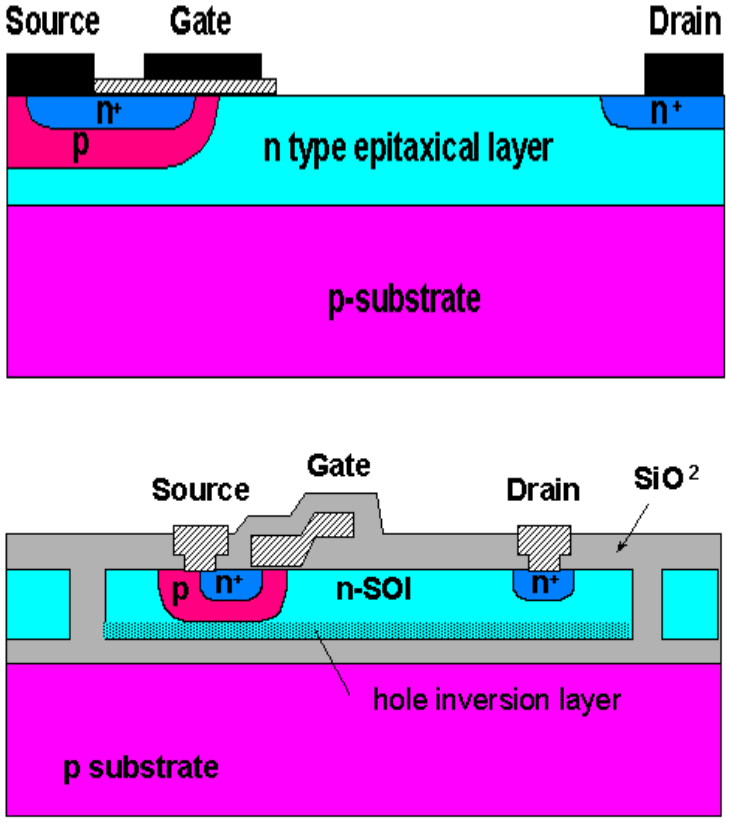
Table 2 Electrical characteristics of standard devices

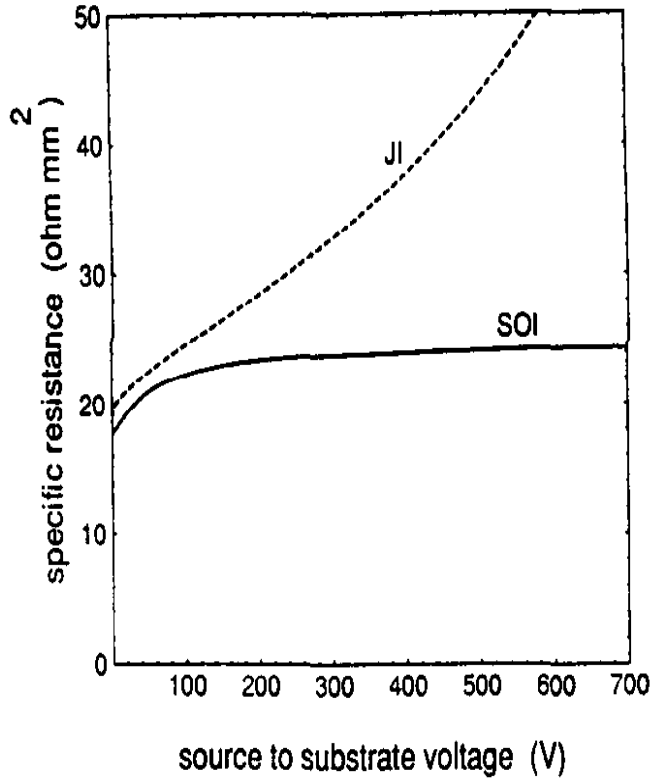
Devices	Parameter	Typical Value
NPN	hFE @Ic=10 μ A	180
	BVceo	50V
	BVcbo	150V
L-PNP	hFE @Ic=10 μ A	300
	BVceo	50V
	BVebo	100V
Zenner Diode	Vz	8.3V
NMOS	Vt @Vds=0.1V	1.1V
	Id @Vgs=Vds=5V	110 μ A/μ m
	BVdss	13V
PMOS	Vt @Vds=0.1V	1.2V
	Id @Vgs=Vds=5V	60 μ A/μ m
	BVdss	15V
HV-PMOS	Vt @Vds=0.1V	1.5V
	Id @Vgs=Vds=5V	20 μ A/μ m
	BVdss	70V
EPROM	Vt @Vds=1V	1.3V
	dVt Vpp=12V,1msec	5.0V
LDMOS	Vt @Vds=5V	1.2V
	Ron @Si only	160m Ω/mm²
	Ron @include metal	195m Ω/mm²
	BVdss	65V

Table 3 Electrical characteristics of option devices

Option Devices	Parameter	Typical Value
VDMOS	Vt @Vds=5V	1.2V
	Ron @Si only	300m Ω/mm²
	Ron @include metal	350m Ω/mm²
	BVdss	70V
Resistor (CrSiN)	sheet resistance	500 Ω/□
	TCR	-2ppm/℃
Resistor (HR-Poly Si)	sheet resistance	500 Ω/□
	TCR	-300ppm/℃

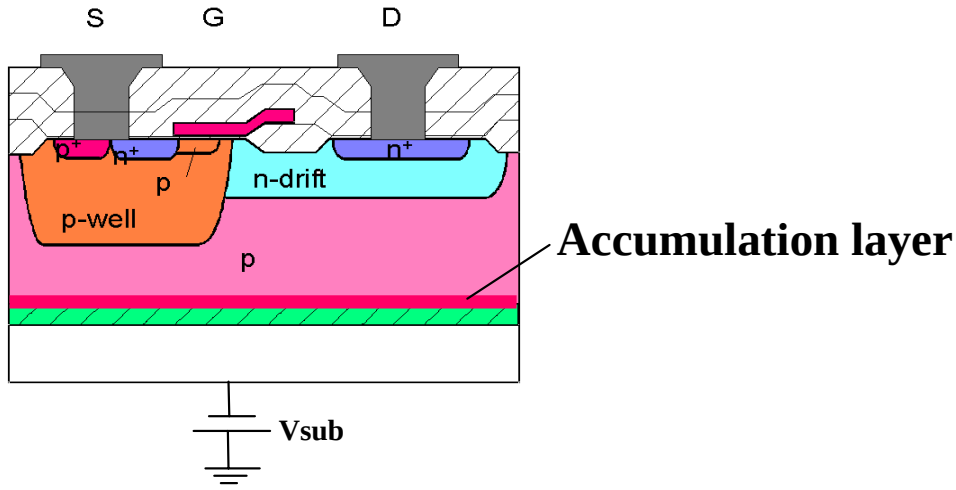
Substrate bias influence on on-resistance

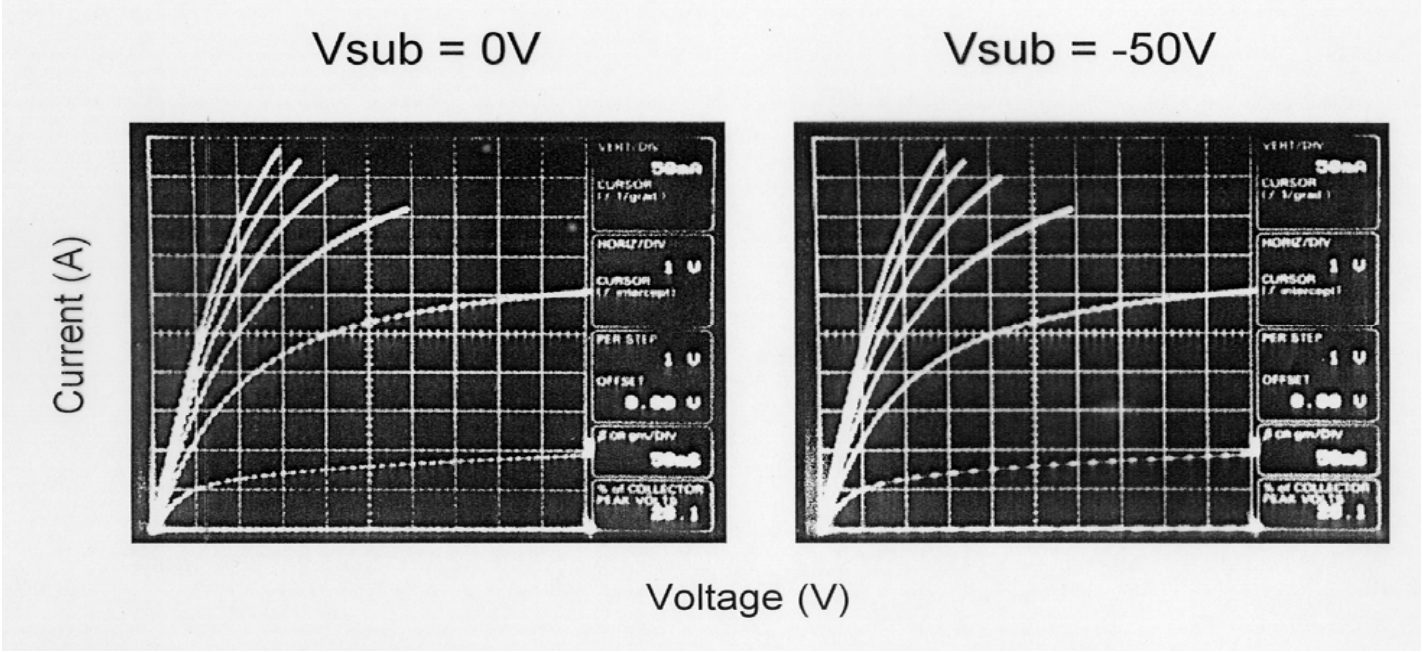




60V Lateral MOSFET

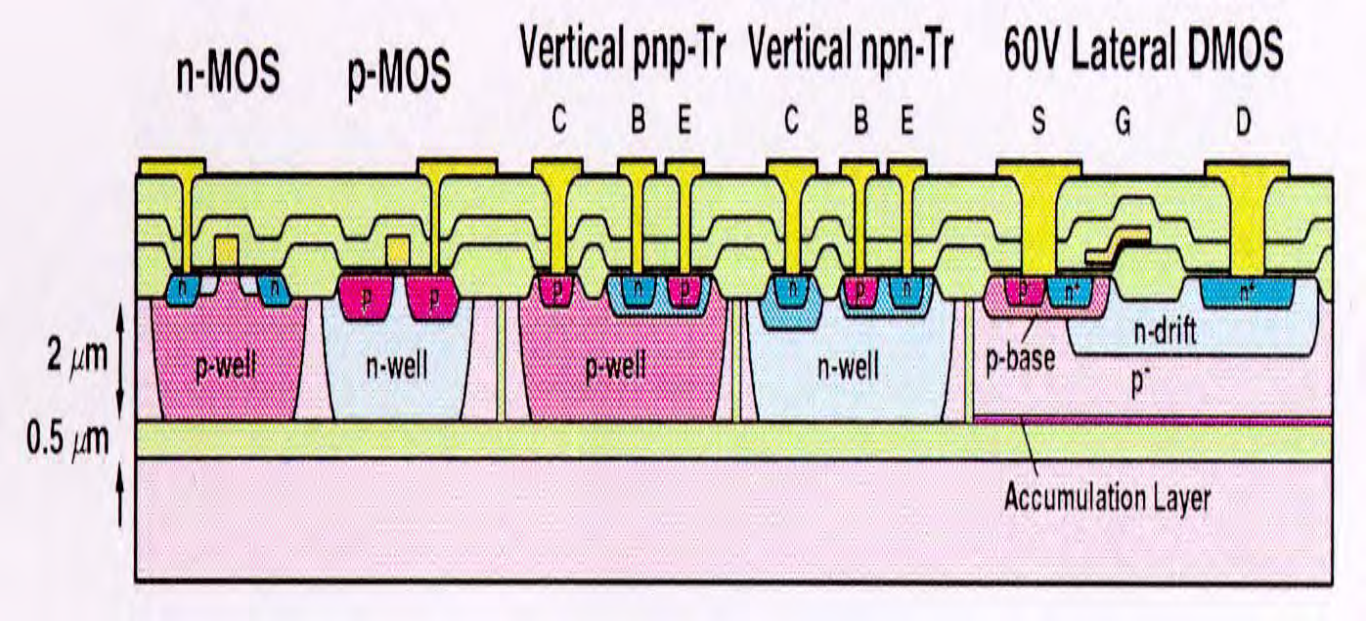
1995 IEDM

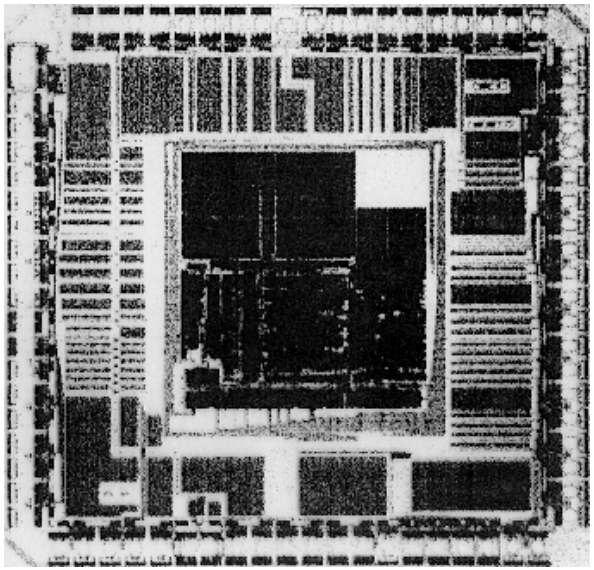




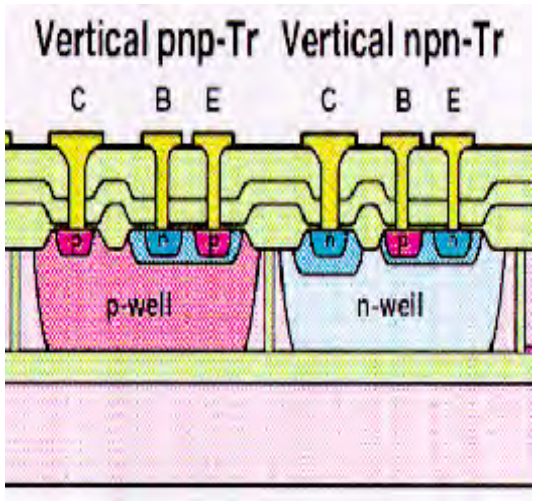
Toward system integration

- Small warpage: Fine lithography.
- CMOS process compatible.
- Integration of 4bit MPU was demonstrated in 1995.

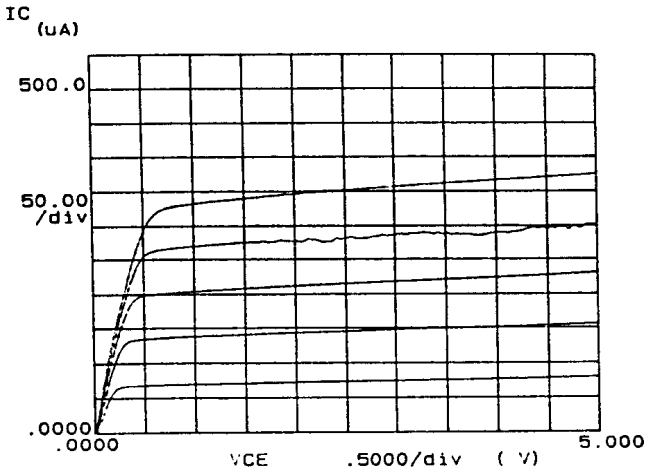




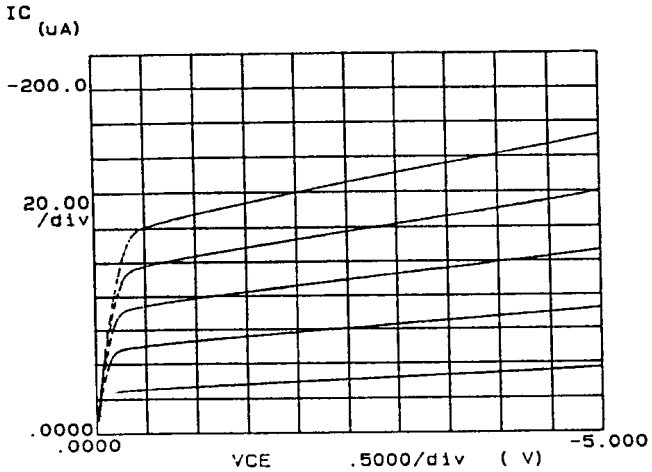
Good Bip Tr. Without buried layers



npn



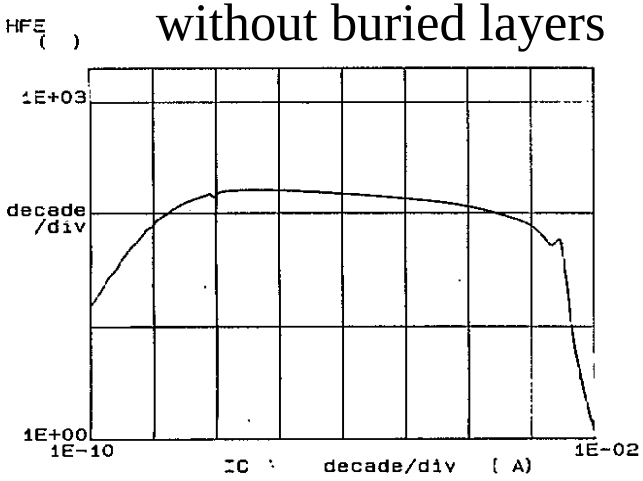
pnp



48mm^2

npn on SOI

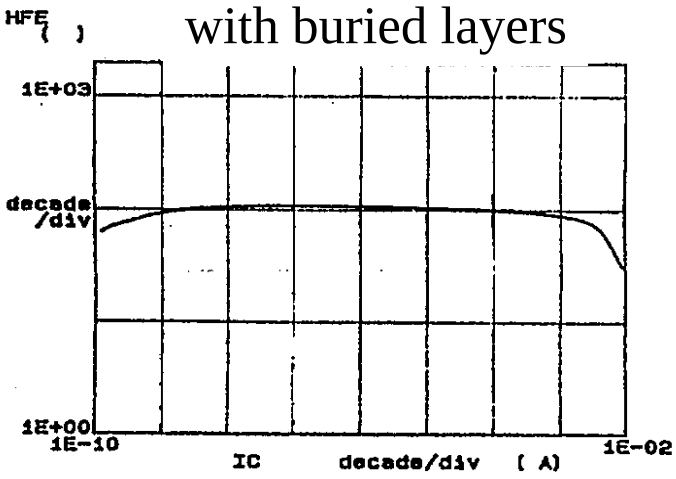
without buried layers



114mm^2

npn on the bulk

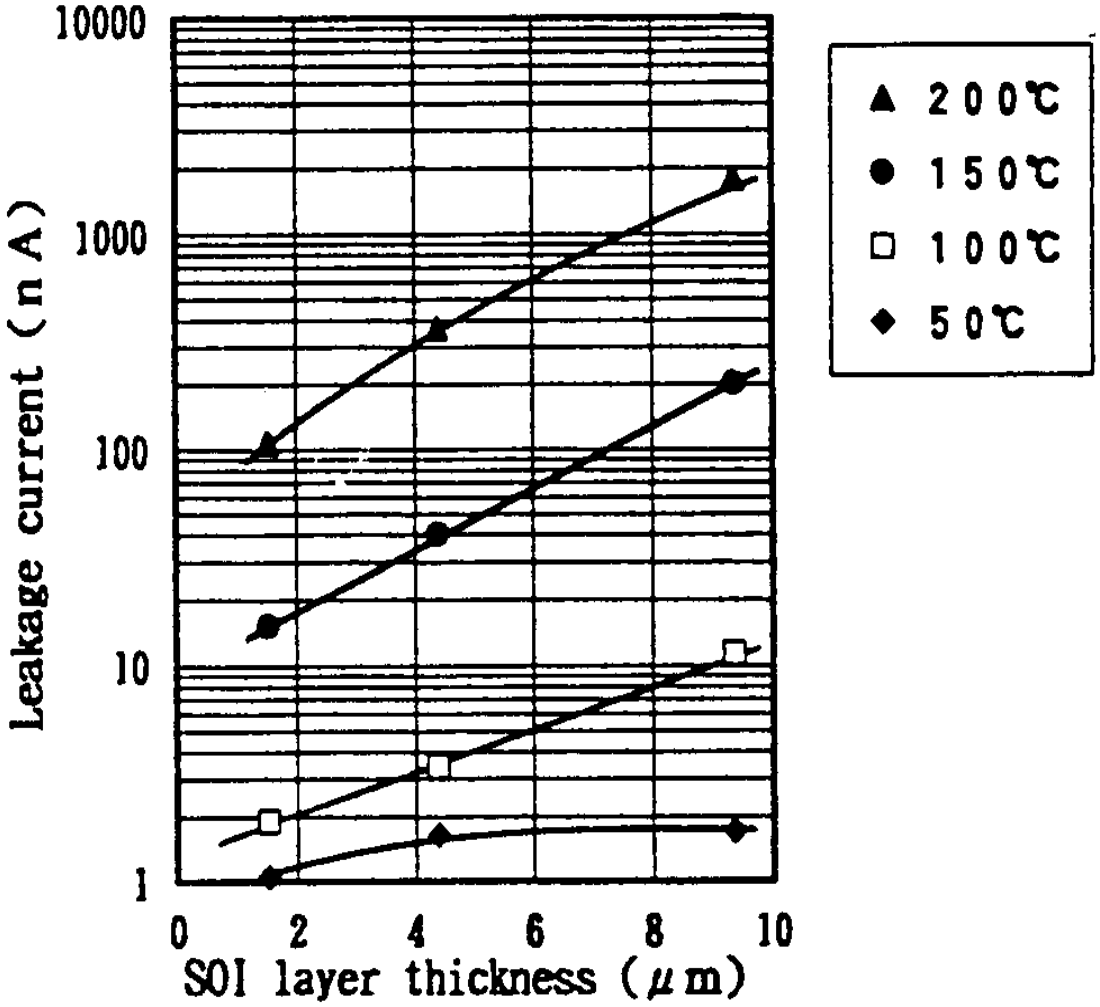
with buried layers

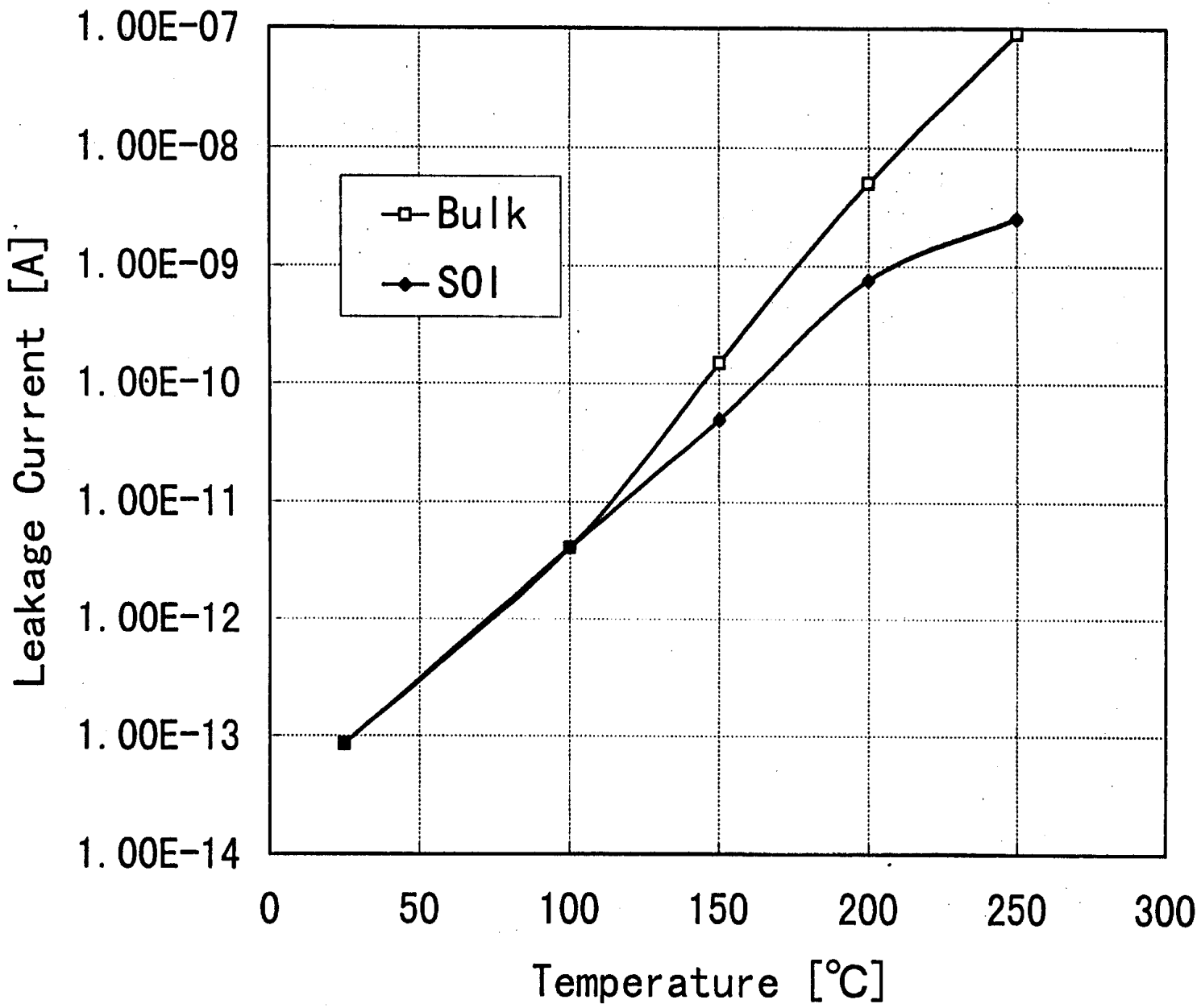


高温動作

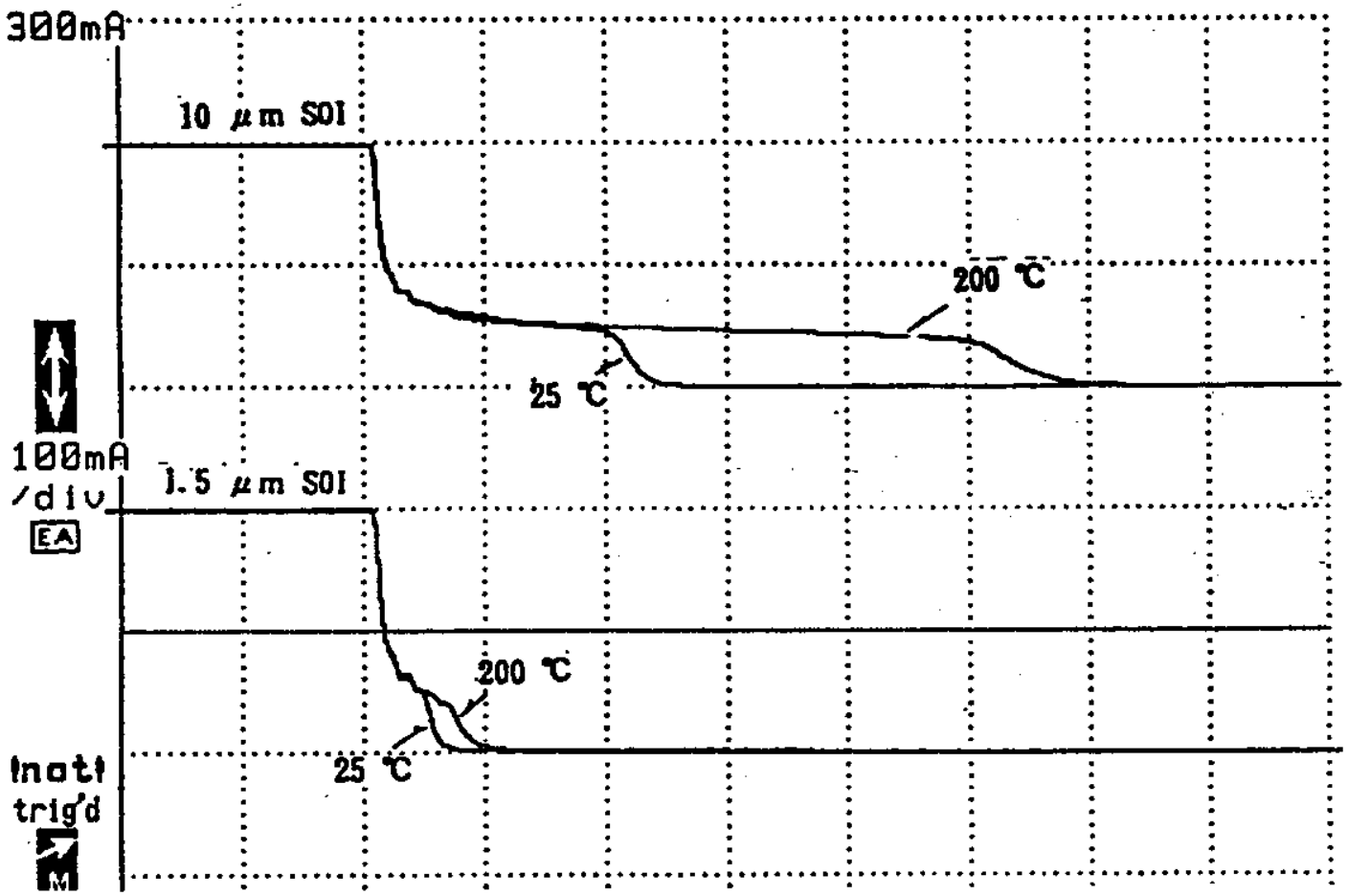
High Temperature Operation

Leakage current vs. SOI thickness

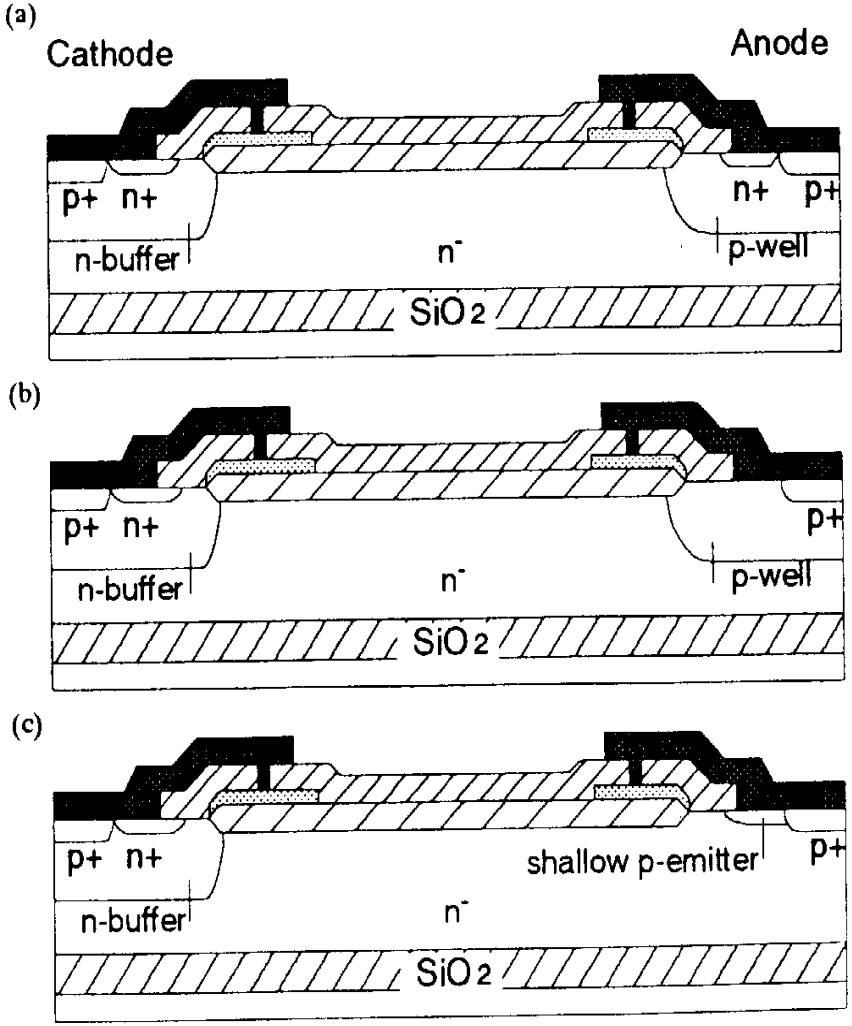


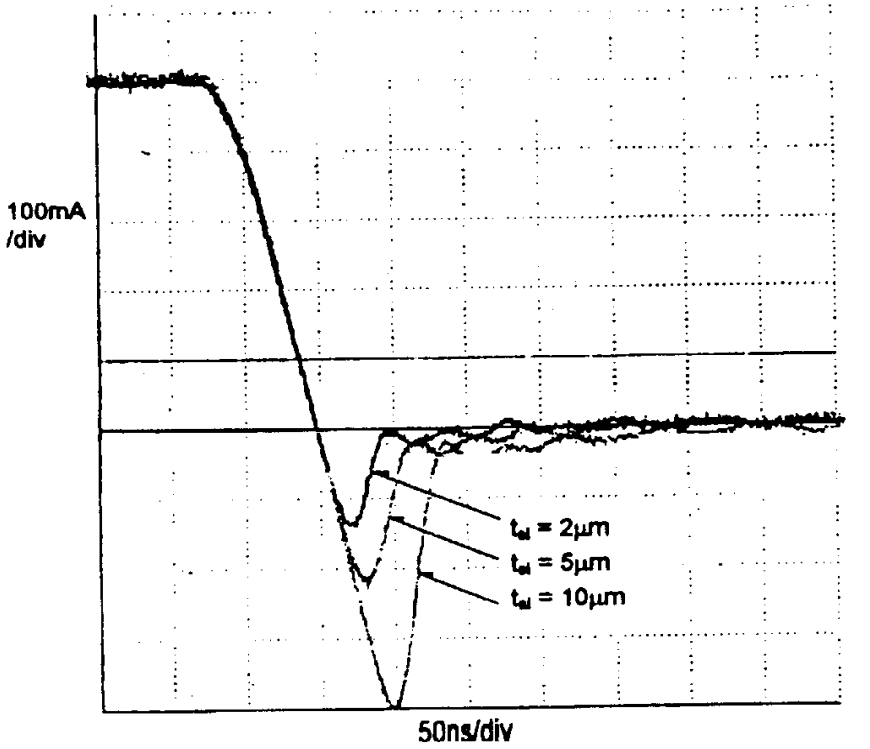

1.00E-07
1.00E-08
1.00E-09
1.00E-10
1.00E-11
1.00E-12
1.00E-13
1.00E-14
Leakage Current [A]
Bulk
SOI
0
50
100
150
200
250
300
Temperature [℃]

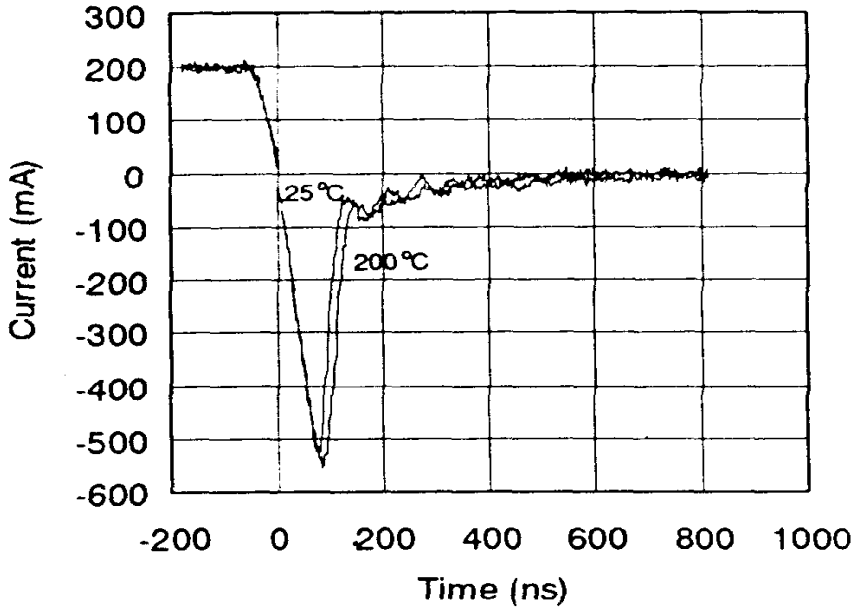
LIGBT in thinner SOI exhibits faster switching speed and less temperature dependence



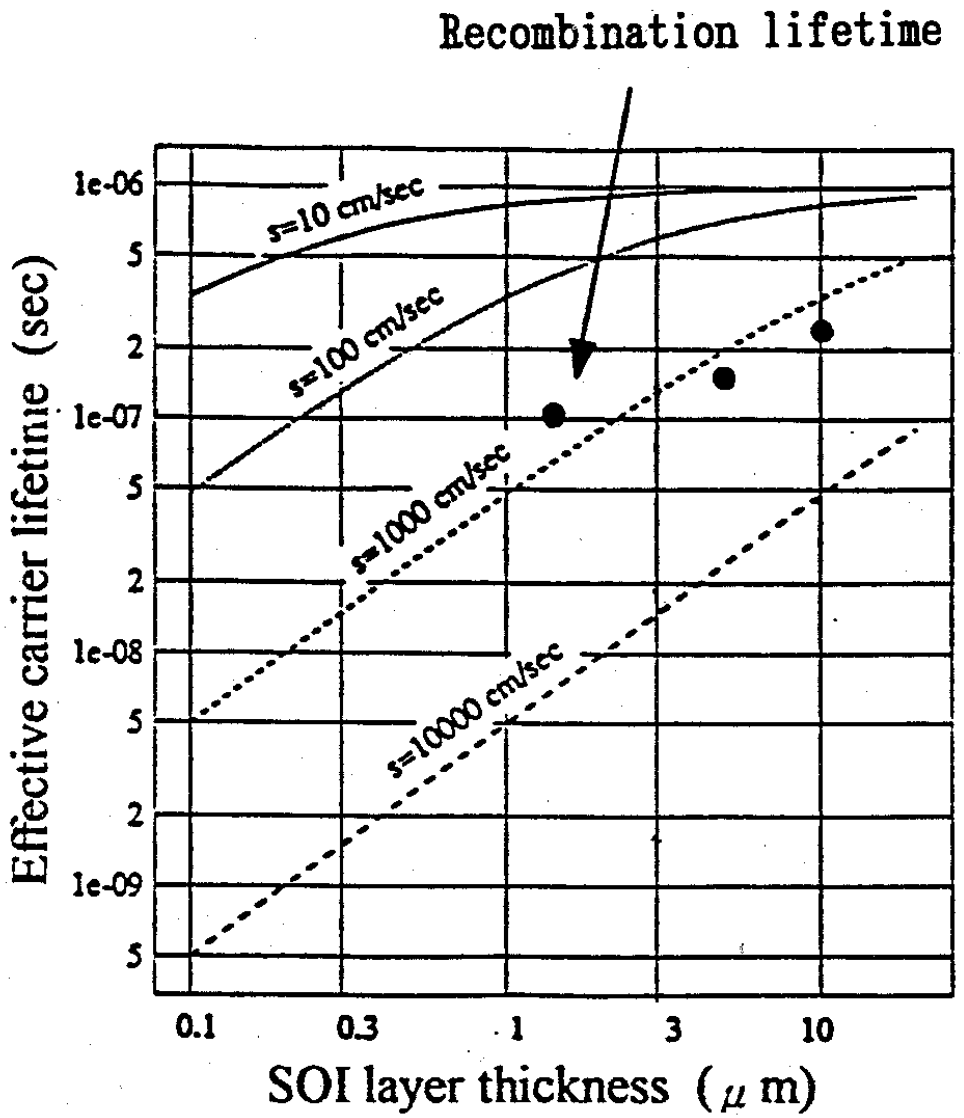
SOI Diode


(a)
Cathode
Anode
p+ n+
n+ p+
n-buffer
n-
p-well
SiO2
(b)
p+ n+
p+
n-buffer
n-
p-well
SiO2
(c)
p+ n+
shallow p-emitter
p+
n-buffer
n-
SiO2


100mA
/div
t_{epi} = 2μm
t_{epi} = 5μm
t_{epi} = 10μm
50ns/div


300
200
100
0
-100
-200
-300
-400
-500
-600
Current (mA)
25℃
200℃
-200
0
200
400
600
800
1000
Time (ns)

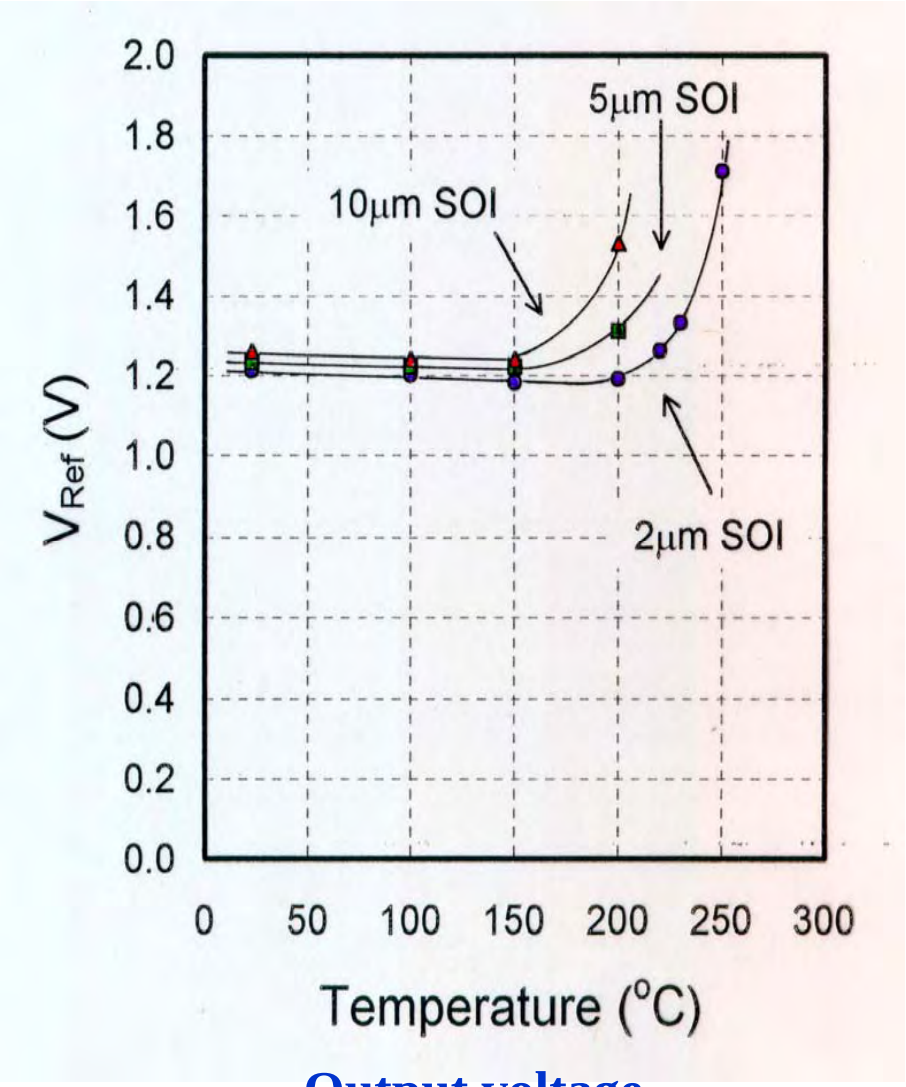
リーク電流少なく、スイッチングスピードは速い



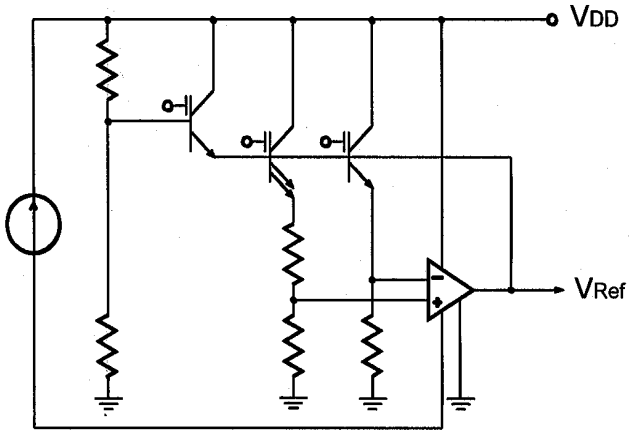
$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{(S_U + S_B)}{t_{SOI}}$$

SOI thickness	1.5 μm	5 μm	10 μm
Recombination lifetime	102.2 ns	151.4 ns	235.7 ns
Generation lifetime	3.46 μs	5.34 μs	4.59 μs

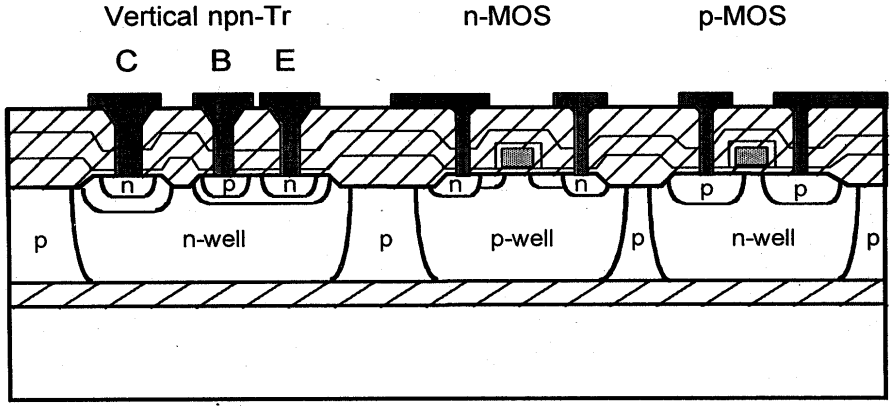
200 °C operation of bandgap reference circuit



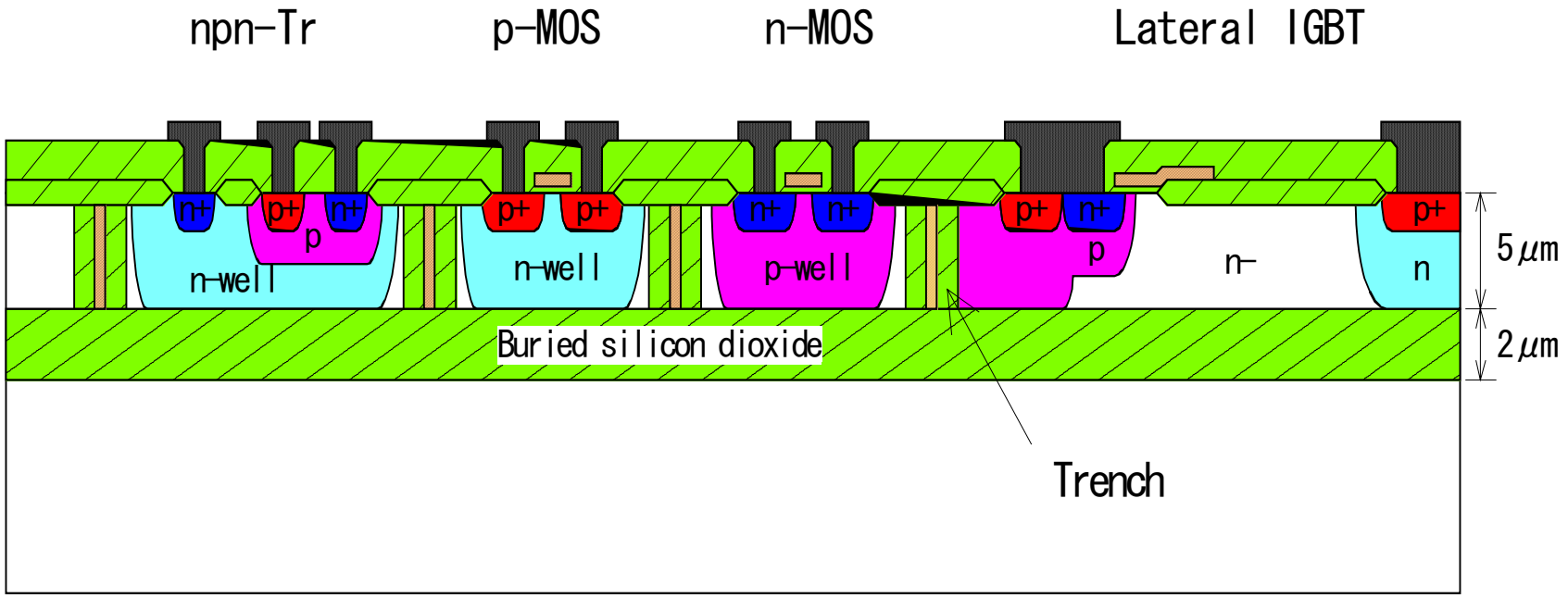
Output voltage of bandgap reference circuit



Block diagram

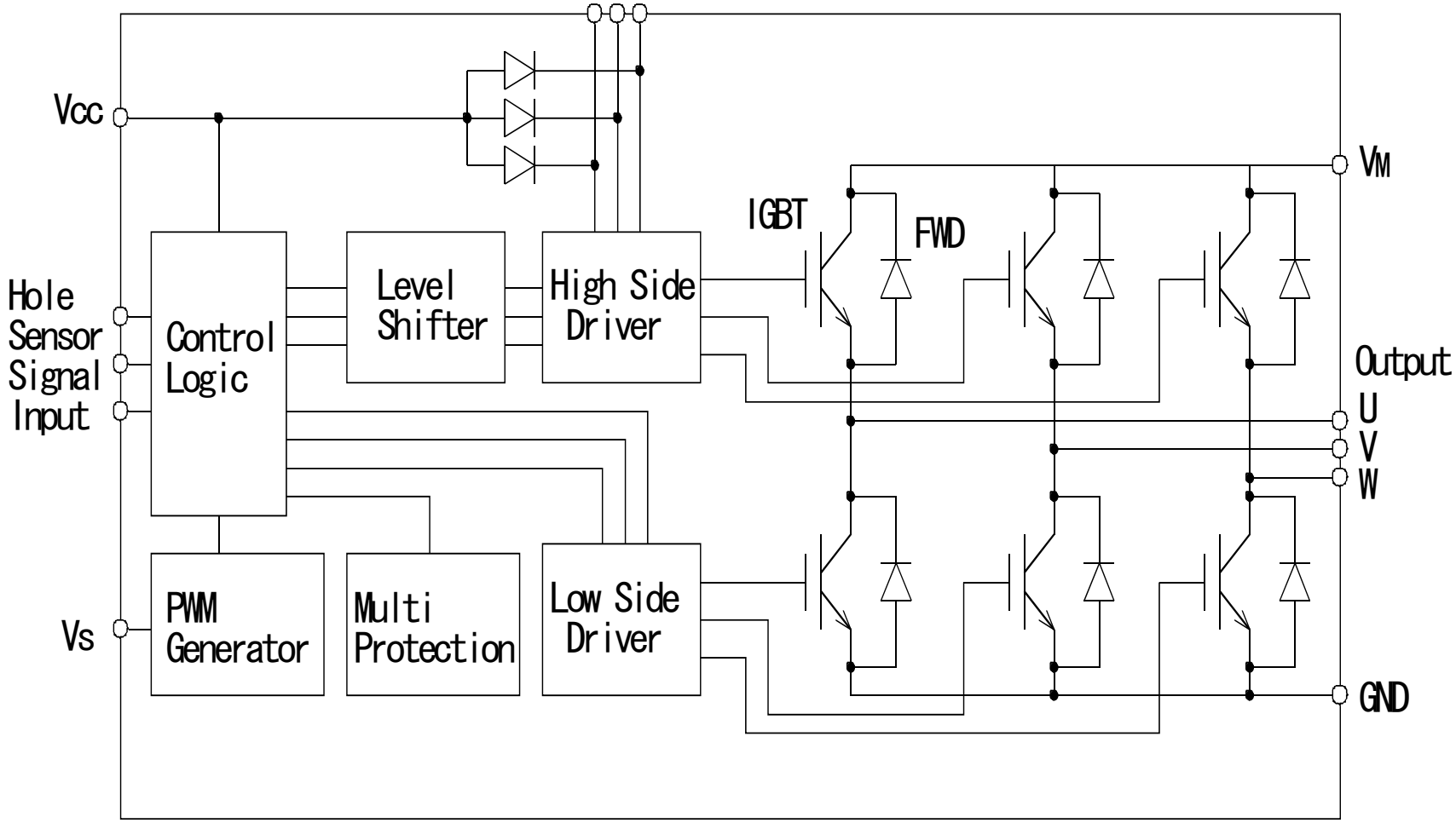


200 °C Operation of thin SOI power ICs

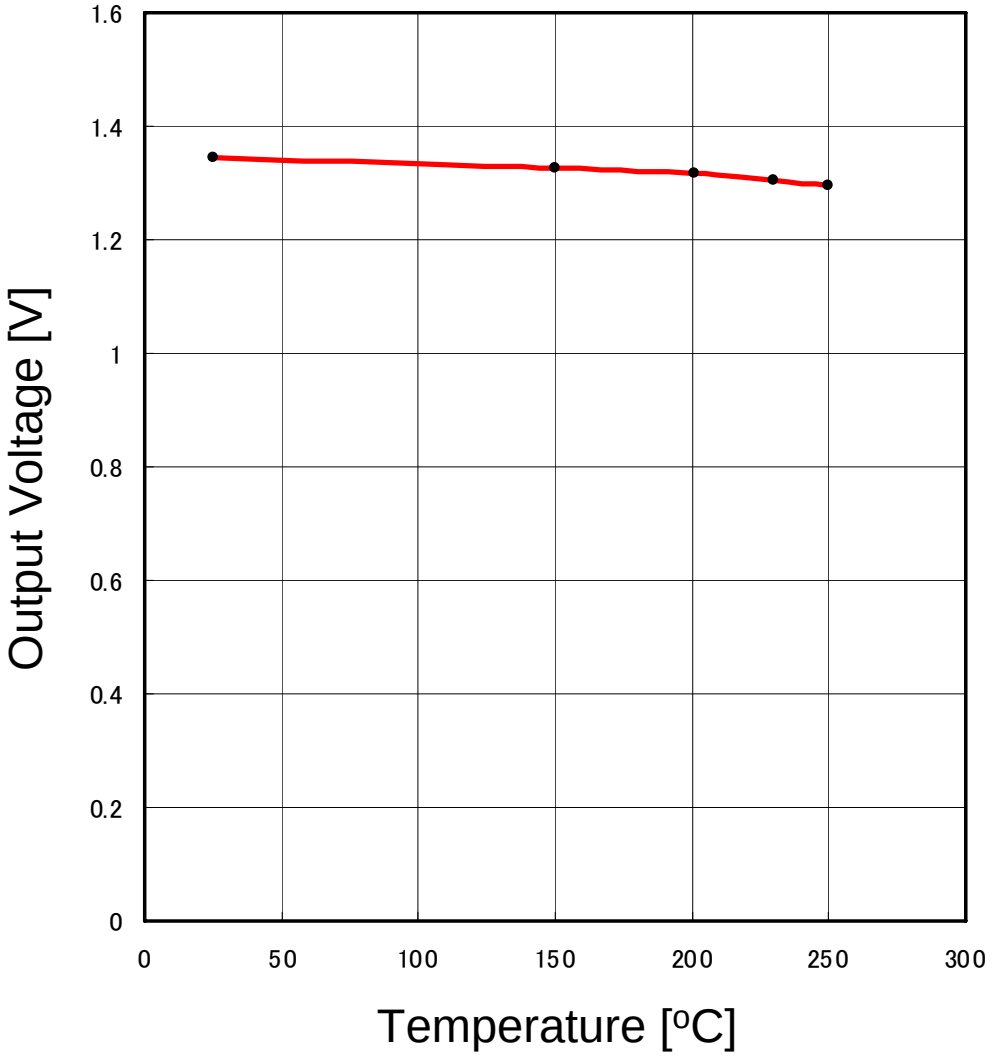


250V 0.5A inverter IC

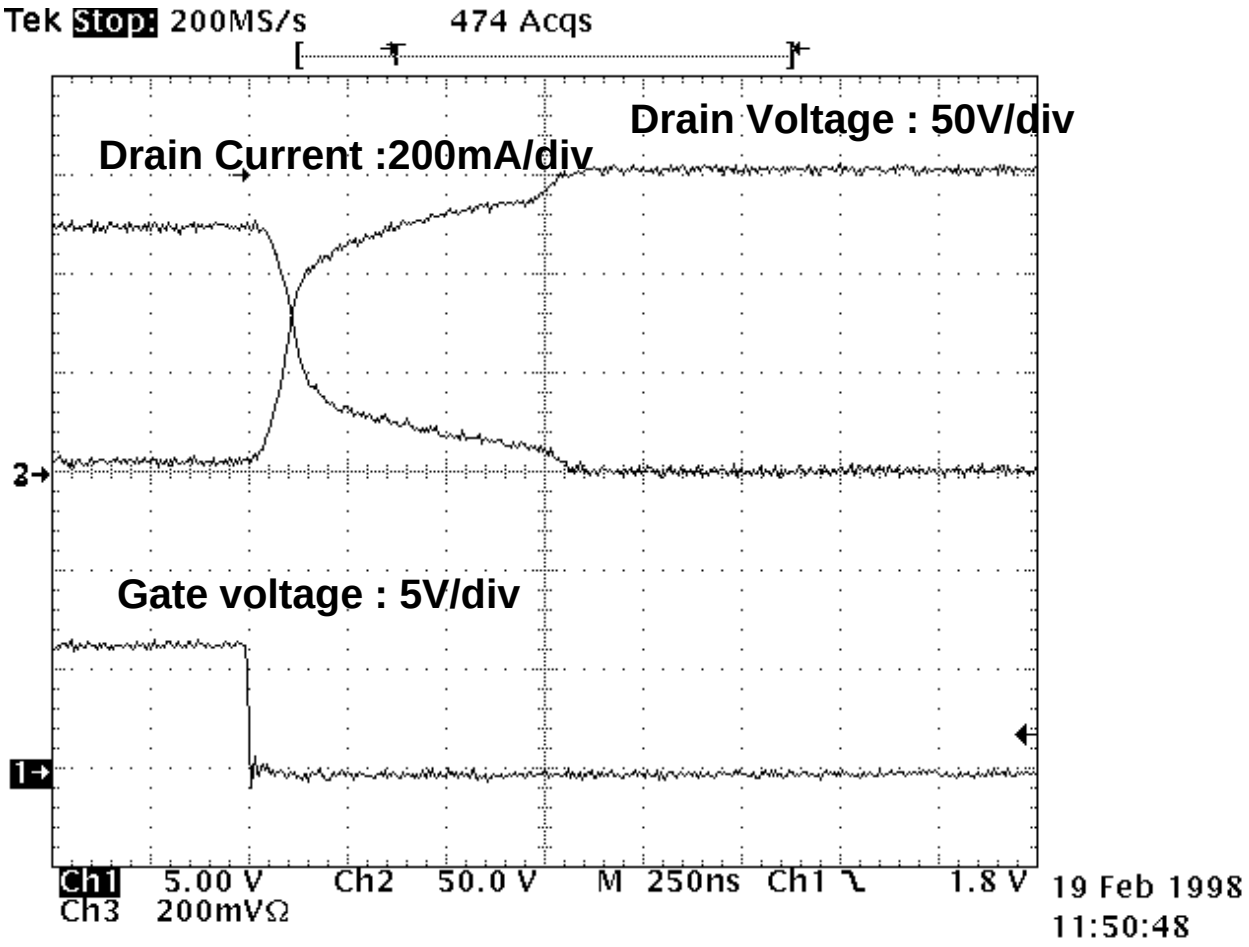
Block diagram of inverter IC



Bandgap reference circuit performance as a function of temperature



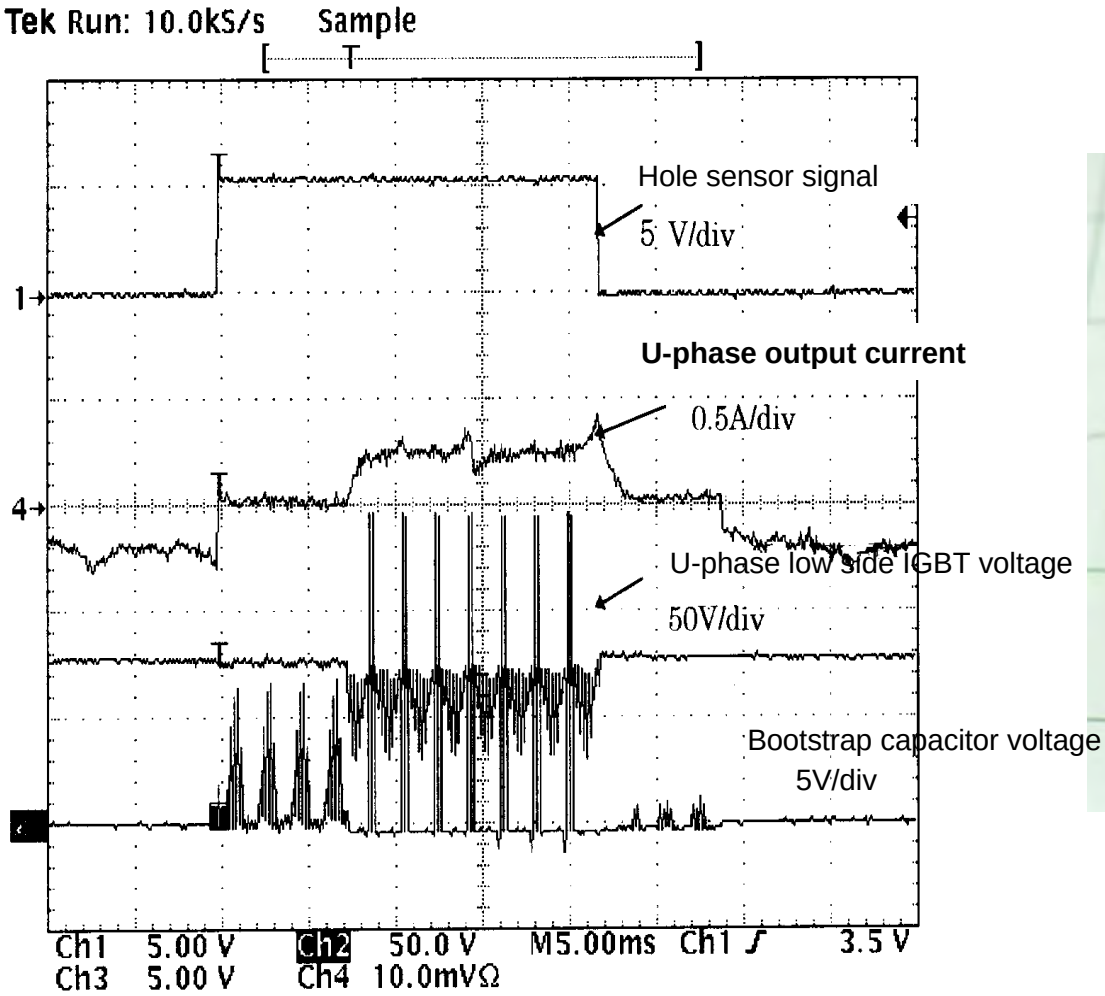
Turn-off waveforms of lateral IGBT at 200°C

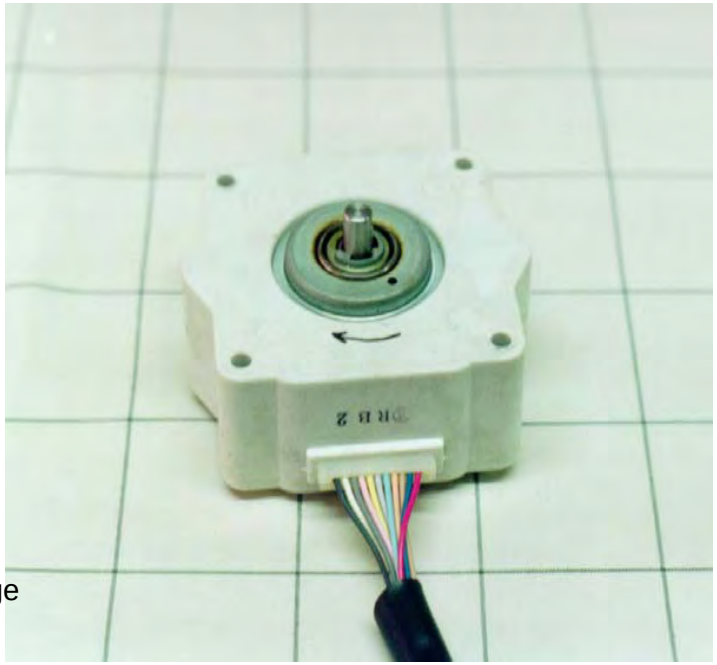


Fall-time=0.5μsec

PWM frequency
≧20kHz

200ºC Operation of
250V 0.5A inverter IC





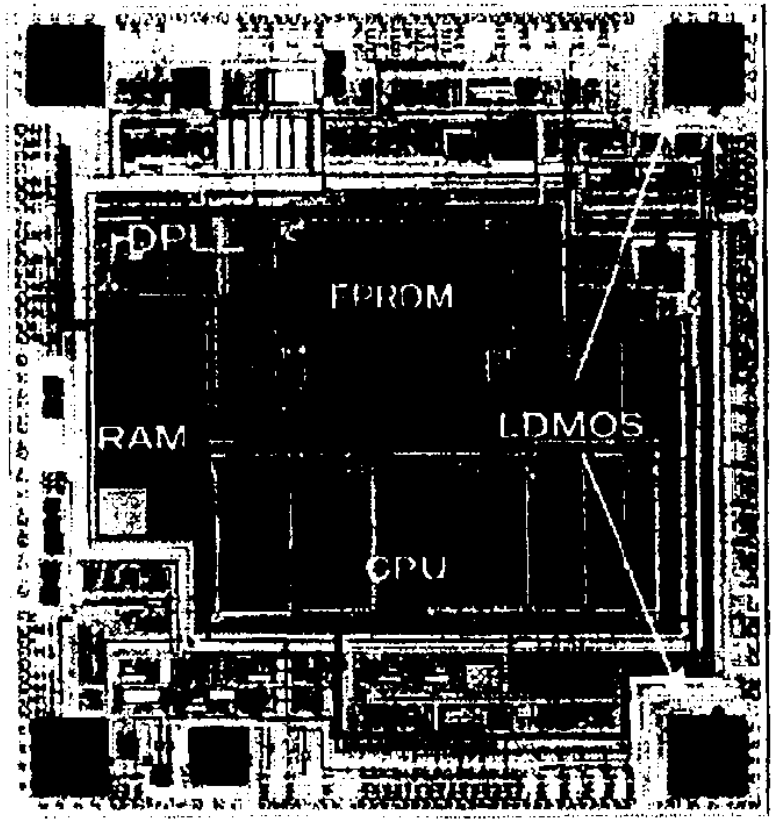
PCIM'98 Japan

BiCD技術における微細化に向けた課題

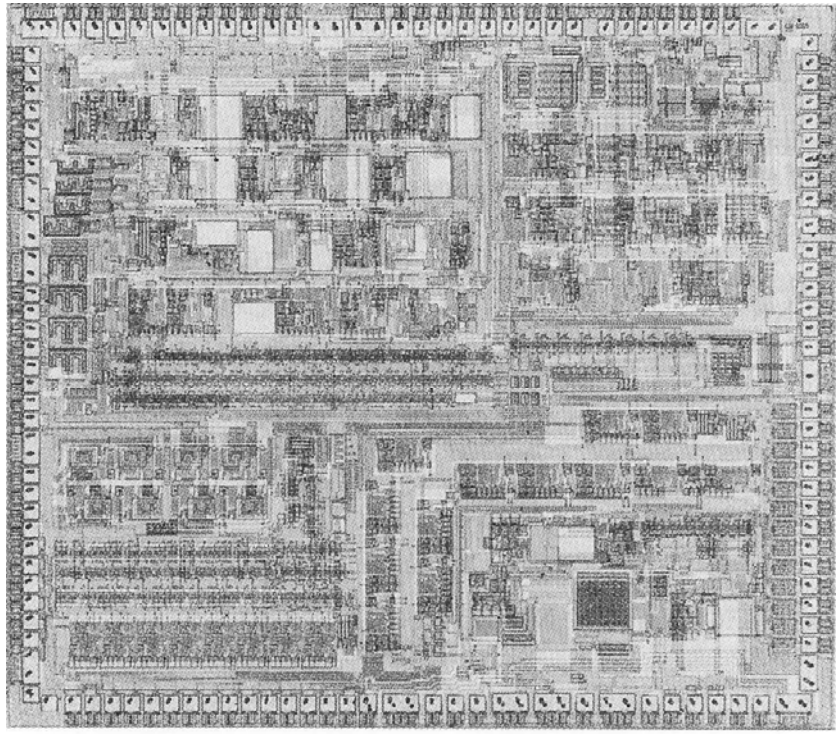
低耐圧ＢＣＤ技術

中川　明夫

セミコンダクター社



Single chip IC to control an air bag



エンジン制御用 ECU 用高集積周辺 IC のチップ写真

BCD name (1984)

- *to classify single chip mixed signal & power silicon technology*

  - “ **B** ” as *Bipolar*
    - for precise ANALOG functions
  - “ **C** ” as *CMOS*
    - for dense DIGITAL design
  - “ **D** ” as *DMOS*
    - for robust HIGH VOLTAGE & POWER devices

なぜＢＣＤ技術か？

→ Power IC の出力段
DMOS vs. Bipolar

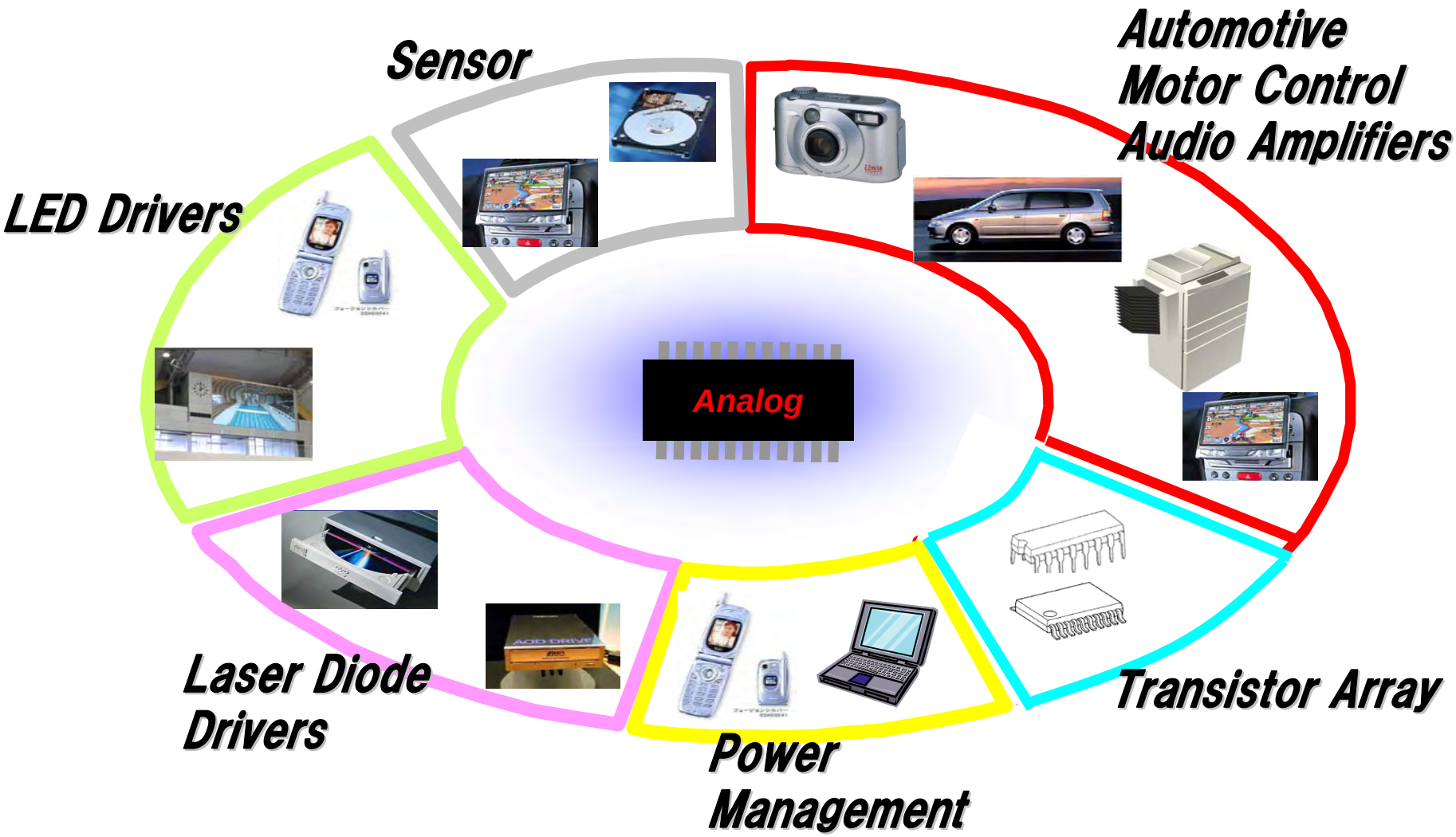
DMOS

- 低いオン抵抗
- 破壊に強い！
- 大電流素子が容易

（ゲート配線：Poly-Si ←電流小さい）

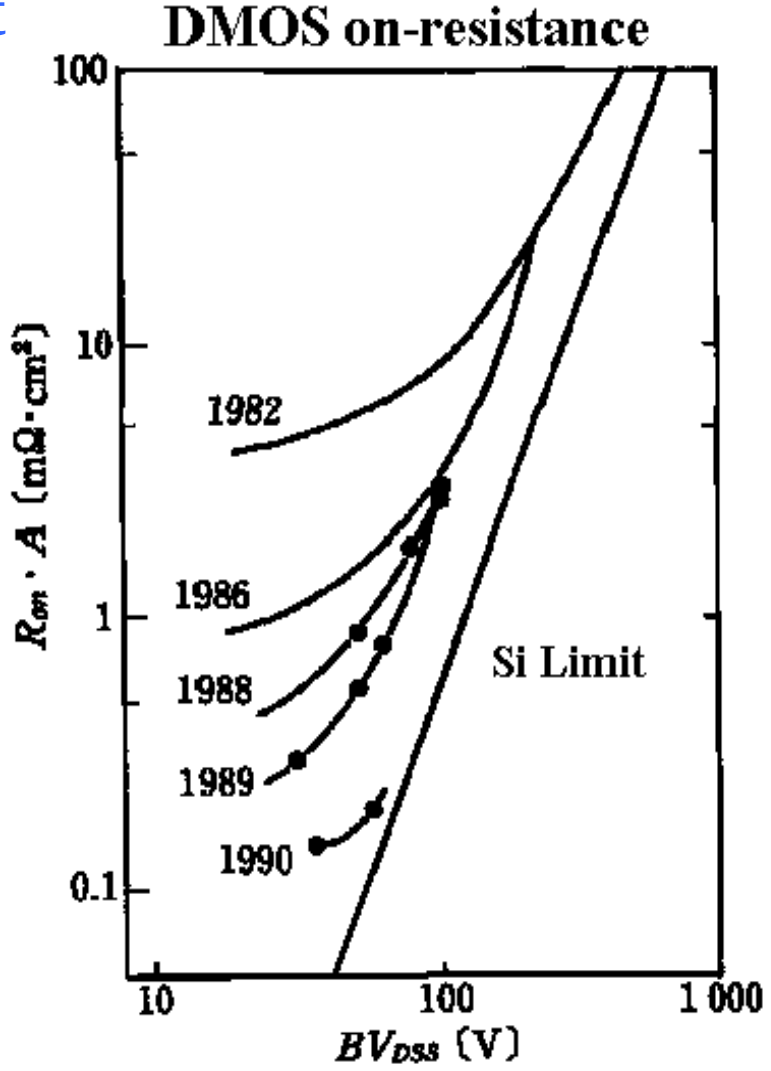
Application Area

Up to 100V Supply voltage



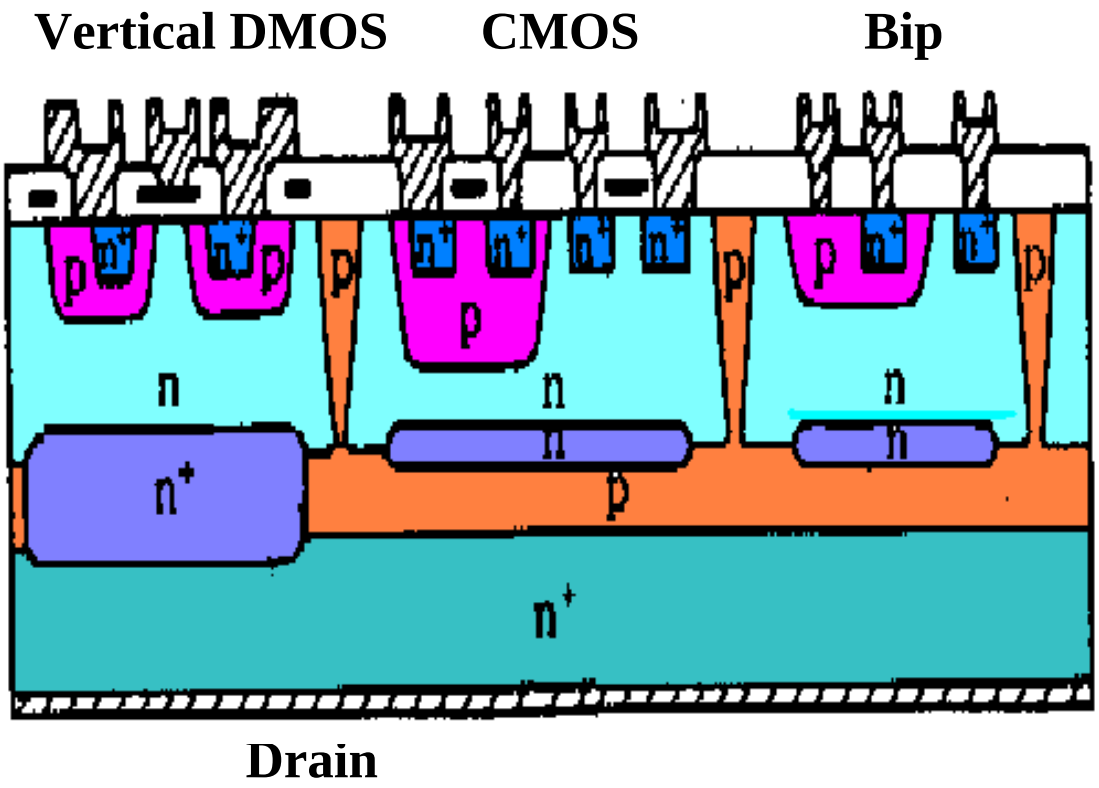
BCDの歴史

- **DMOSFET Ron Improvement**



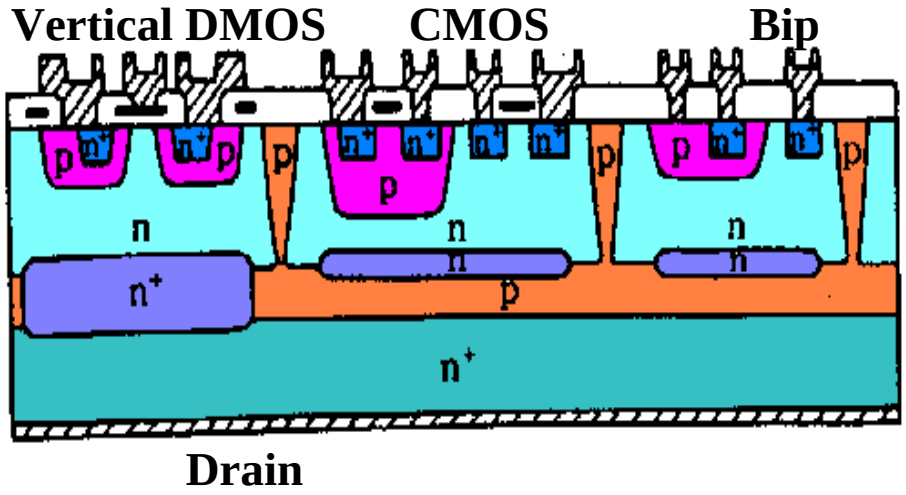
Smart Power　縦型DMOS + 制御回路

•Smart Power Concept in early 1980's



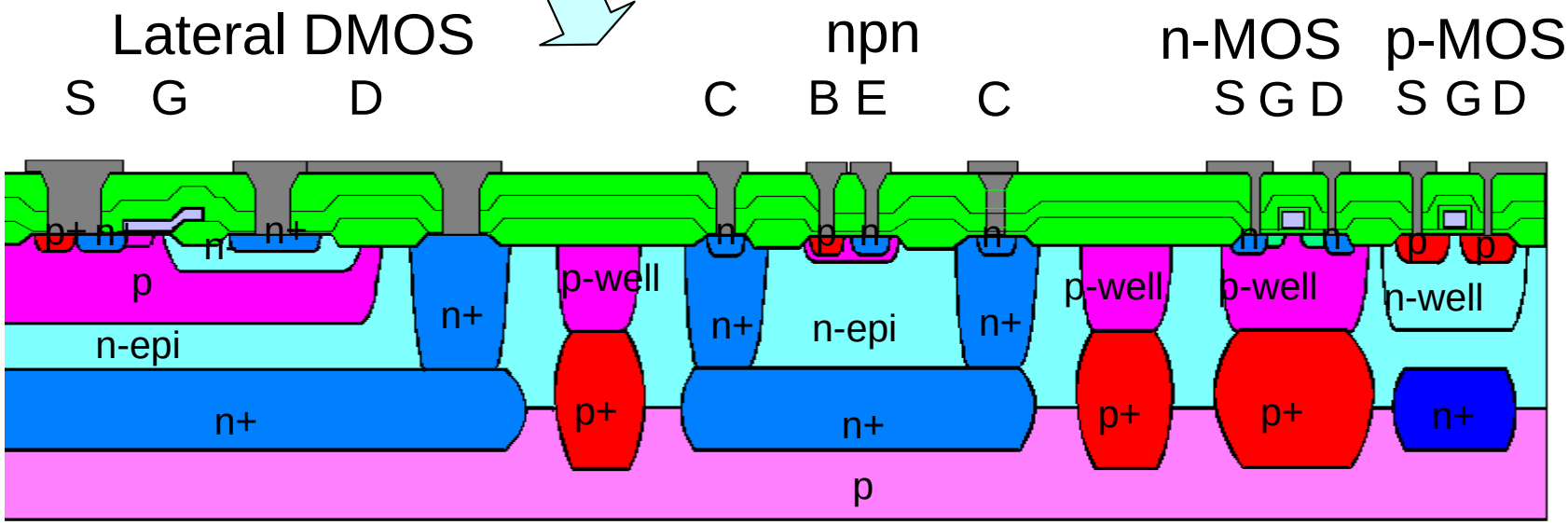
Smart Power : Vertical DMOS

has lost advantage.



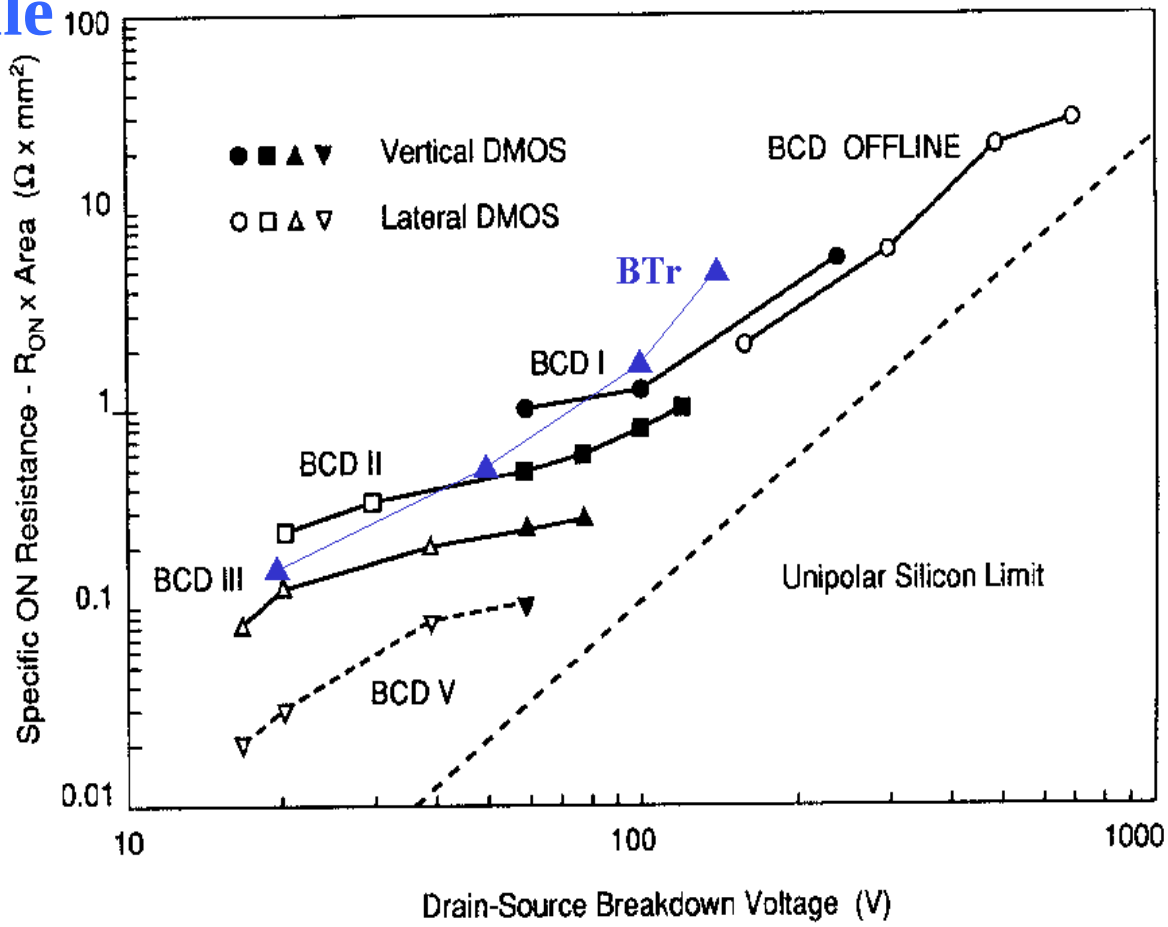
BCD : Lateral DMOS :

reasonable cost
large current
multi-output

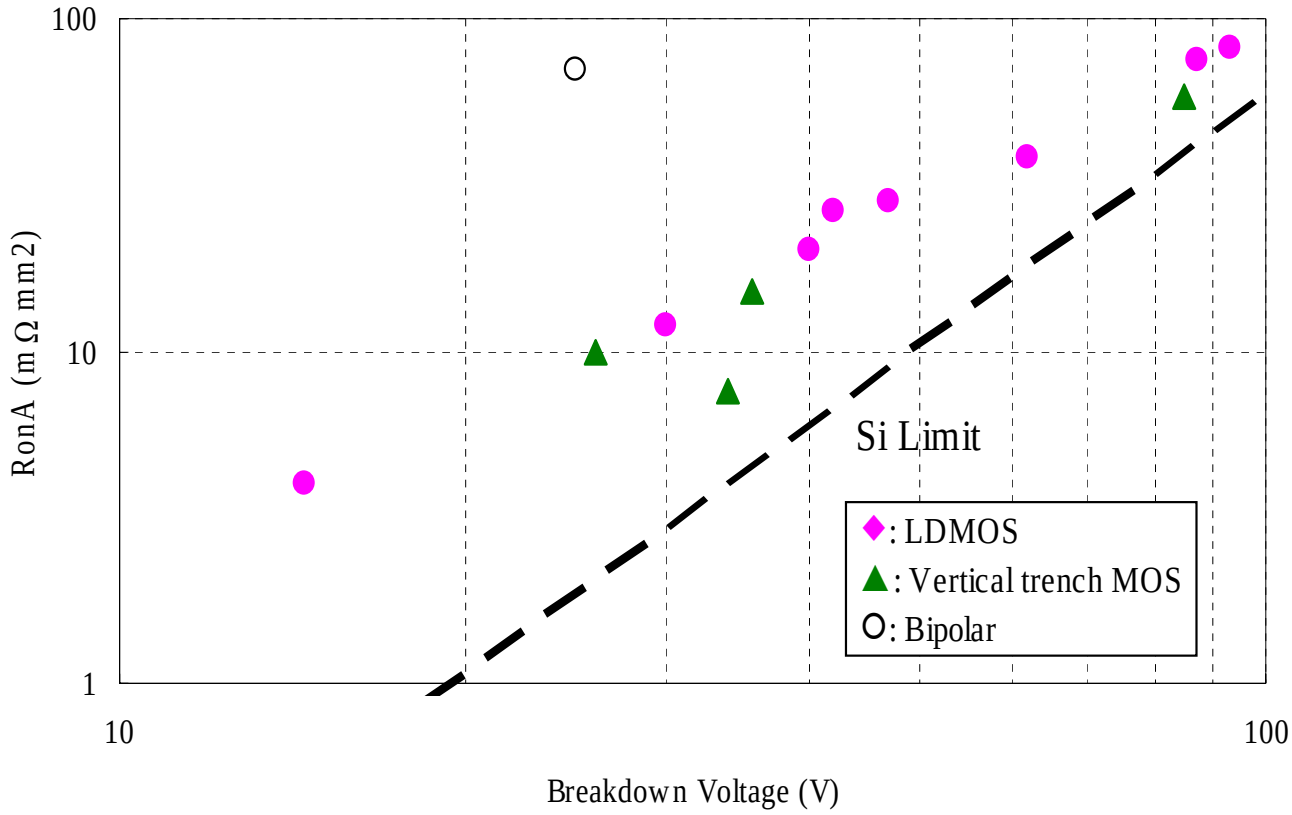


BCD技術　横型DMOS + 制御回路

- Smart Power Concept
- **BCD Technology**
  - **0.6μm design rule**

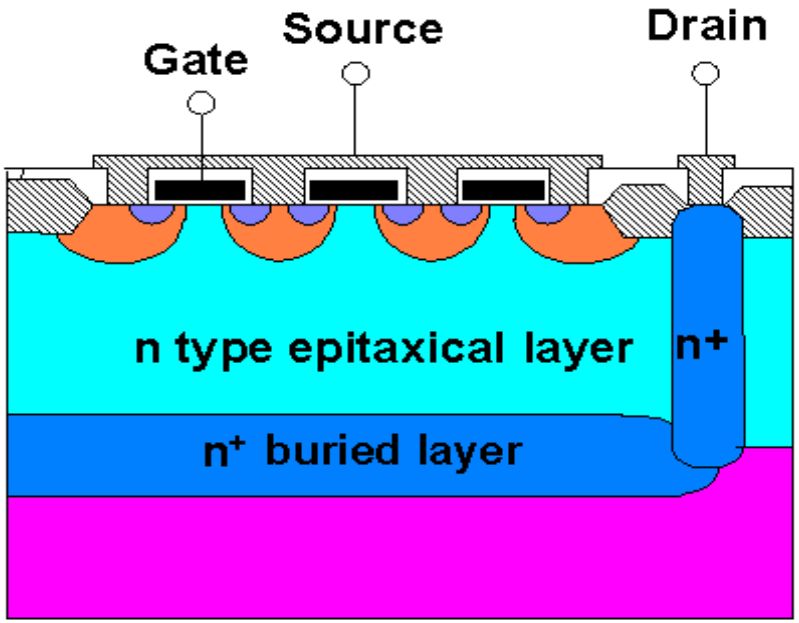


Lateral DMOS vs. Vertical Trench MOSFET

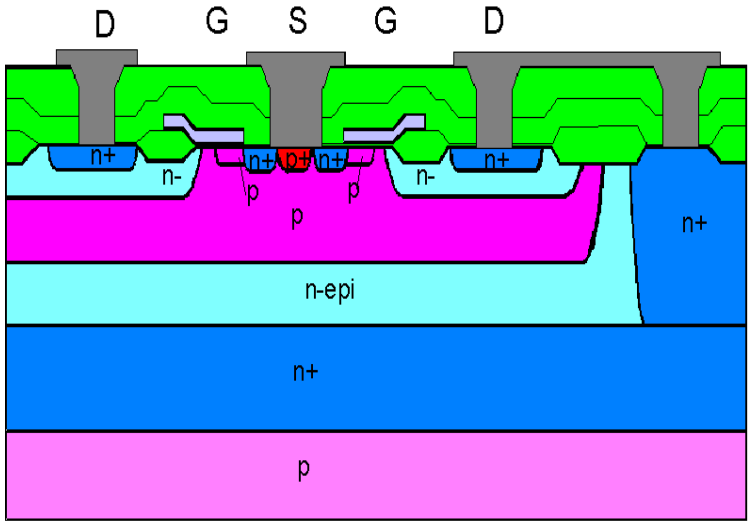


Lateral DMOS vs. Vertical DMOS

LDMOS:　Rds(on) is simply reduced depending on design rule



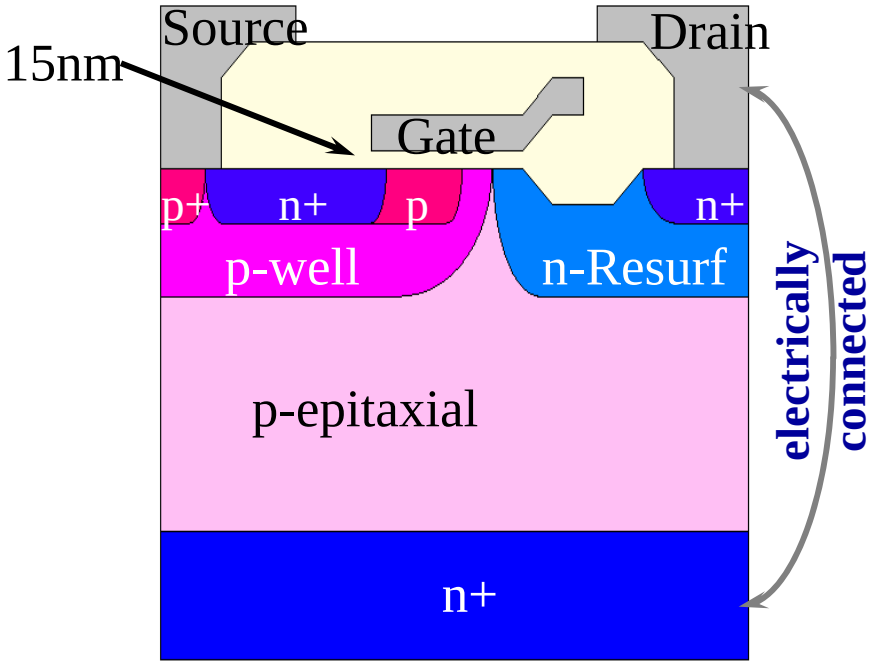
Up Drain vertical DMOS

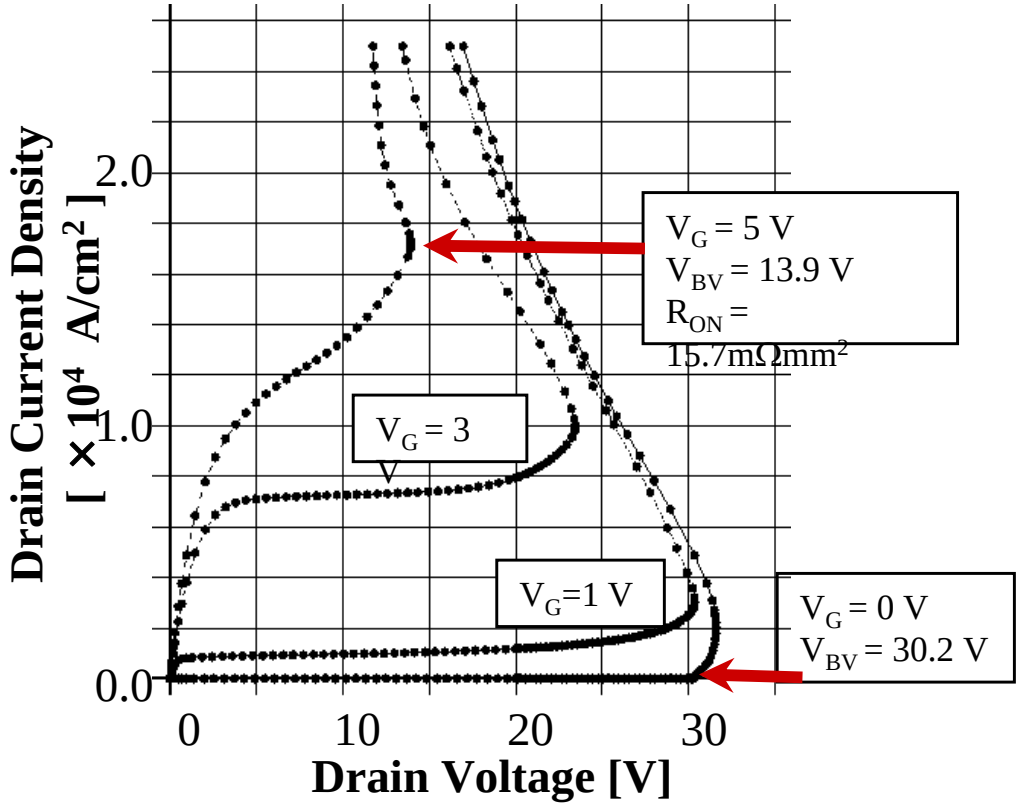


LDMOS

従来のLDMOS　問題点

----Low on-state breakdown voltage

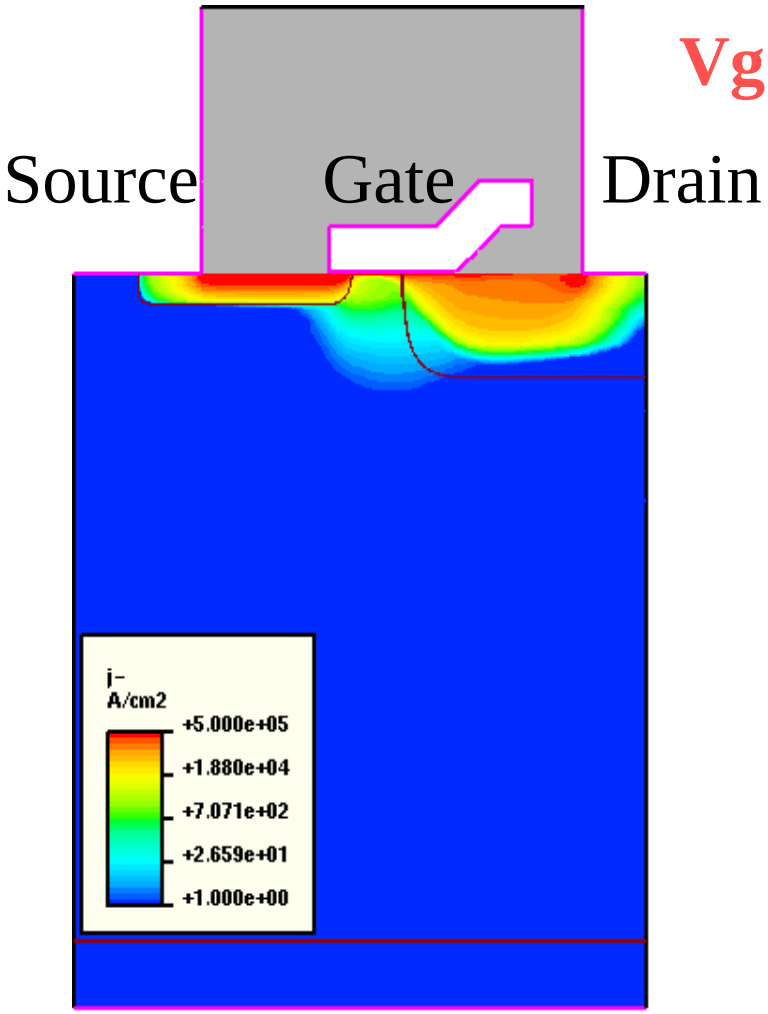


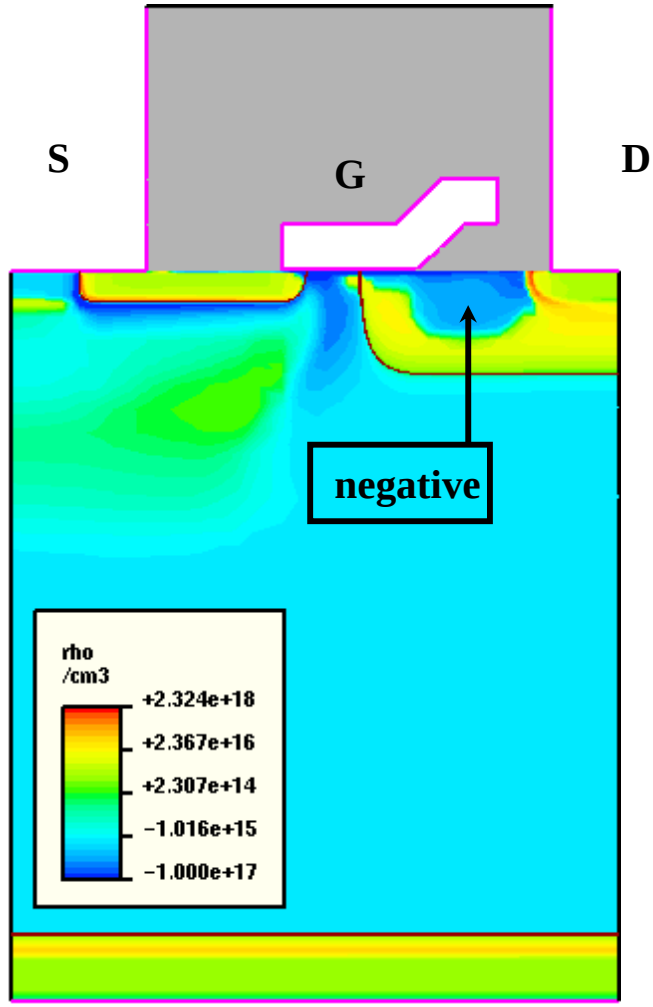


Net charge distribution

Electron current density

Vg=5V





Net positive Resurf charge ρ_{net} under a drain current of I_D

$$\rho_{\text{net}} = \rho_{\text{Resurf dose}} - I_D / qv_s$$

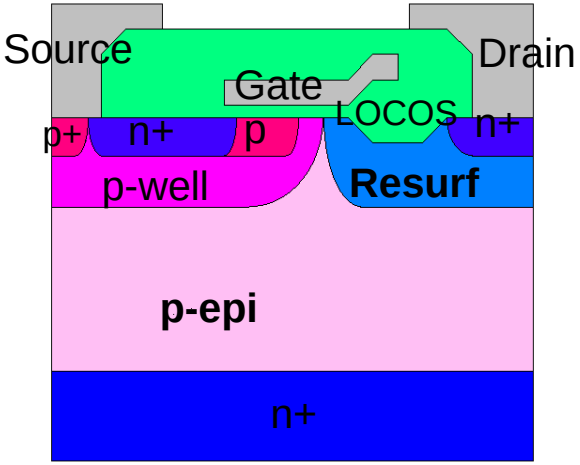
$\rho_{\text{Resurf dose}}$: original Resurf dose

q : elementary electric charge

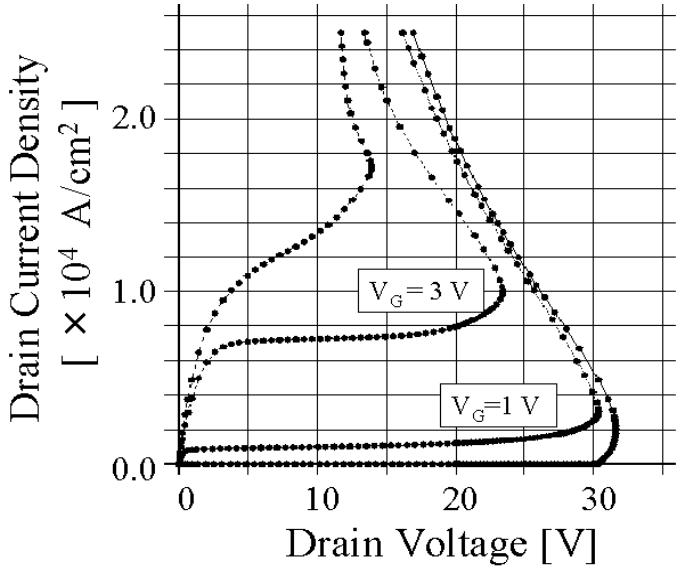
v_s : electron saturation velocity

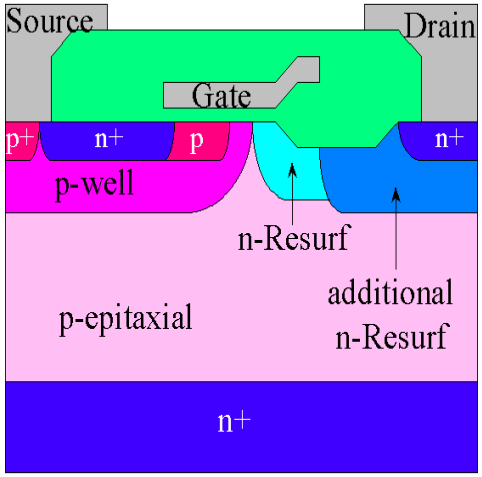
Adaptive Resurf

----- Improvement of on-state breakdown voltage

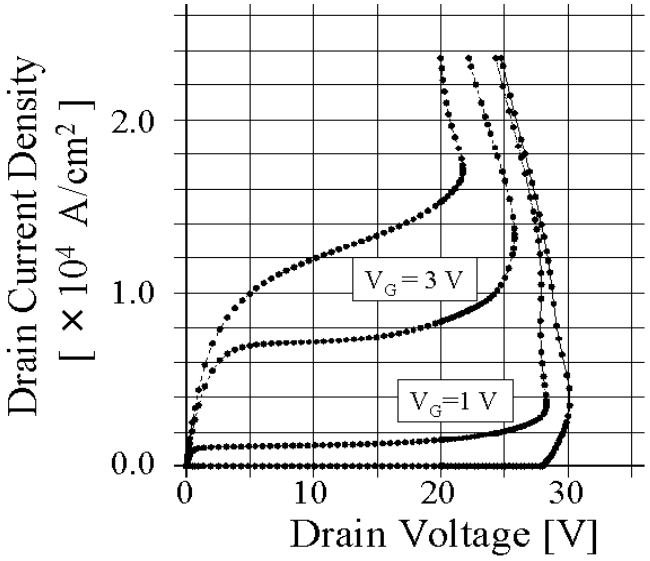


Conventional



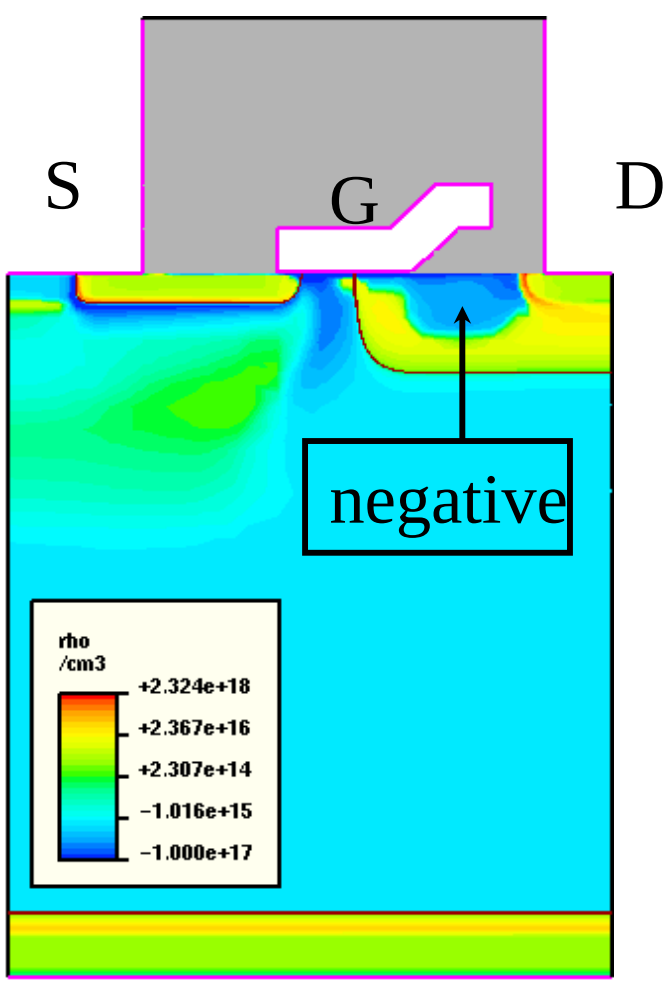


Improved LDMOS with Adaptive Resurf

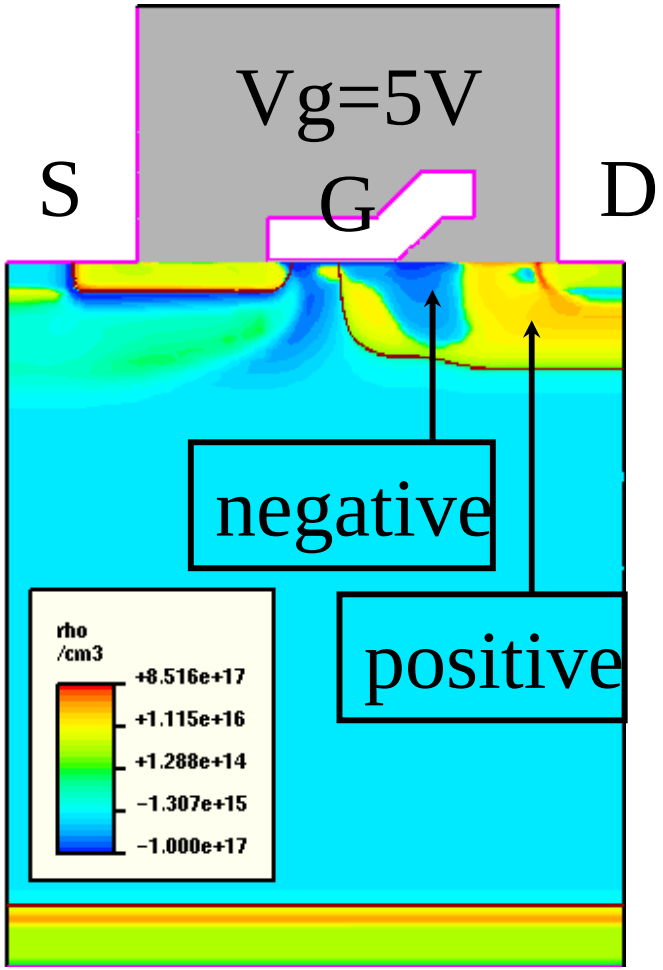


Adaptive Resurf concept

Net space charge distribution

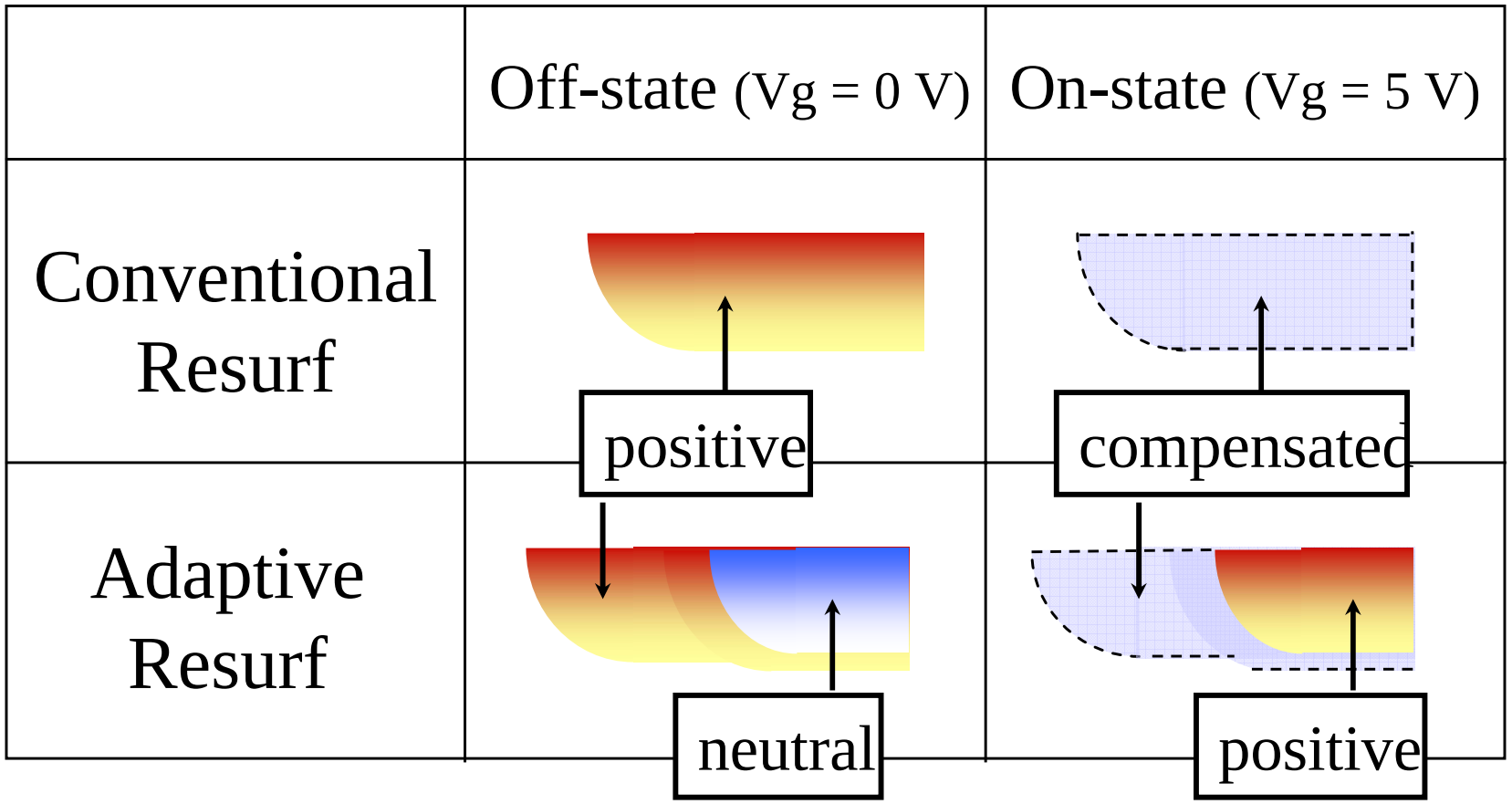


Conventional

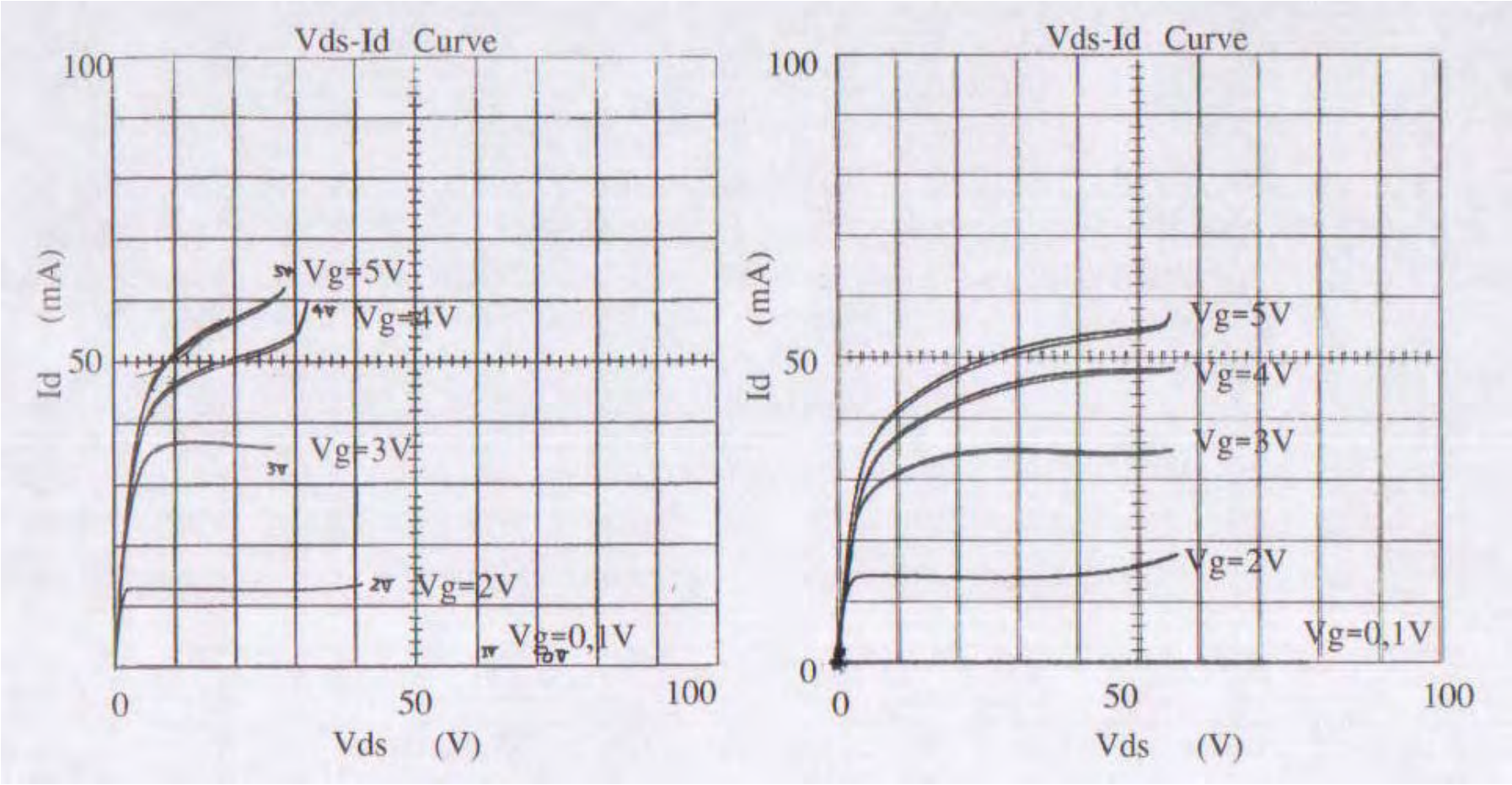


Adaptive Resurf

Adaptive Resurf concept



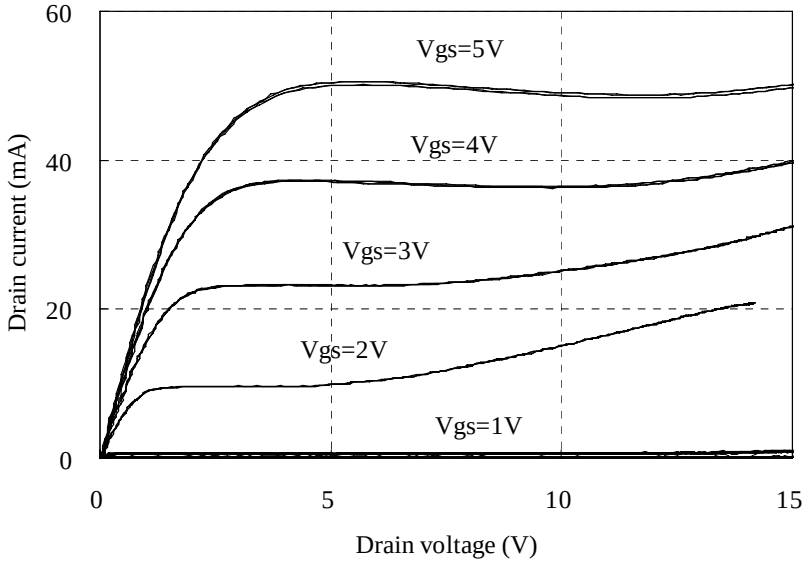
Effects of Adaptive Resurf



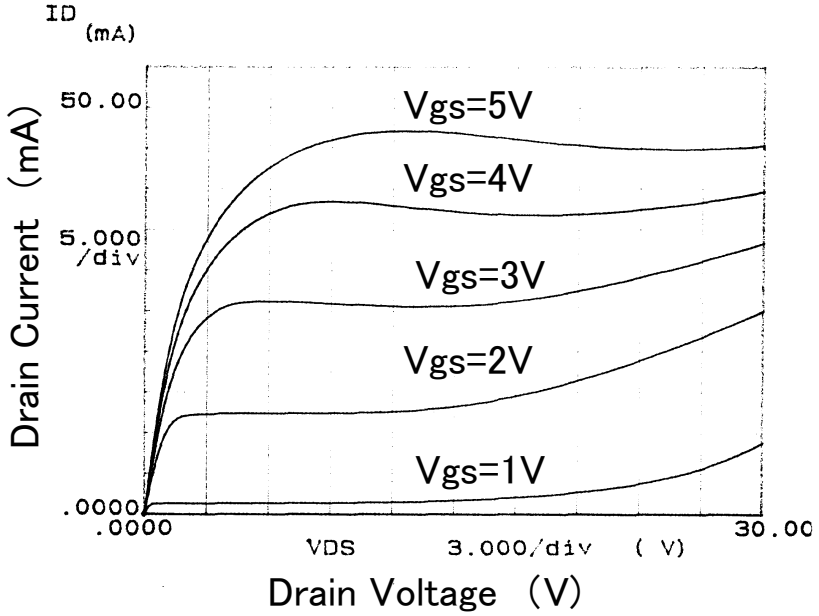
Conventional LDMOS **Improved LDMOS**

Experimental Results

I-V characteristics of n-channel LDMOS

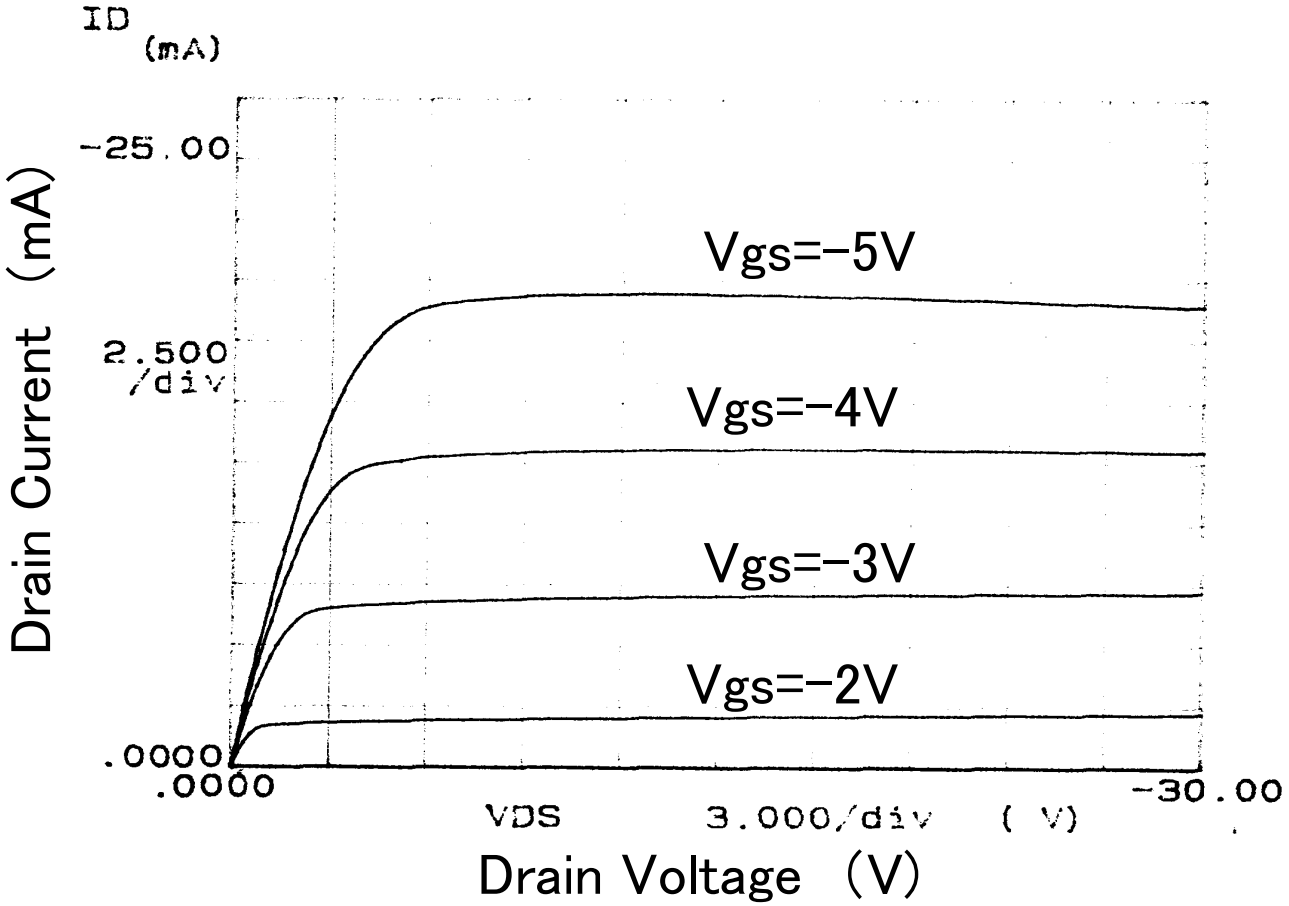


15V LDMOS



25V LDMOS

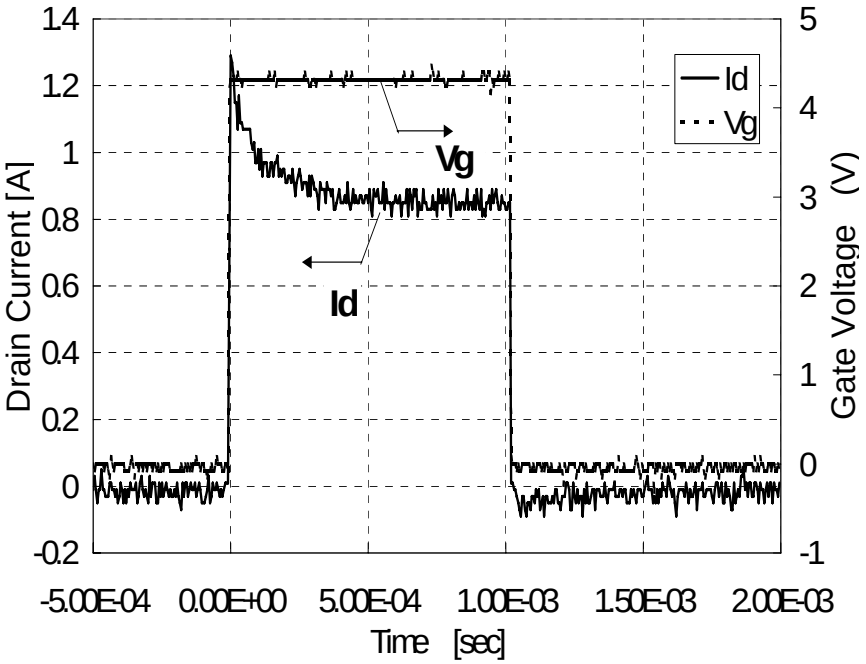
I-V characteristics of 25V p-channel LDMOS

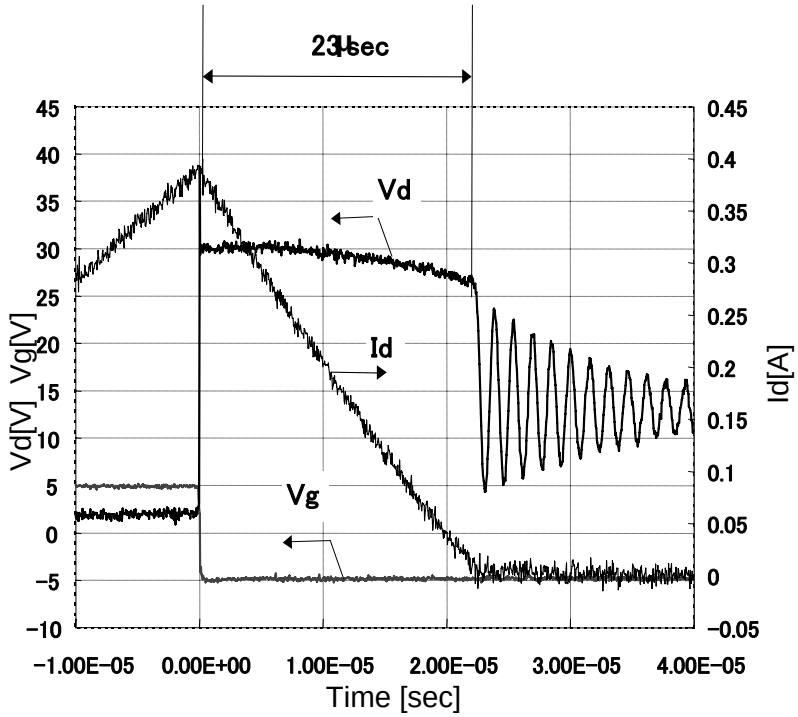


Electrical Characteristics for Developed LDMOS

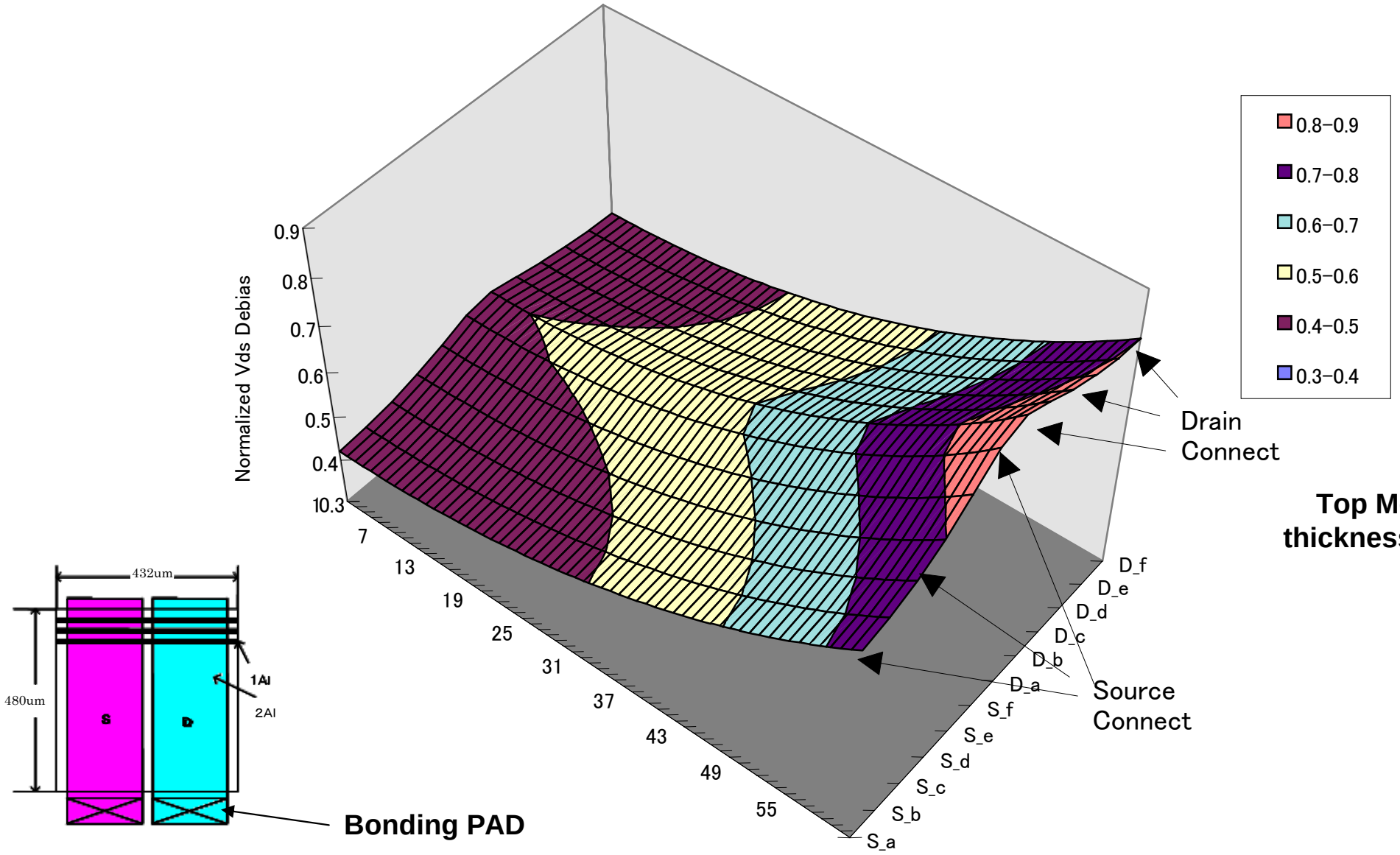
	60V LDMOS	25V LDMOS
Breakdown voltage	70V	30V
On-state Breakdown Voltage	45V	30V
Rds(on)	180mΩmm^2	28mΩmm^2
ESD level EIAJ	300V	300V
MIL	2500V	6000V

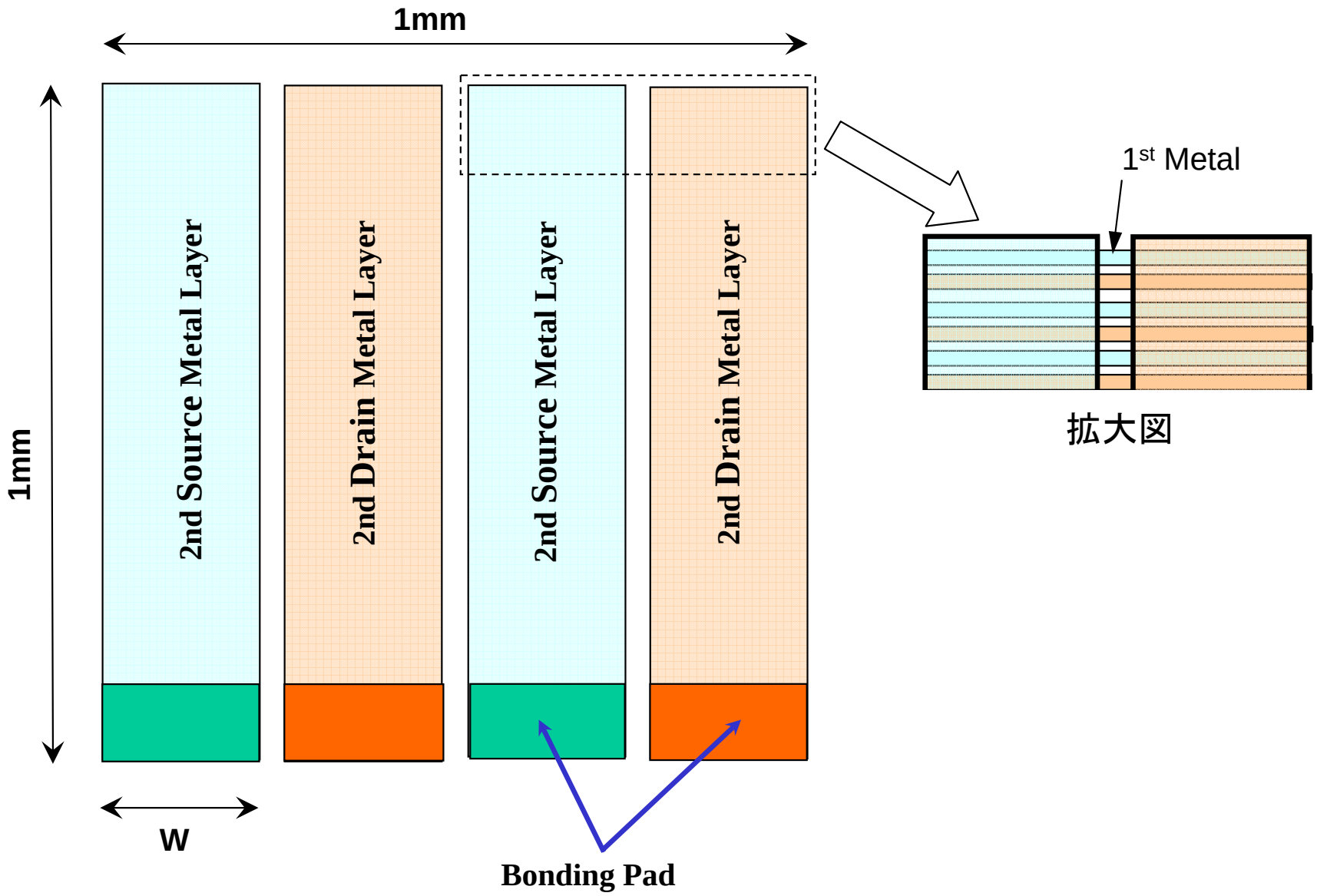
負荷短絡 & UIS

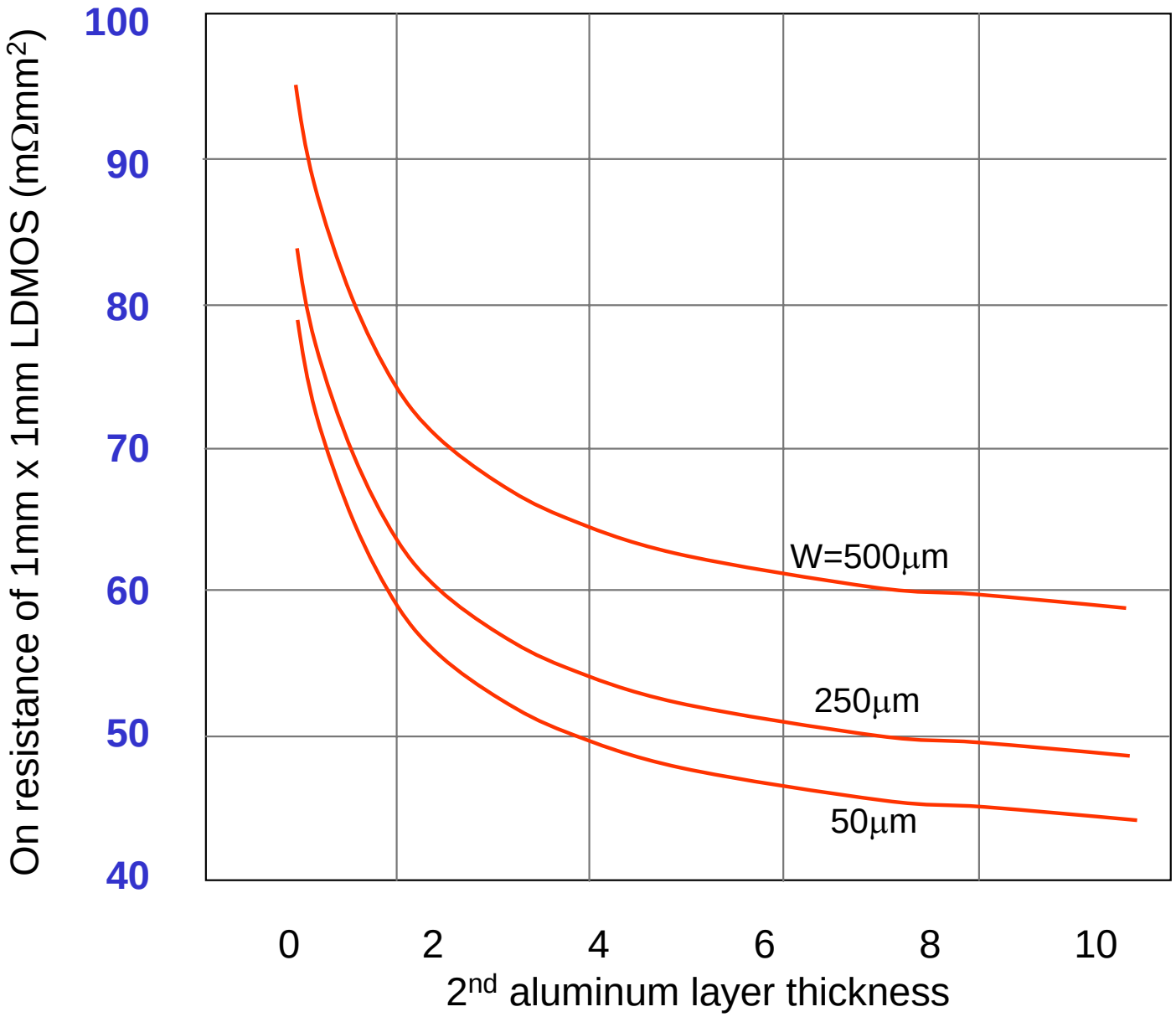

Drain Current [A]
Gate Voltage (V)
Time [sec]
Id
Vg
Id
Vg
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
5
4
3
2
1
0
-1
-5.00E-04
0.00E+00
5.00E-04
1.00E-03
1.50E-03
2.00E-03


23Usec
Vd
Id
Vg
Vd[V] Vg[V]
Id[A]
Time [sec]
45
40
35
30
25
20
15
10
5
0
−5
−10
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
−0.05
−1.00E−05
0.00E+00
1.00E−05
2.00E−05
3.00E−05
4.00E−05

大電流化：電極配線抵抗


Normalized Vds Debias
0.9
0.8
0.7
0.6
0.5
0.4
10.3
7
13
19
25
31
37
43
49
55
S_a
S_b
S_c
S_d
S_e
S_f
D_a
D_b
D_c
D_d
D_e
D_f
0.8–0.9
0.7–0.8
0.6–0.7
0.5–0.6
0.4–0.5
0.3–0.4
Drain
Connect
Source
Connect
Top Metal
thickness:1um
432um
480um
S
D
1Al
2Al
Bonding PAD


1mm
1mm
2nd Source Metal Layer
2nd Drain Metal Layer
2nd Source Metal Layer
2nd Drain Metal Layer
W
Bonding Pad
1st Metal
拡大図



シリコン素子抵抗=40 mΩmm²

Cu electroplating – TI

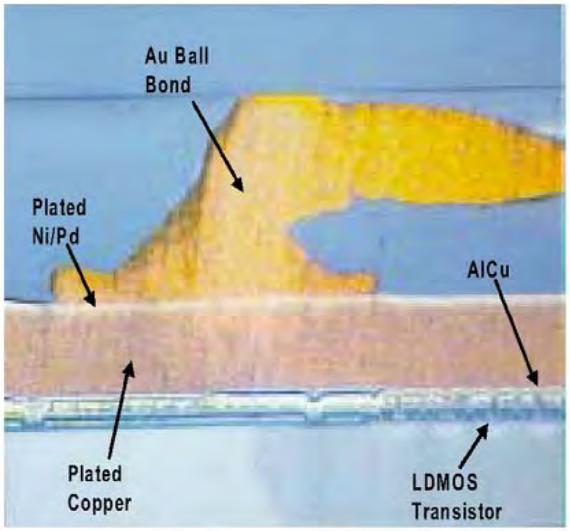
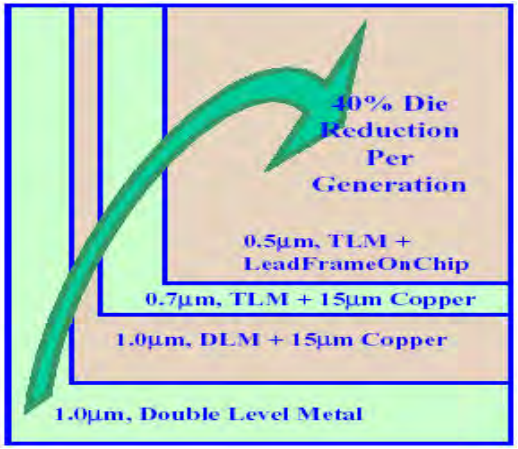


Fig. 1: LBC6 BOAC (bond over active circuit) capability
(Au ball bond on plated Cu/Ni/Pd
over active Ldmos transistor)



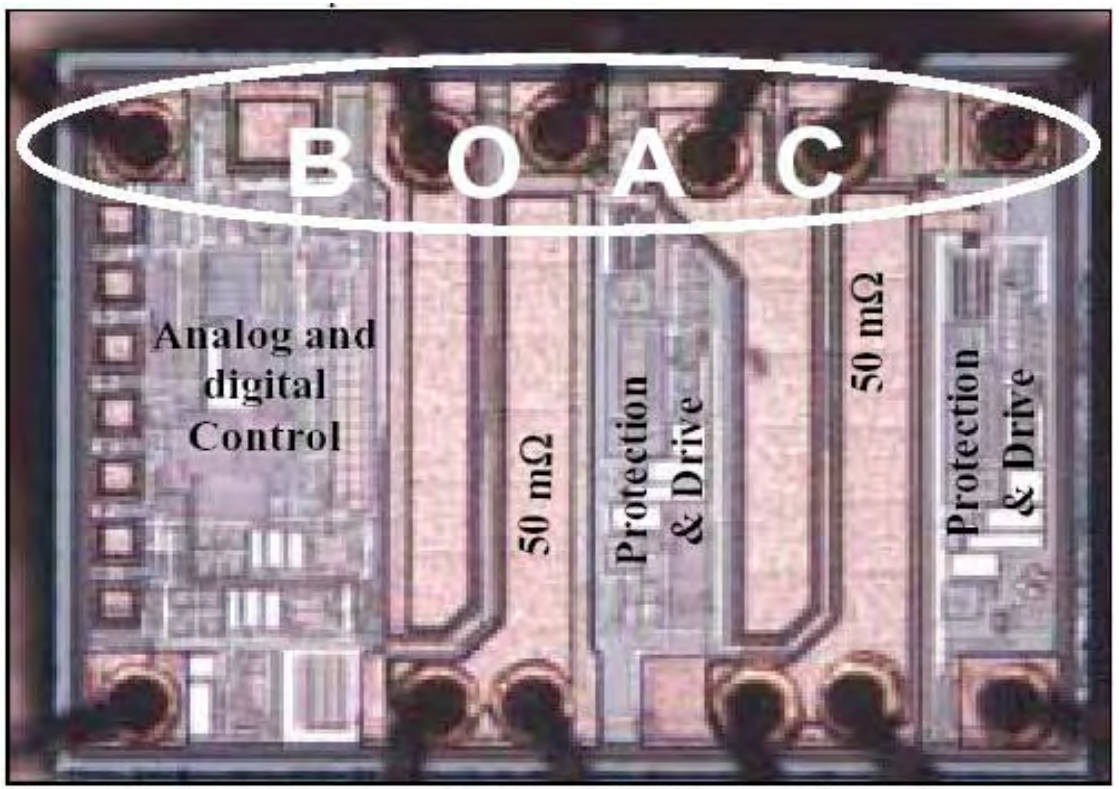


Figure 1. A dual output 50mΩ PCMCIA switch is shown using LeadfFameOnChip. Bonds are directly Over Active Circuitry (BOAC) attached with centralized power busses.

Design of a 4 MHz, 5V to 1V Monolithic Voltage Regulator Chip

(Student Paper)

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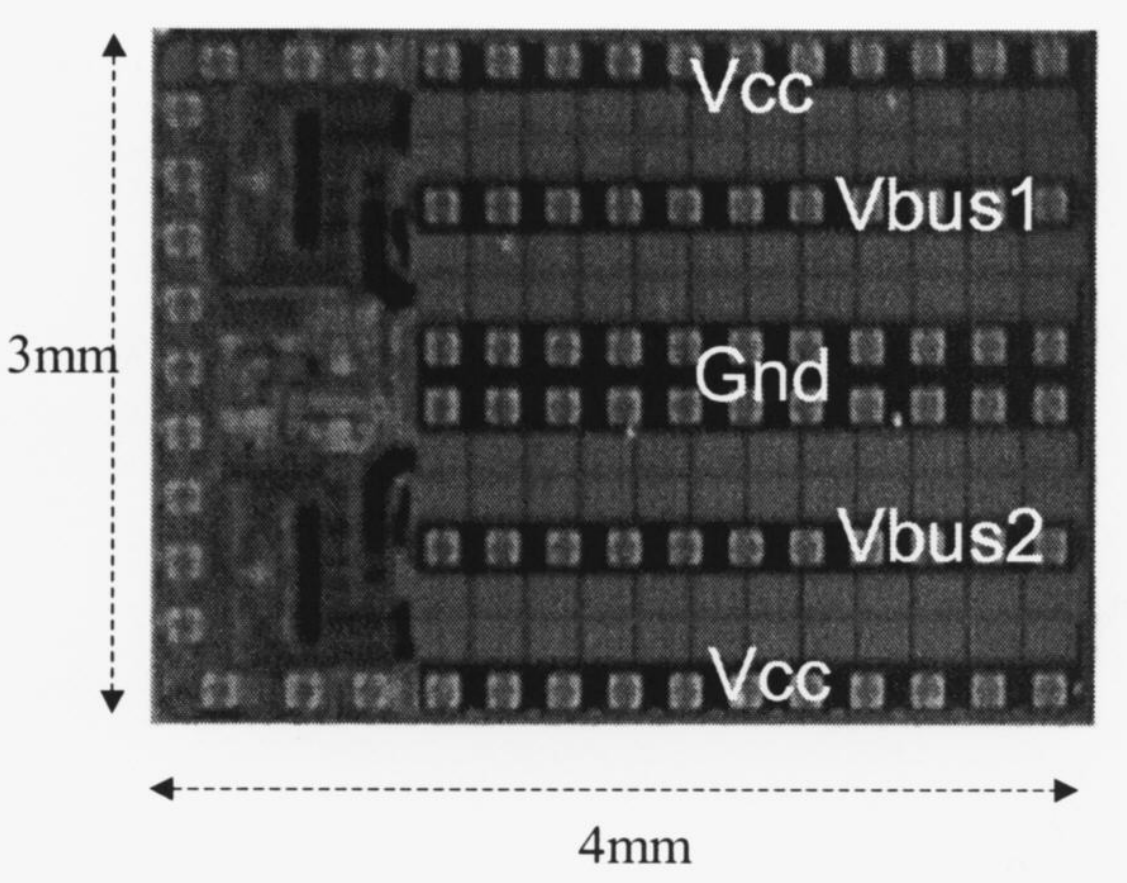
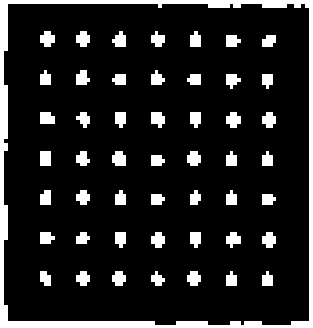
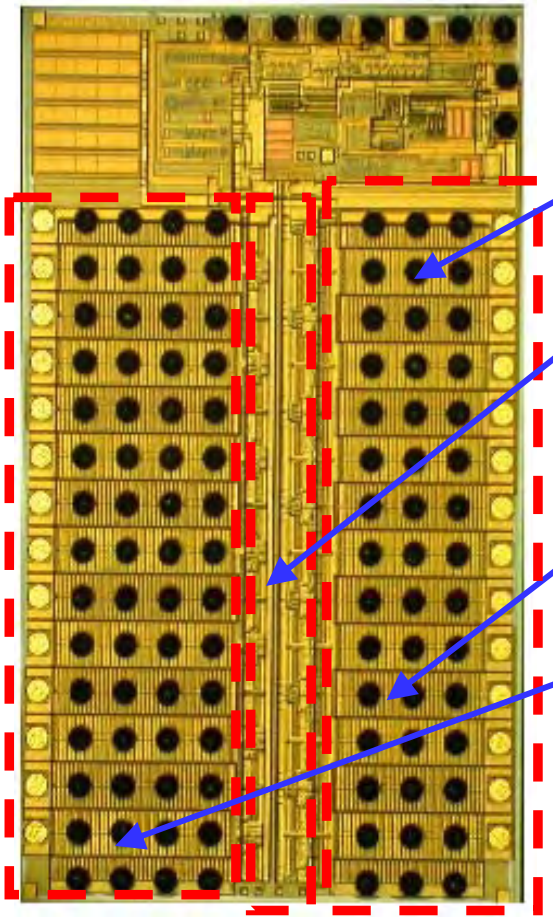
Center for Power Electronics Systems, Department of Electrical and Computer Engineering
Virginia Polytechnic Institute and State University, Blacksburg, VA 24060-0179, USA
Phone: +1(540) 231-5494, Fax: +1(540) 231-6390, Email: xsun@vt.edu





BGA and Bump's reduces parasitic R & L

12V 10A chip



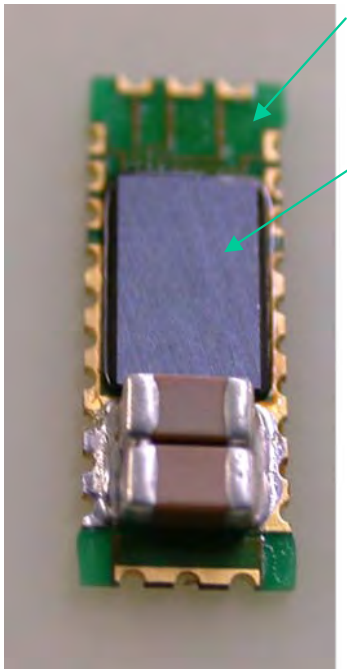
Bump ball

Driver Circuits

Pch LDMOS

Nch LDMOS

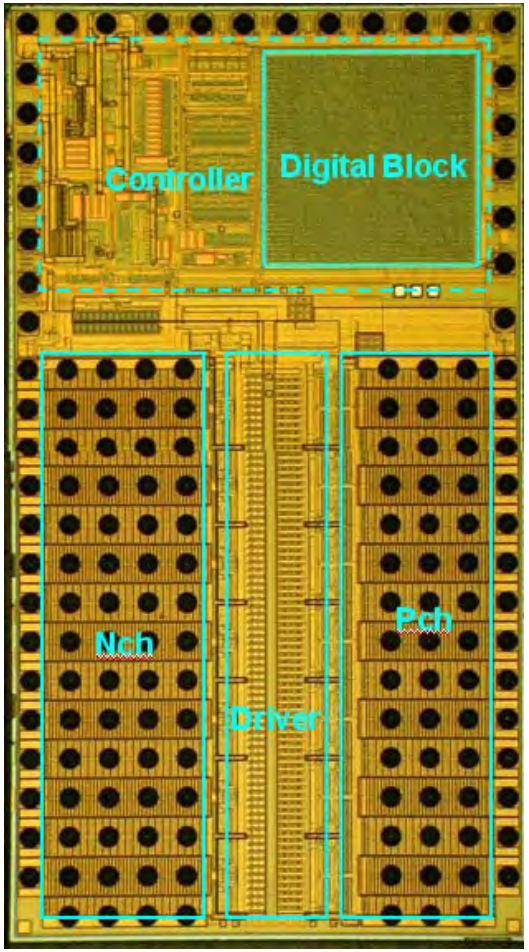
The chip size：20.3mm^2



Evaluation PCB

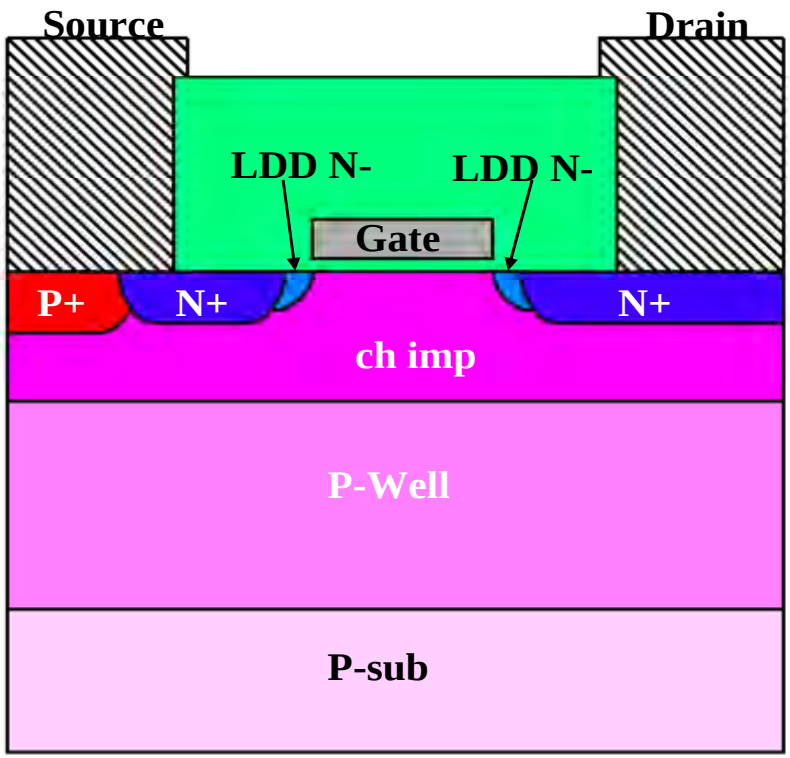
Chip

5V 20A 1chip DCDC Converter

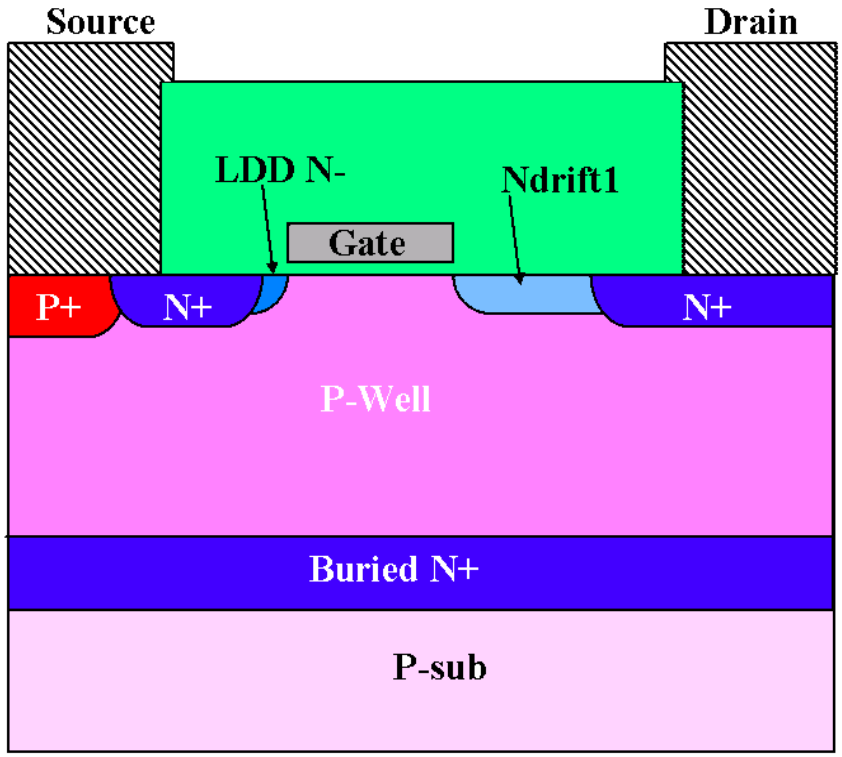


1チップ電源に最適なパワー段が必要

5V系と20V系のパワー段を開発



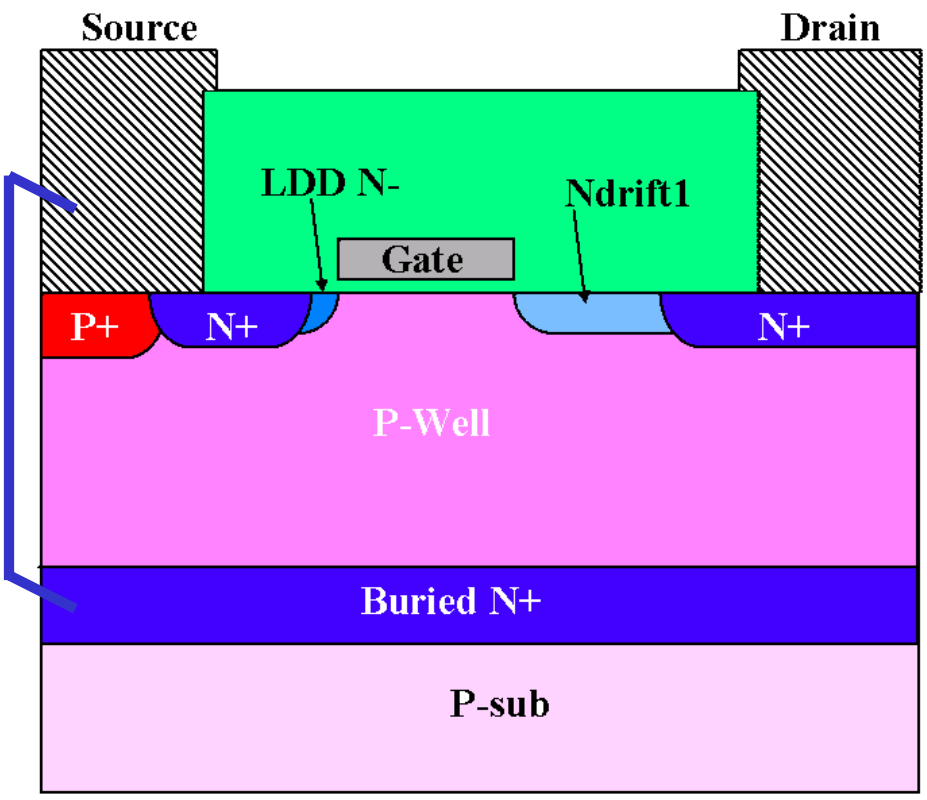
5V Power CMOS



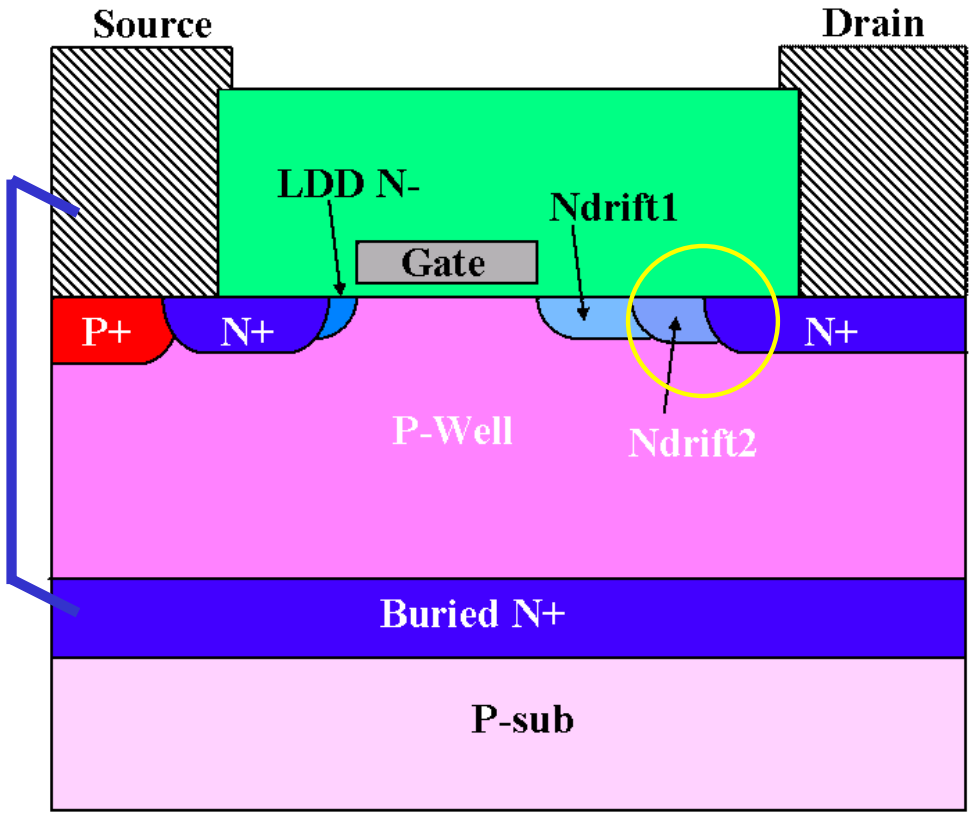
20V Lateral DMOS

20V MOSFET 構造

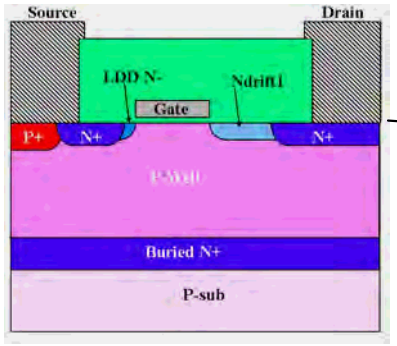
1-step n-implant LDMOS

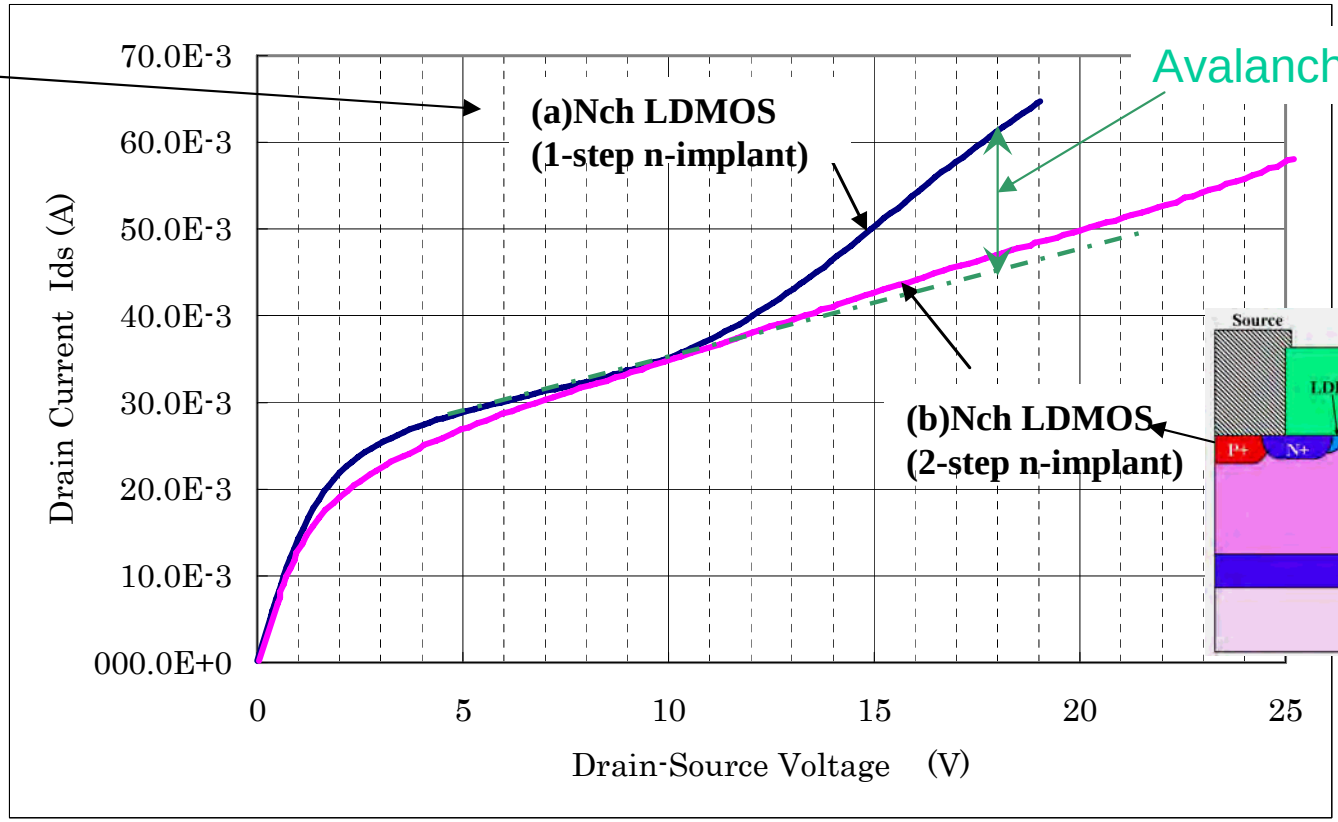


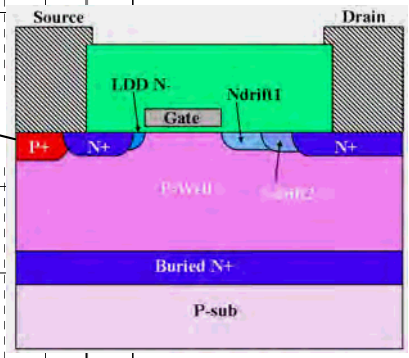
2-step n-implant LDMOS
（Adaptive Resurf）



N-ch LDMOS 特性



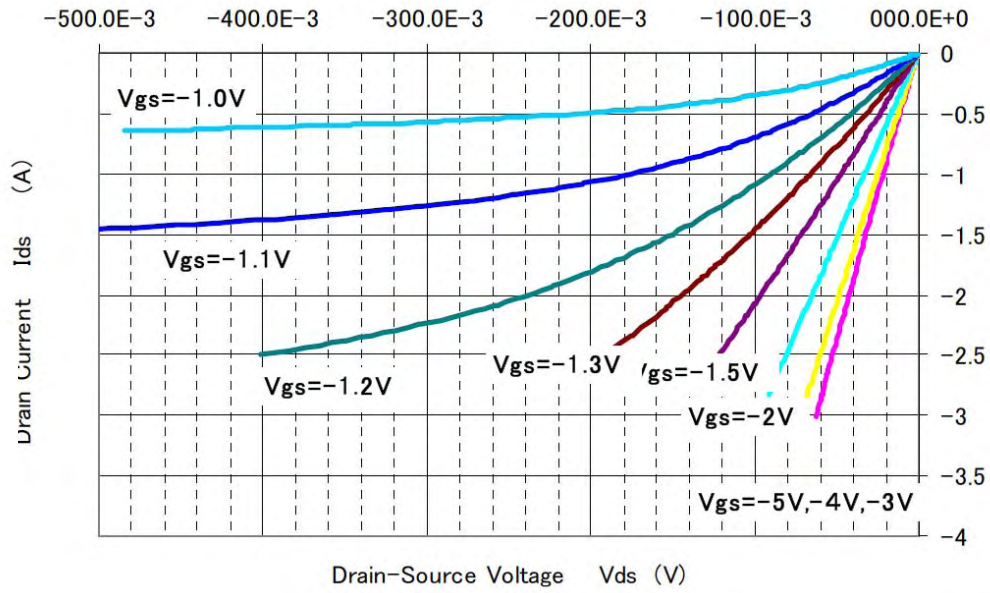




(@Vgs=5V, Channel width=157um)

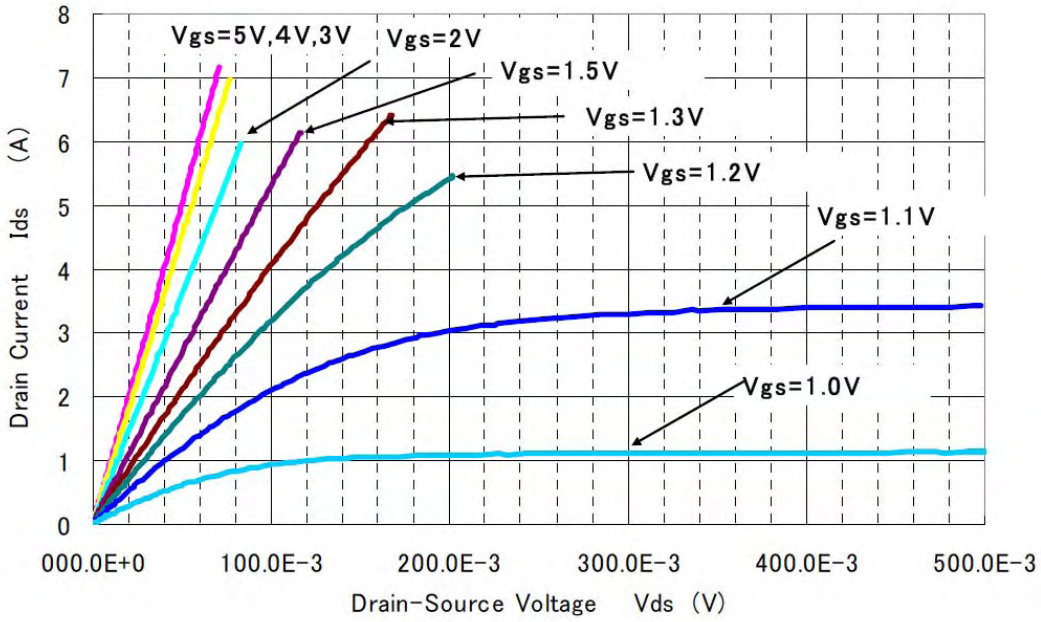
大電流素子の特性

Ron :19.3m Ω(@Vgs=5V, Ids=5A)



(effective area =3mm2)

(effective area =3.6mm2)

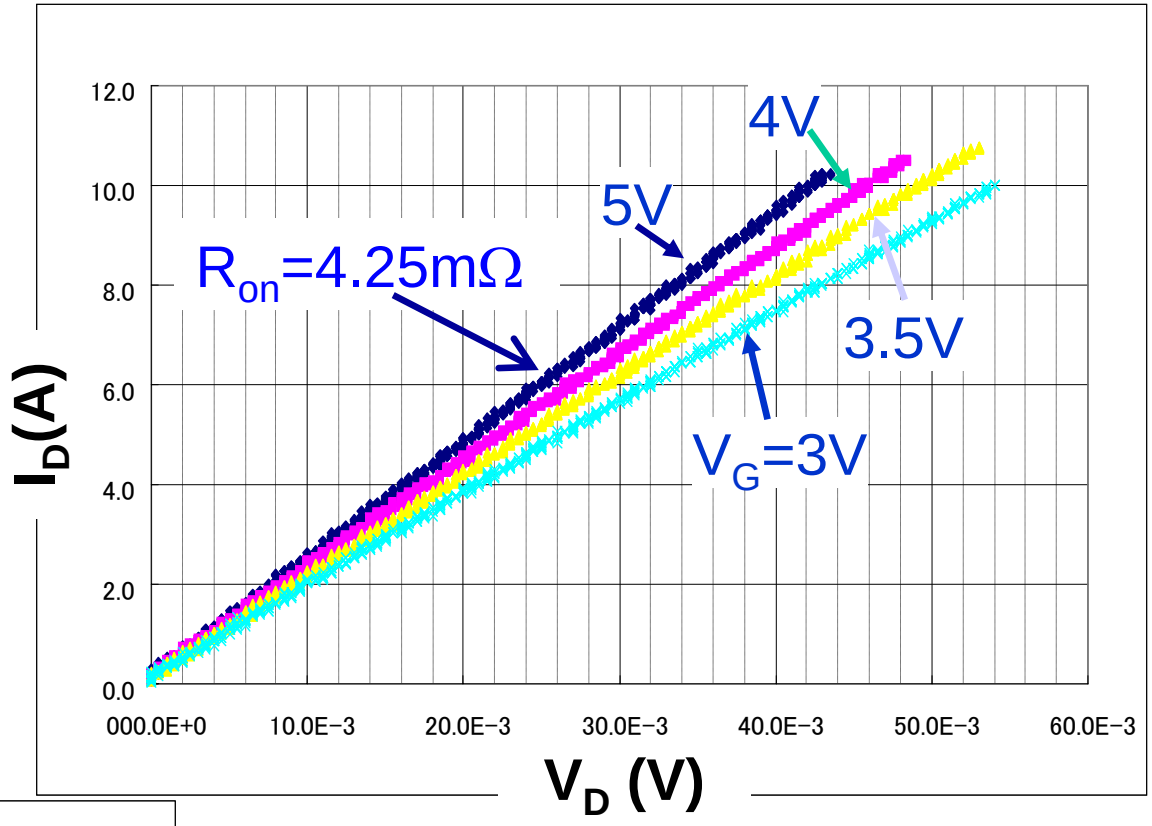


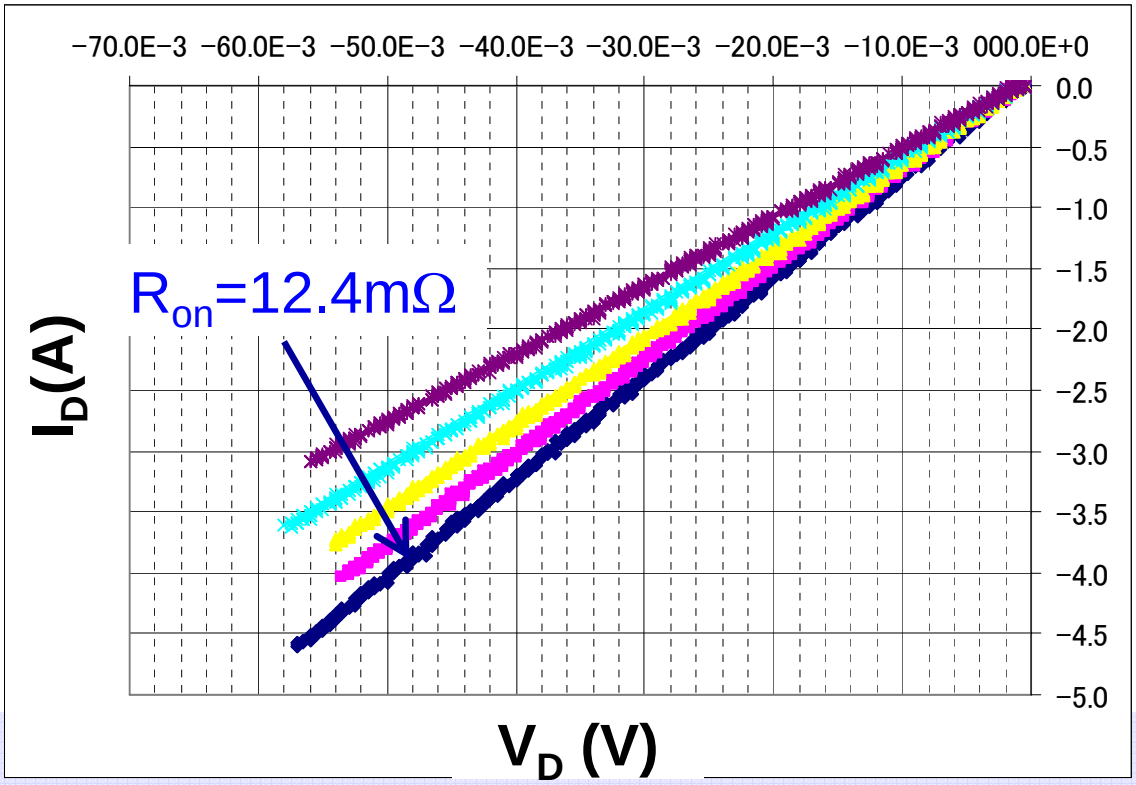
Ron :9.7m Ω(@Vgs=5V, Ids=5A)

5V NchMOS

Area 3.61mm^2

$R_{on}A$ 8.1mΩmm^2



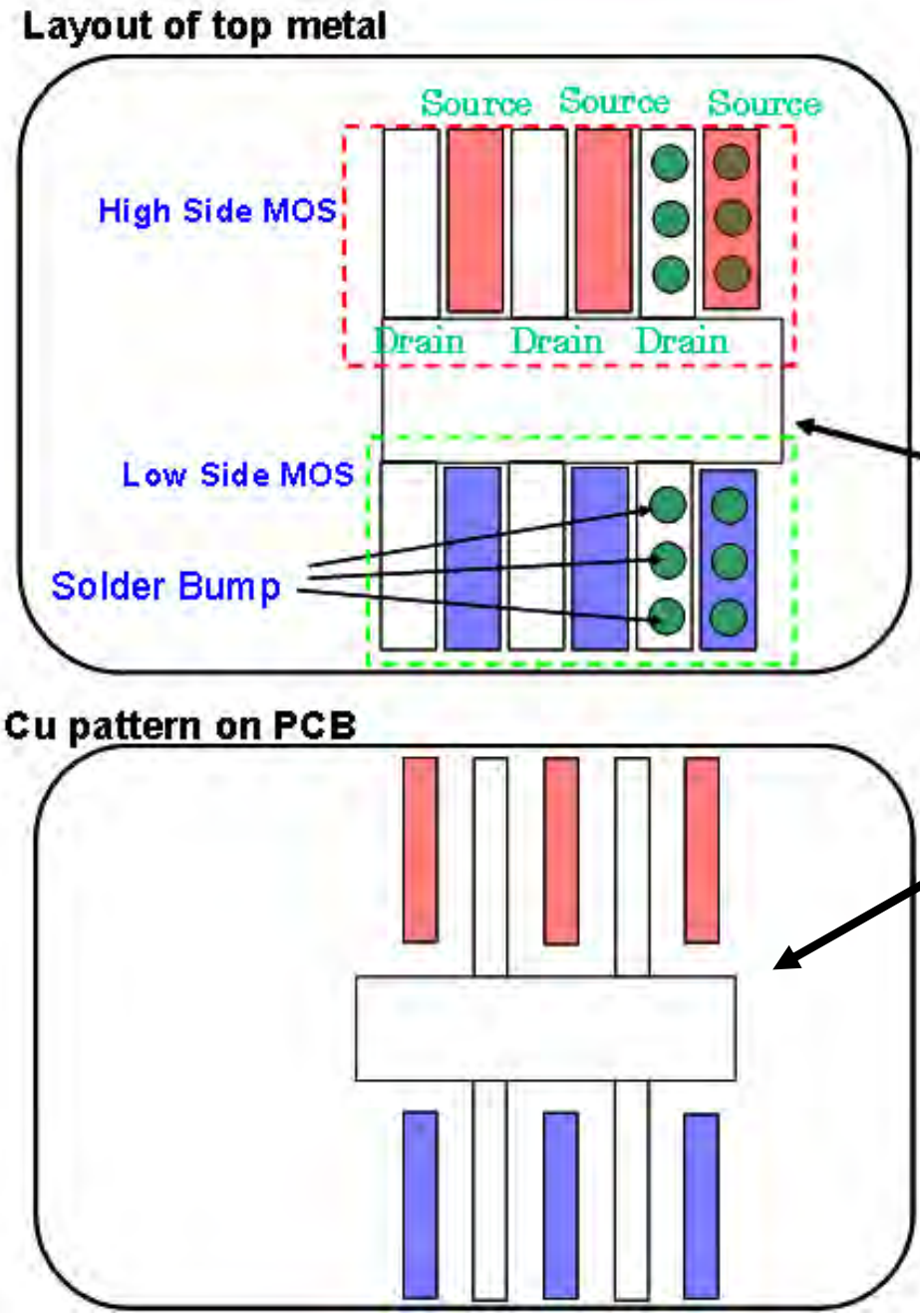


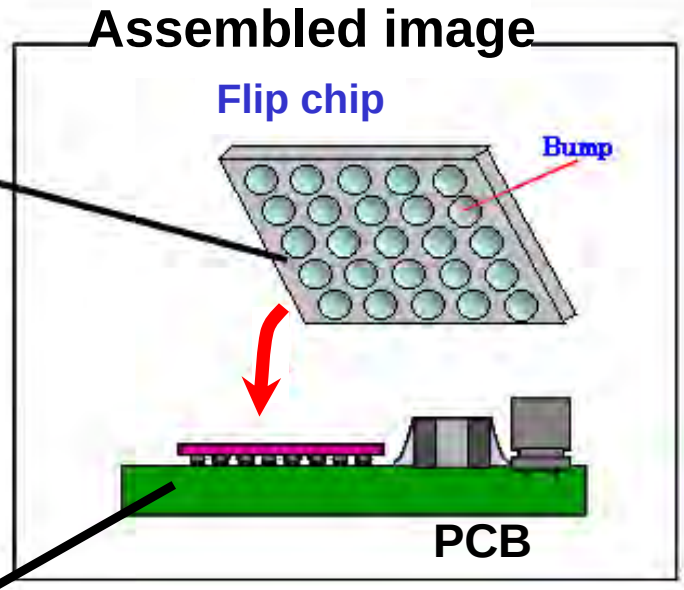
5V PchMOS

Area 3mm^2

$R_{on}A$ 30.5mΩmm^2

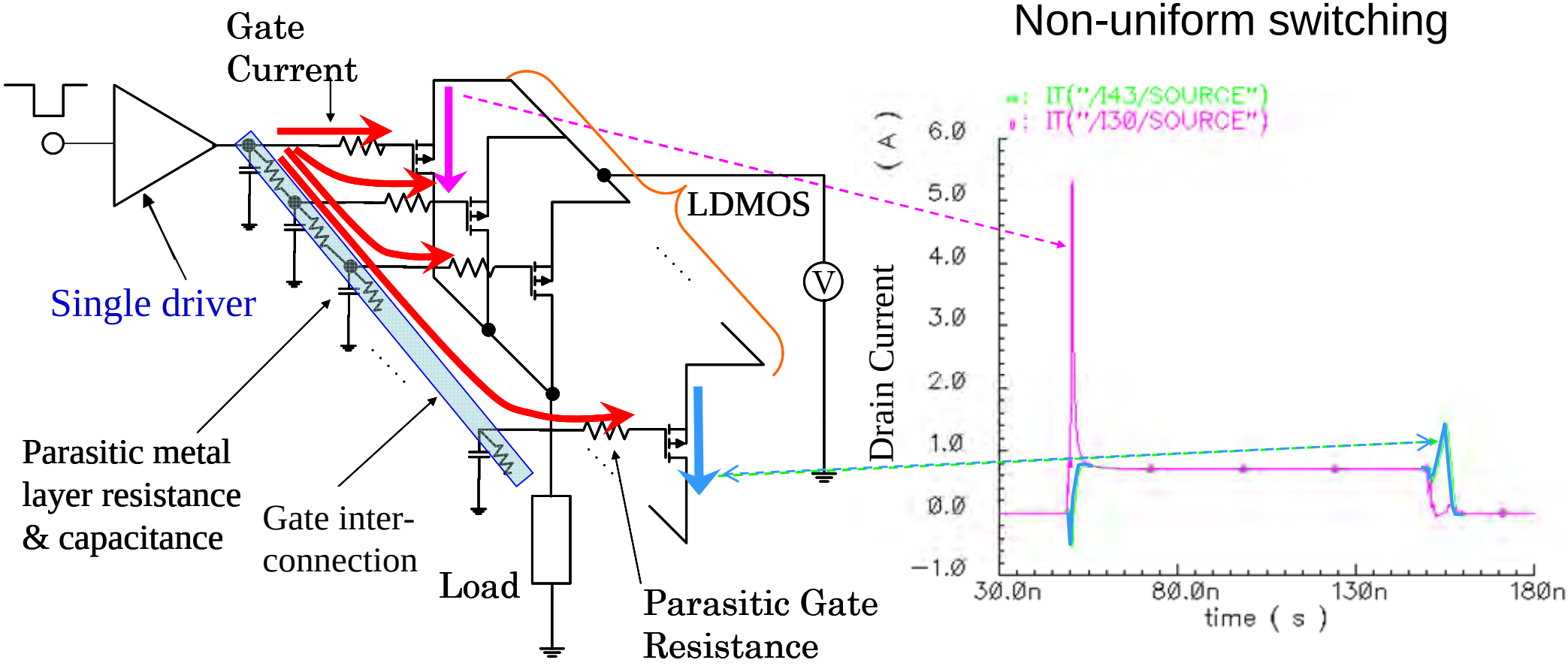
Interconnection resistance can be reduced by Bump Technology



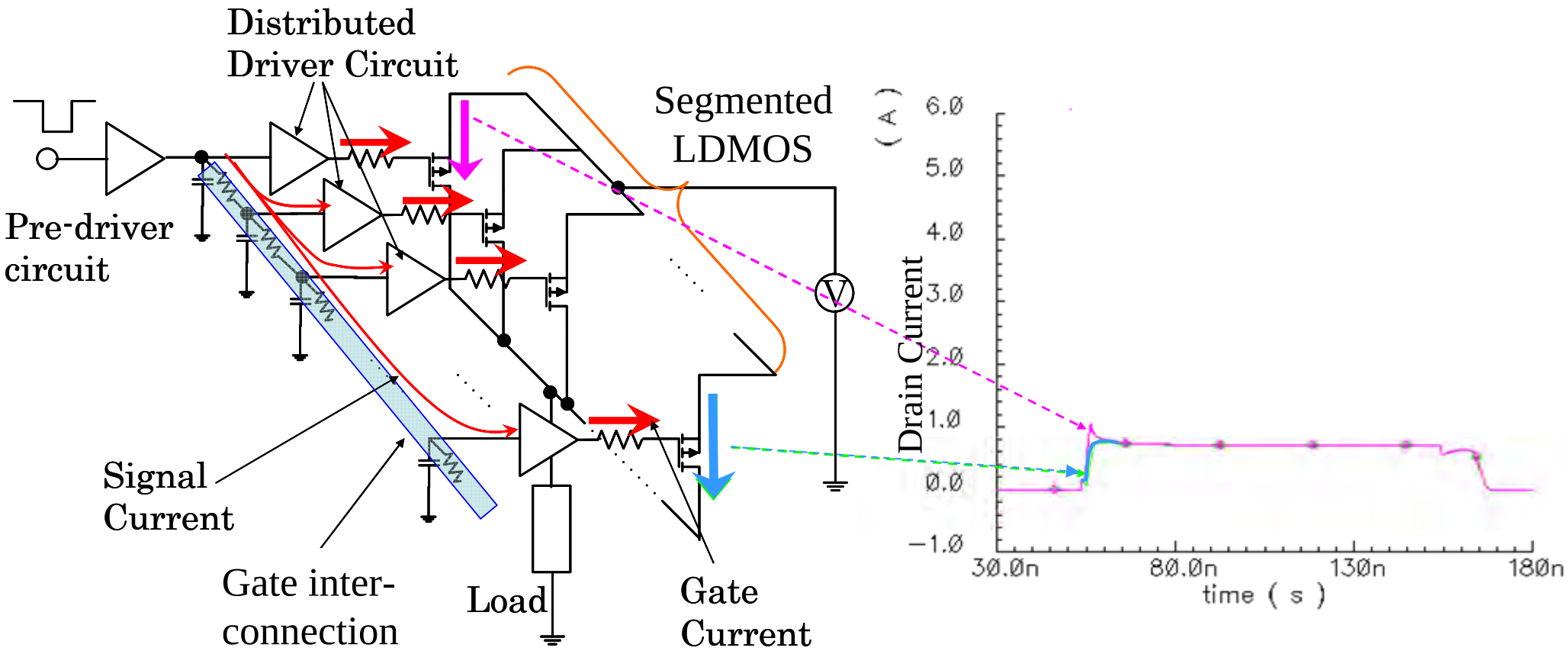


Thick Cu metal in PCB reduces interconnection resistance.

Single driver circuit layout

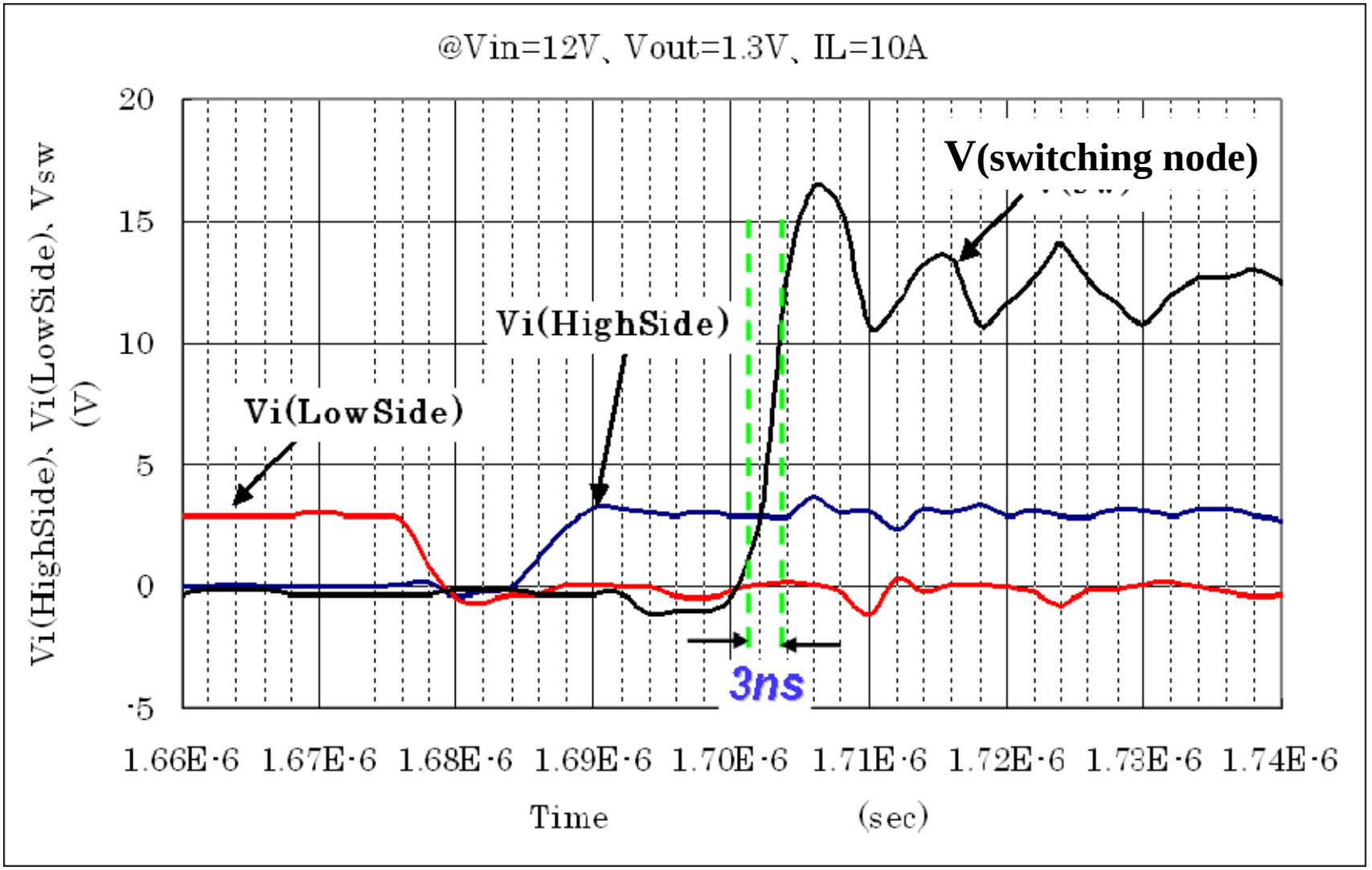


Distributed driver circuit layout

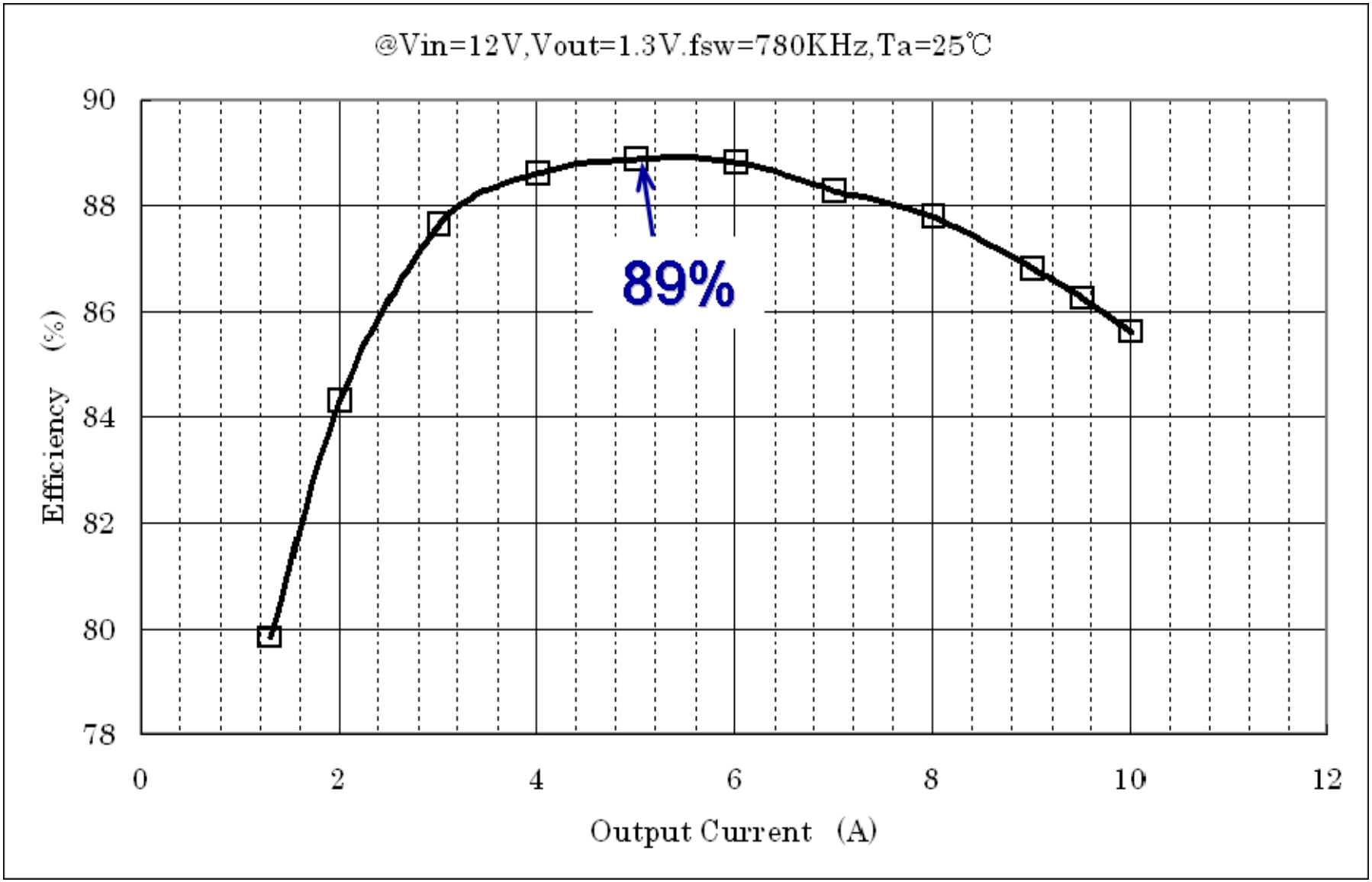


(@Switching frequency=780KHz, Input Voltage=12V, Load resistance=1.2Ω)

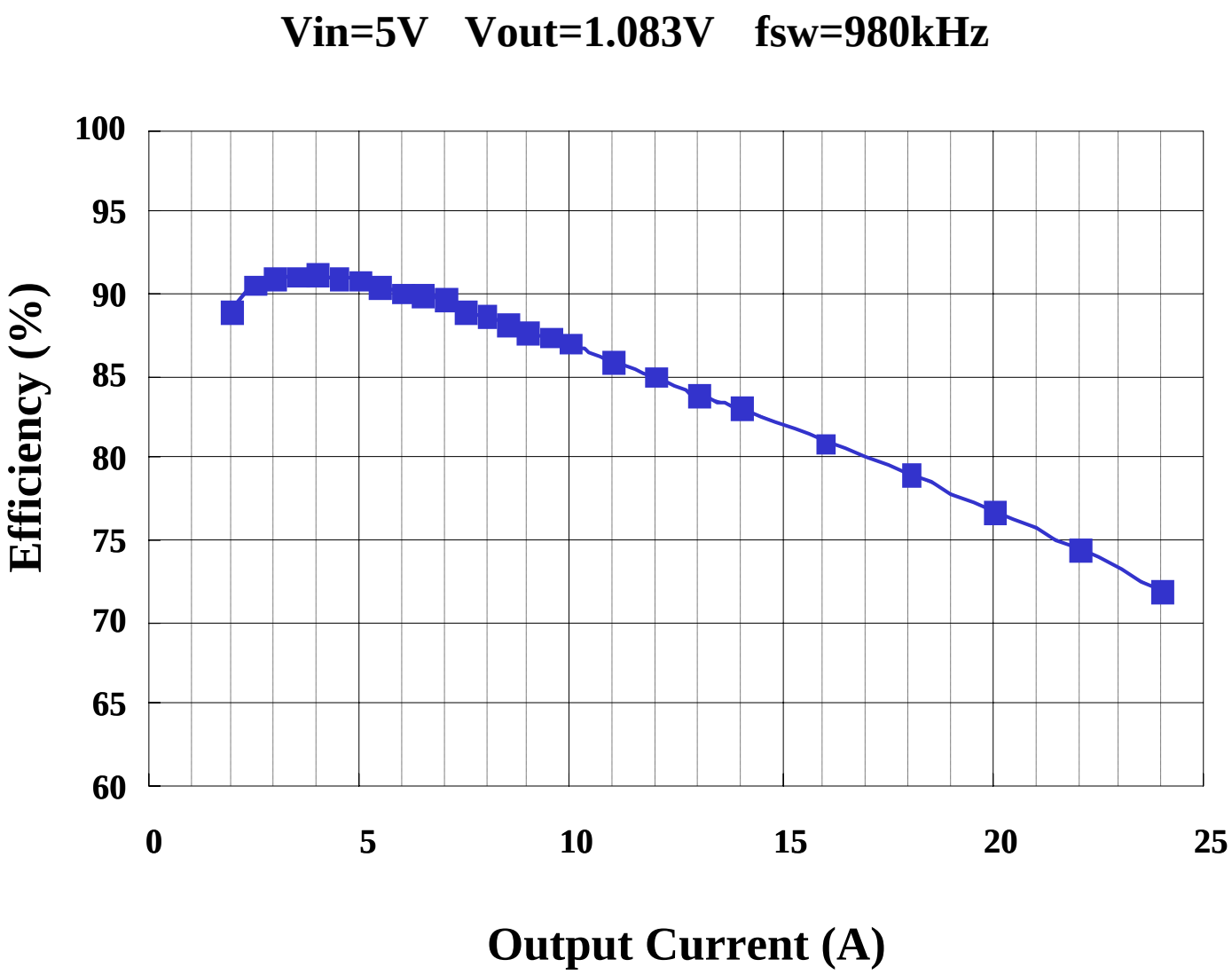
Switching waveforms



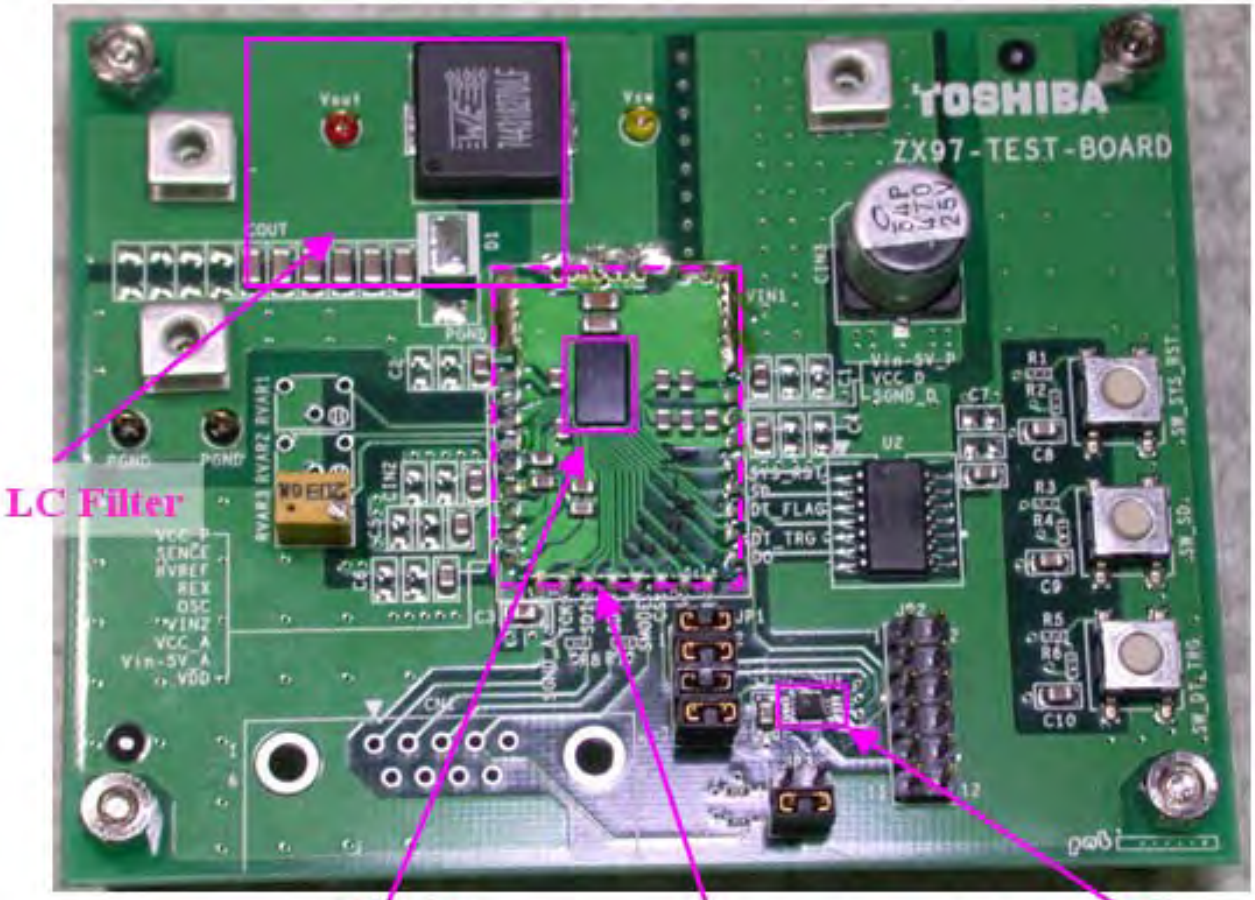
Measured efficiency vs. output current



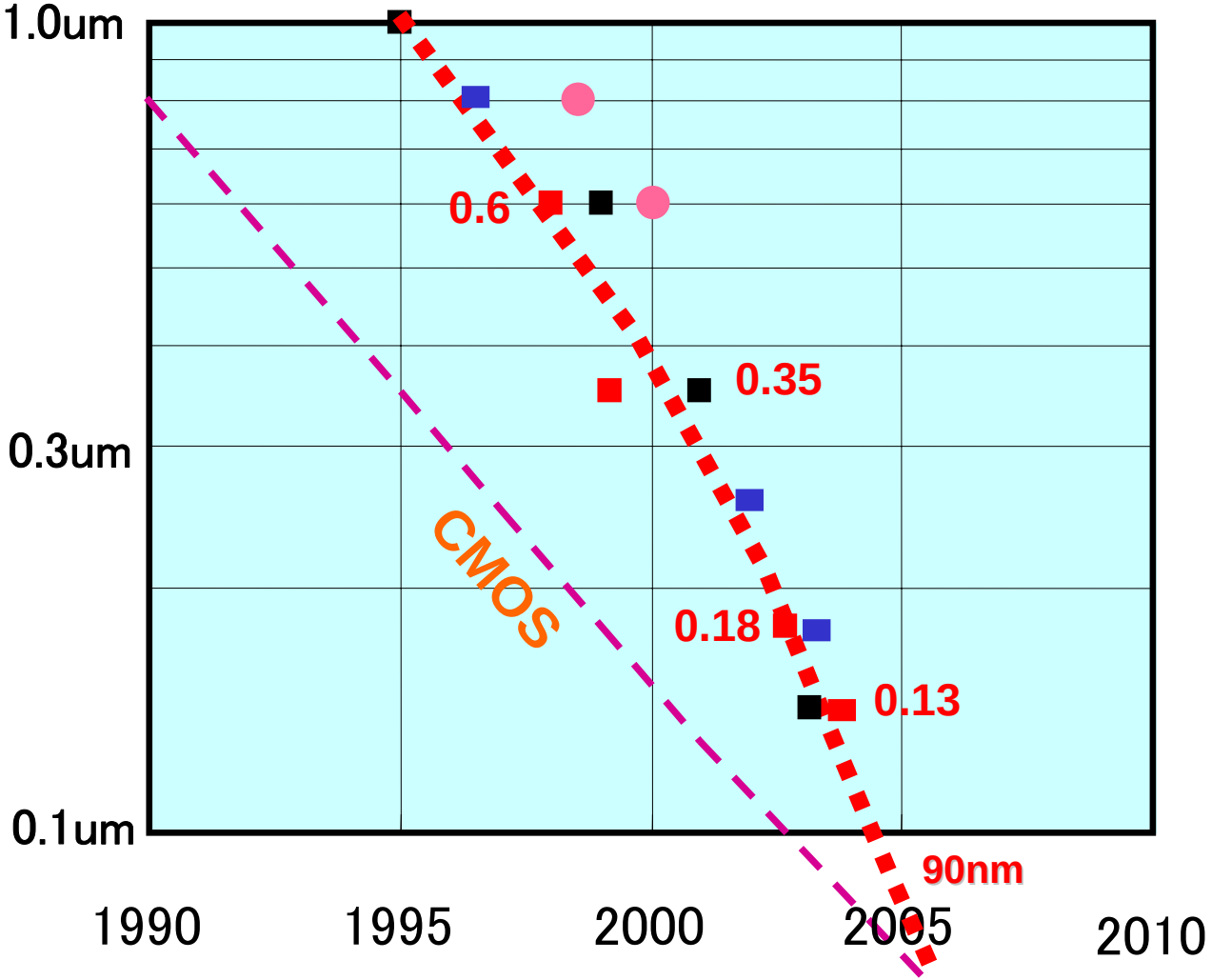
20A operation



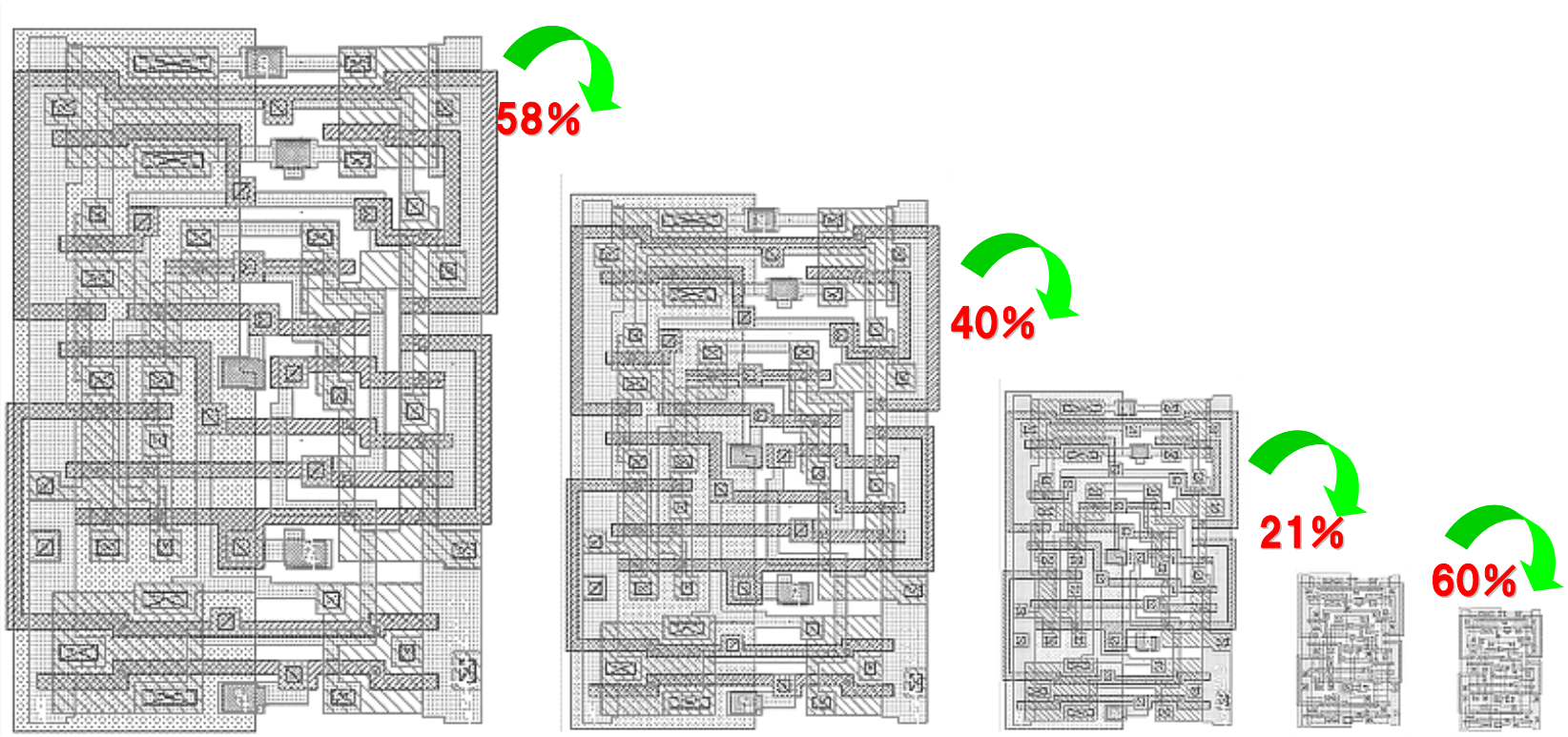
Evaluation PCB Board



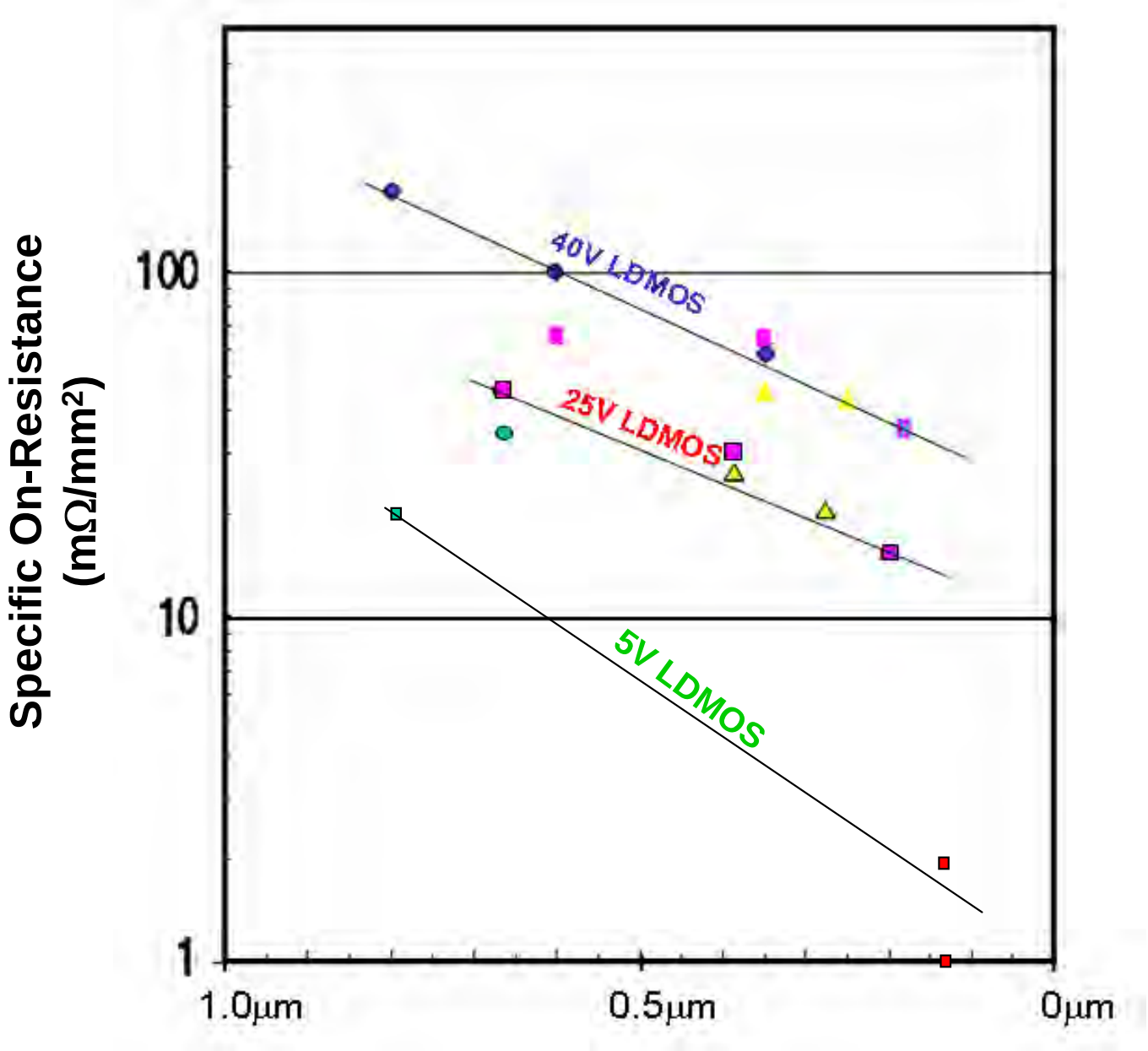
微細化するパワーICプロセス



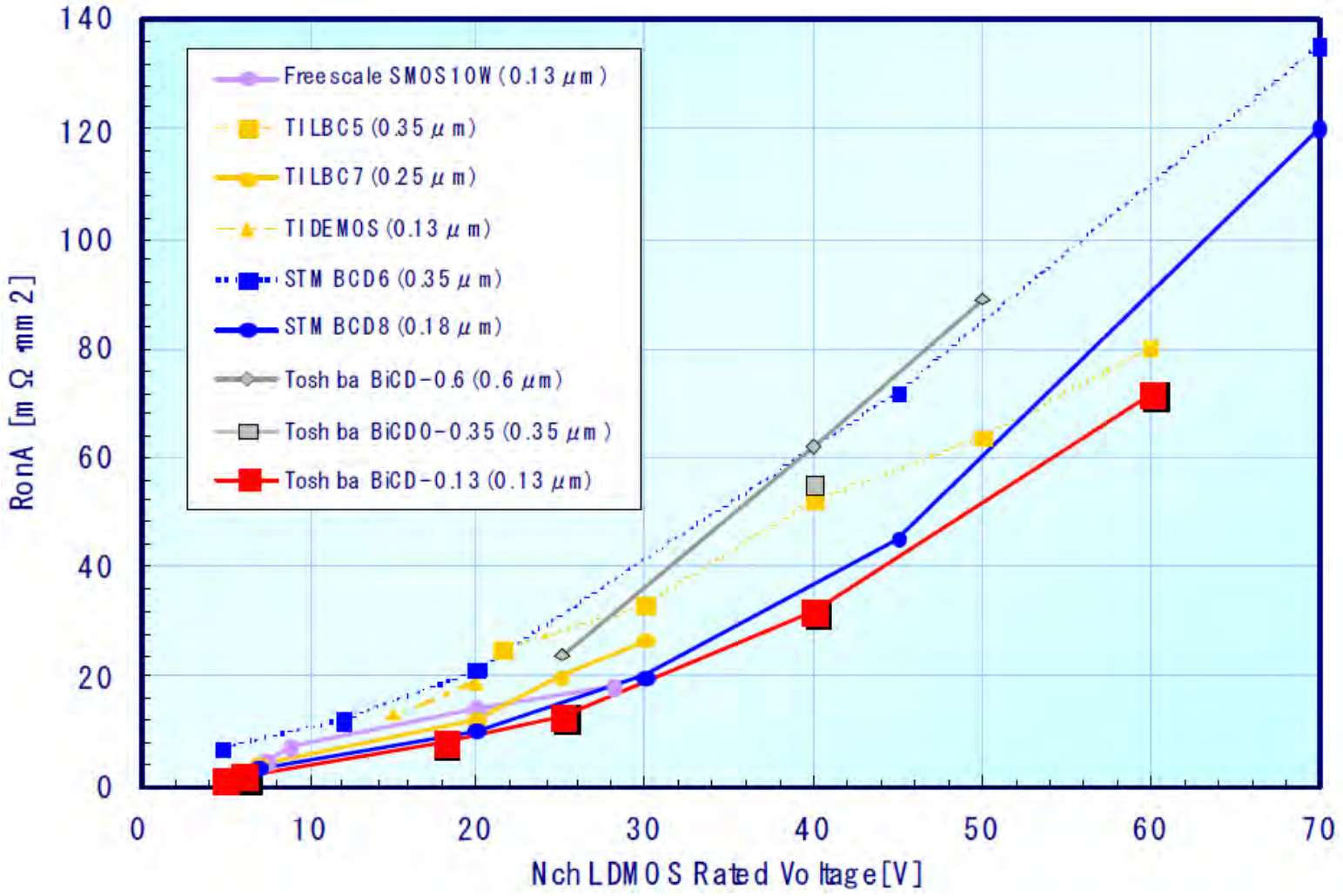
CMOS Logic area reduction



なぜ微細化なのか？


Specific On-Resistance
(mΩ/mm²)
100
10
1
40V LDMOS
25V LDMOS
5V LDMOS
1.0μm
0.5μm
0μm

nch-LDMOS On-Resistance



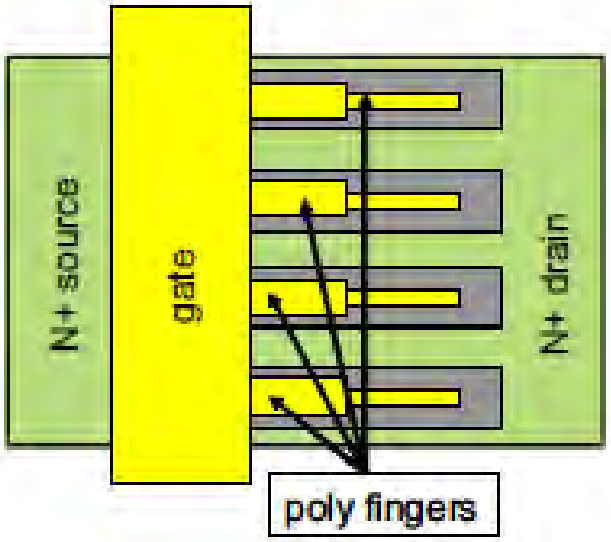
Data from ISPSD (2000 to 2007), VLSA-TSA (2008)

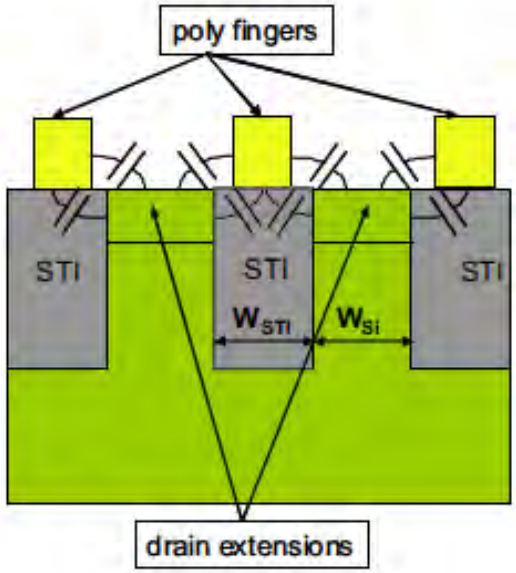
パワーICも65nmの時代へ

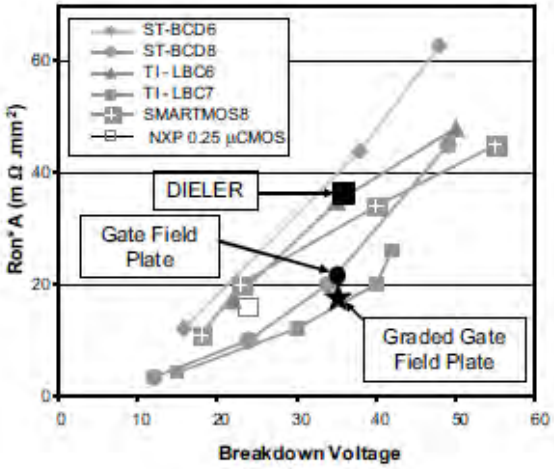
“Innovative lateral field plates by gate fingers on STI regions in deep submicron CMOS” ISPSD’08

A.Heringa, NXP-TSMC Research Center Leuven, Belgium

65nmCMOSプロセスを用いてマスク追加せずにLDMOSを作成する優れた手法。
ドレインのリサーフ条件を満たすためSTIを繰り返し入れることで平均の濃度を下げてリサーフ条件を実現。今回は更にSTI上にフィールドプレートを設けることでSJと同じ原理でオン抵抗を下げ、他社の0.18umBCDのLDMOS同等の特性を実現。今後、ファウンドリーを使うことが主流になる中、優れた手法。



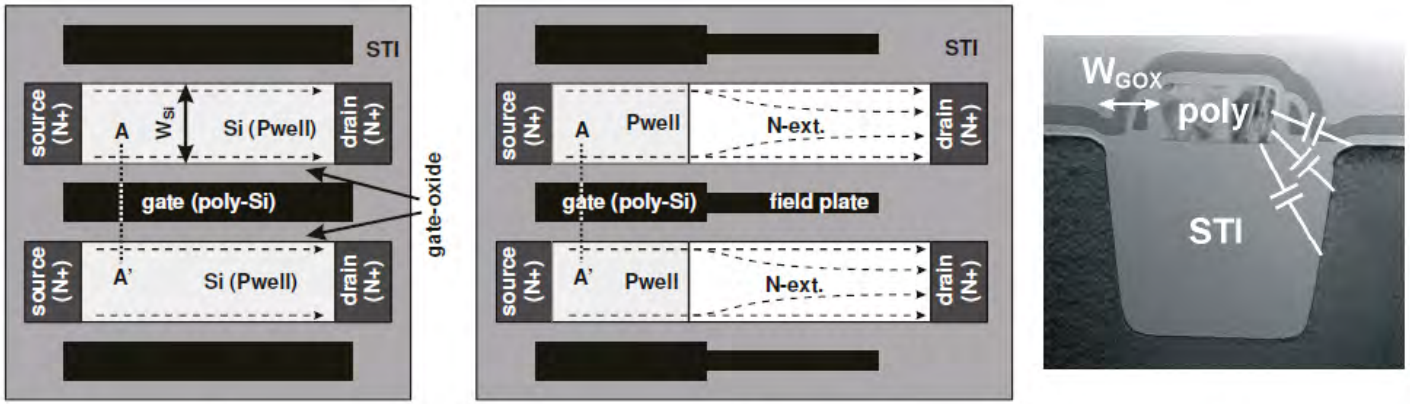




Towards universal and voltage-scalable high gate- and drain-voltage MOSFETs in CMOS

ISPSD’09

Jan Sonský, NXP-TSMC Research Center; Gerben Doornbos, Anco Heringa, Michiel van Duuren, NXP Semiconductors;
Jesús Pérez-González, NXP-TSMC Research Center



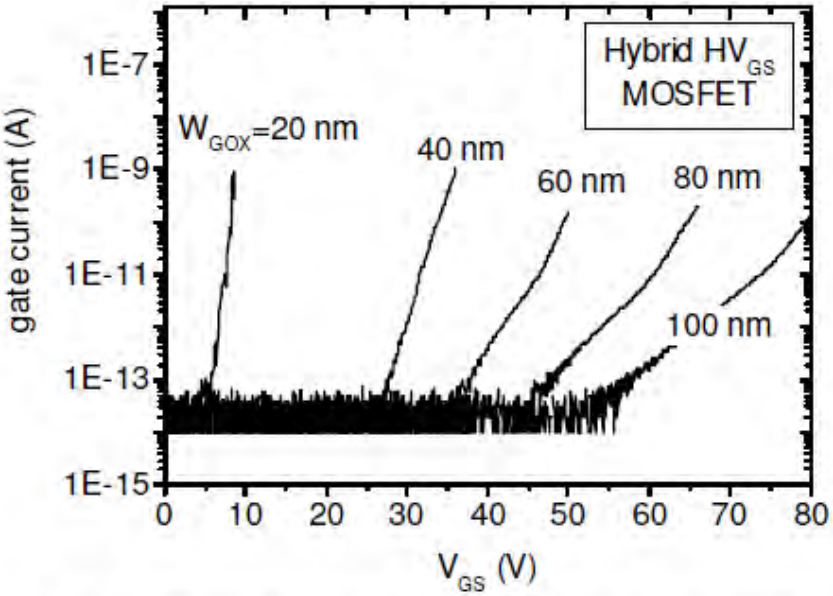
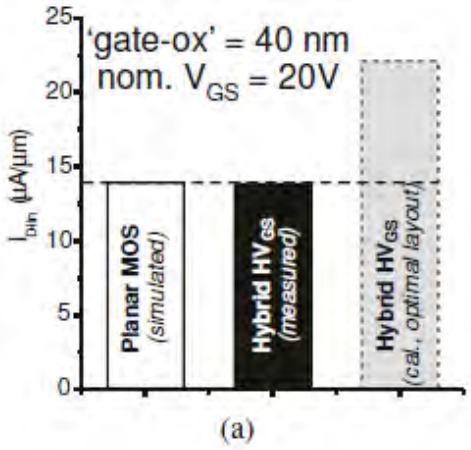
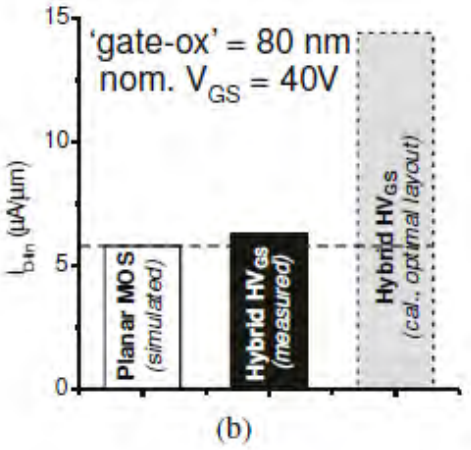


Figure 5. Measured gate-oxide breakdown characteristics of the Hybrid HV_{GS} transistor for different effective gate oxide widths.

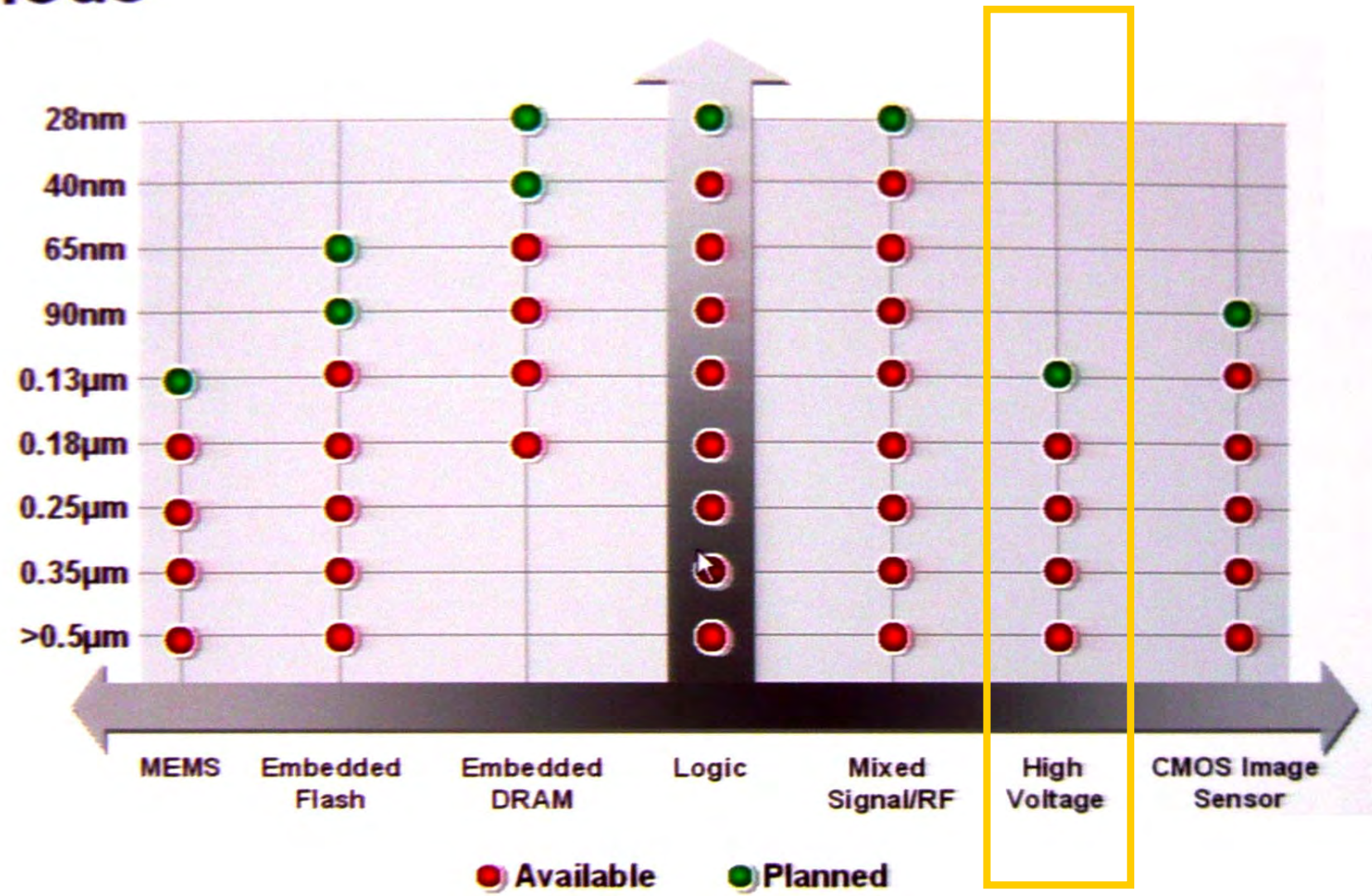




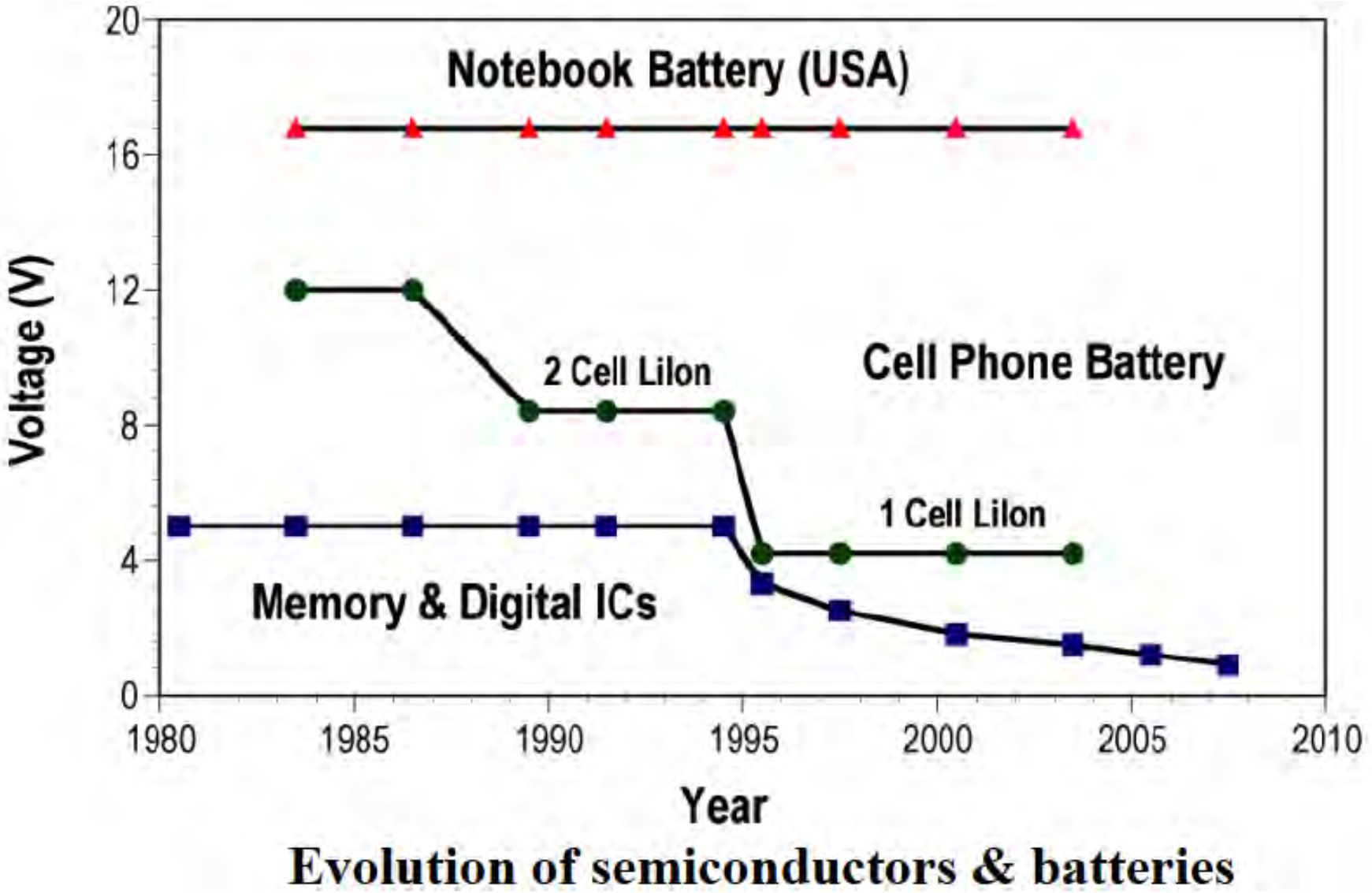
従来型のMOSFETと同等以上の特性可能

TSMC ファウンドリーの参入

0.18um – the widest built and adopted node



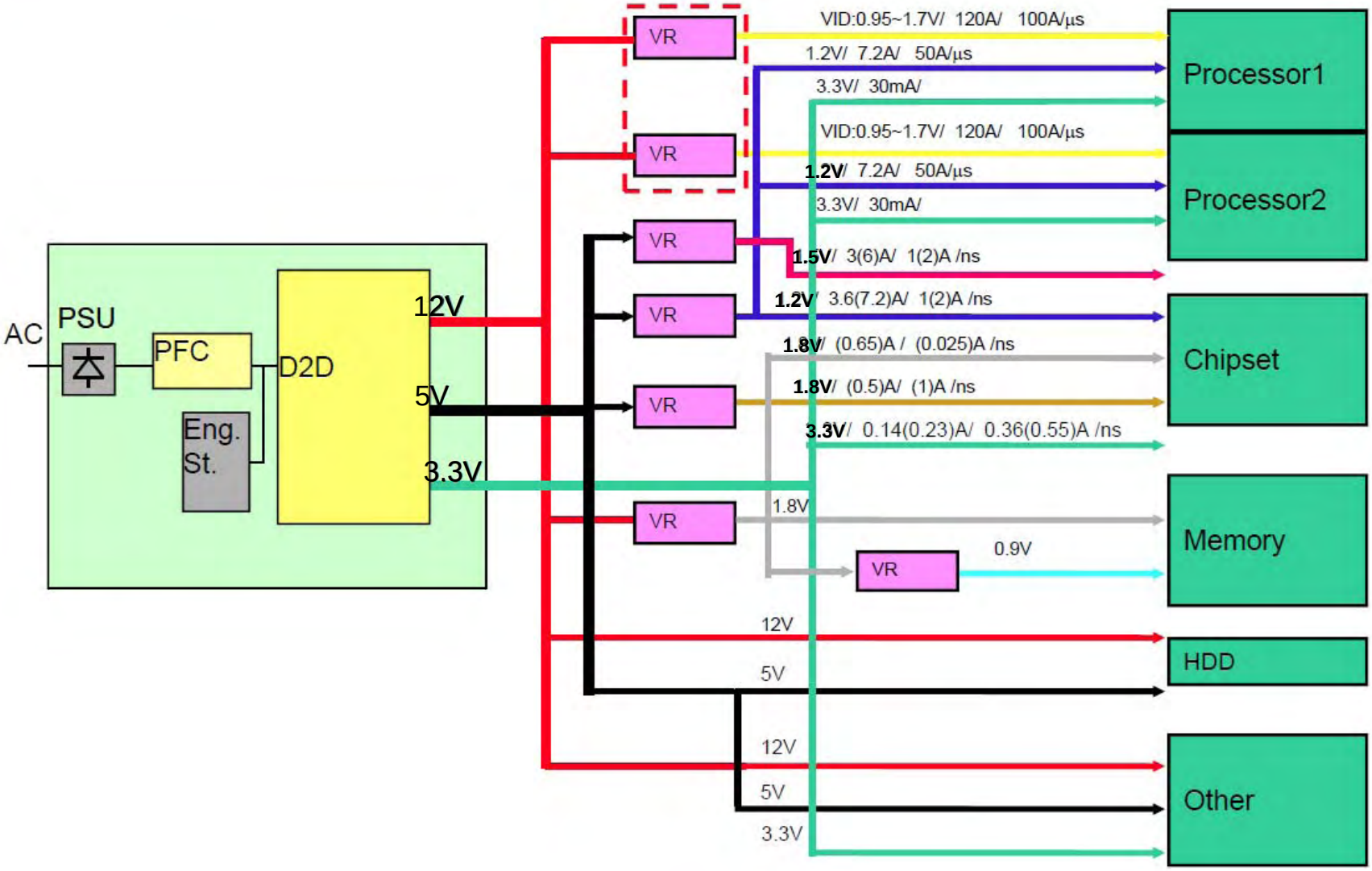
微細LSIの課題



Evolution of semiconductors & batteries

ISPSD'2000, R. Williams, Advanced Analogic Technologies, Inc.

Present Server Power Architecture



SoC、CPU の Power Crisis

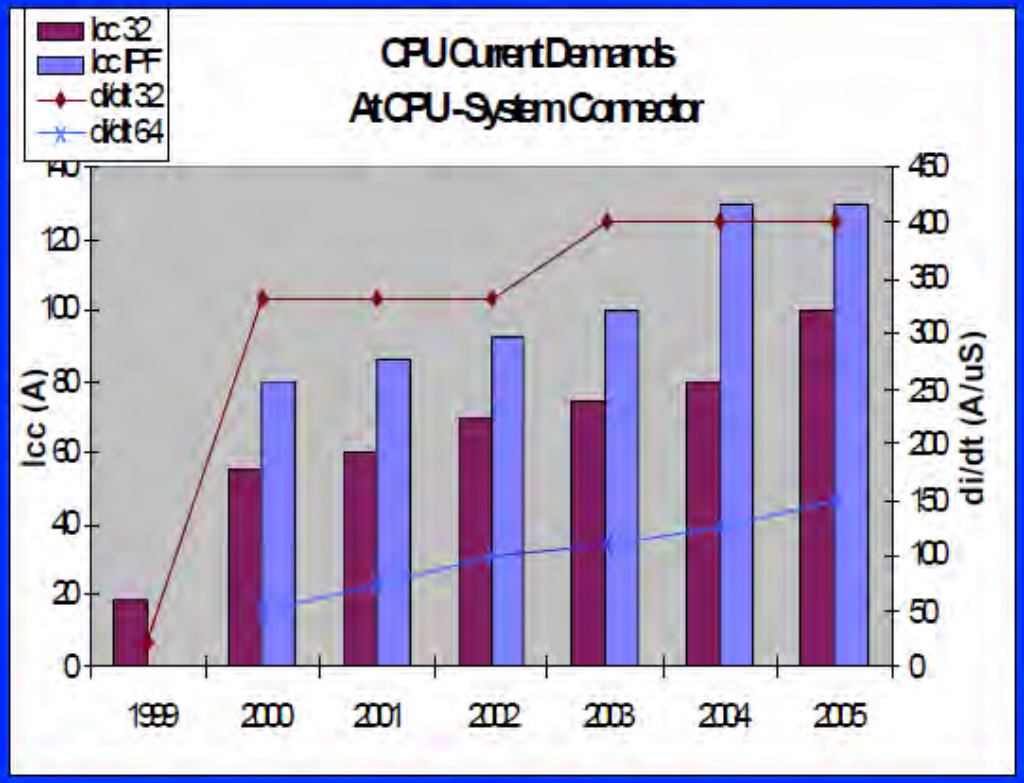
微細CMOSのCPU／SoCは消費電力大

SoCにDDコンを搭載して
低速で良い回路ブロックの電源電圧を
ダイナミックに下げる。

The CPU Load

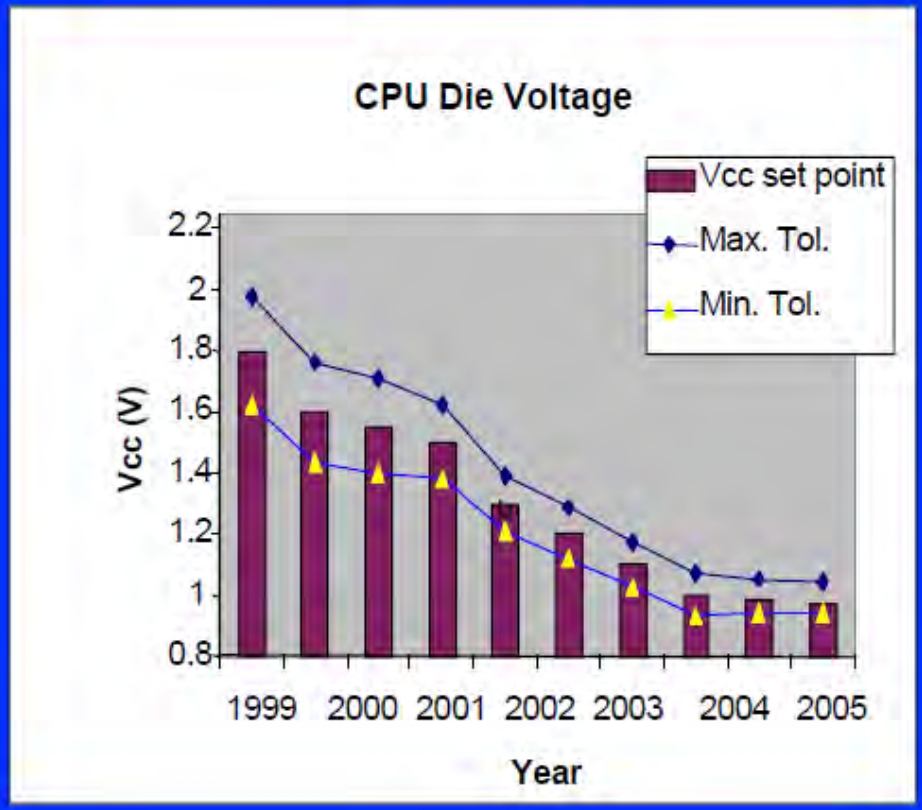
Current and Voltage

Intel Technology Symposium 2001



Icc ↑ 2X

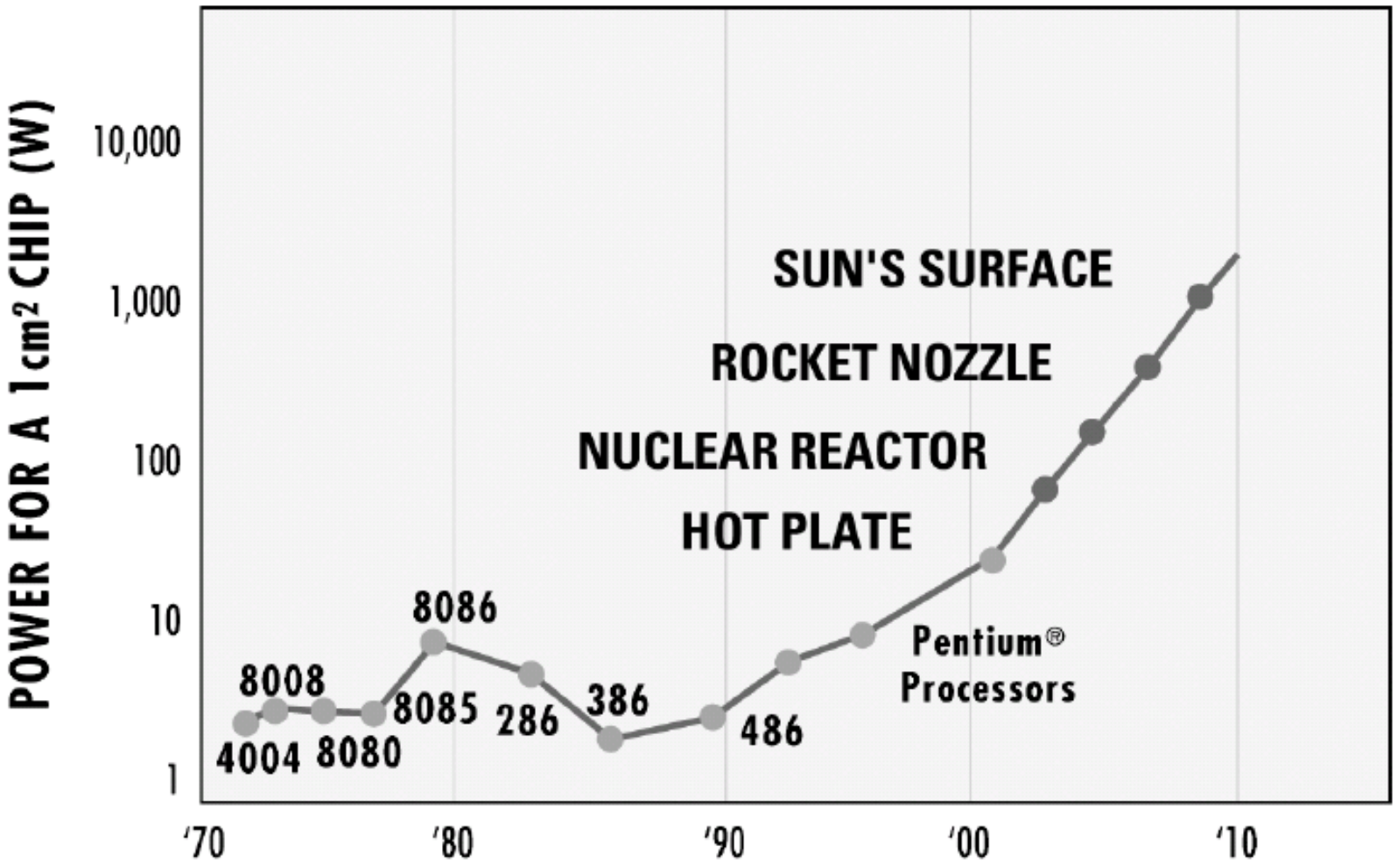
Vcc ↓ 1/3X



Z_{out} ↓ 3X

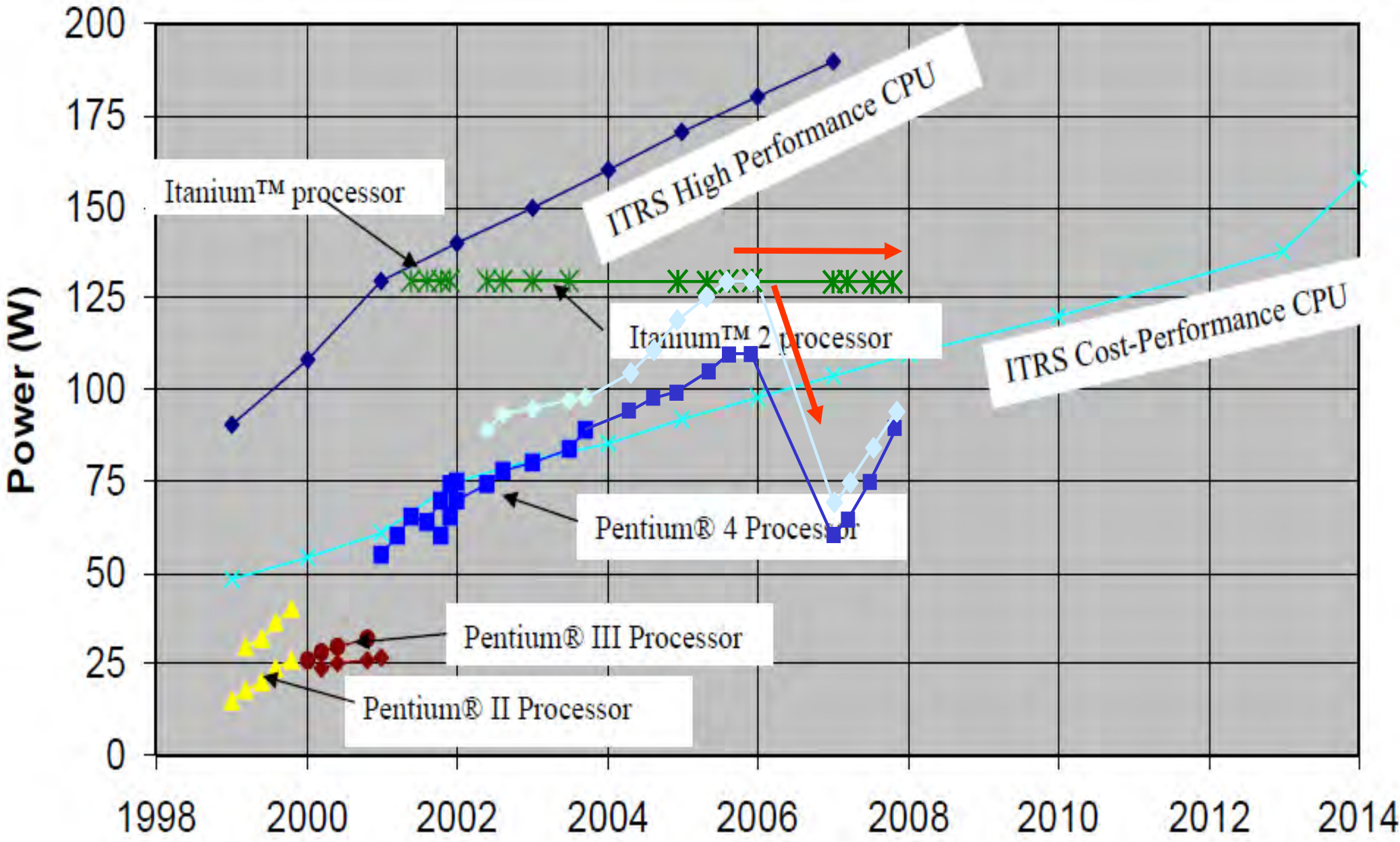
Economics demanding cost of VR remain flat

CPU、SoCのPower Crisis

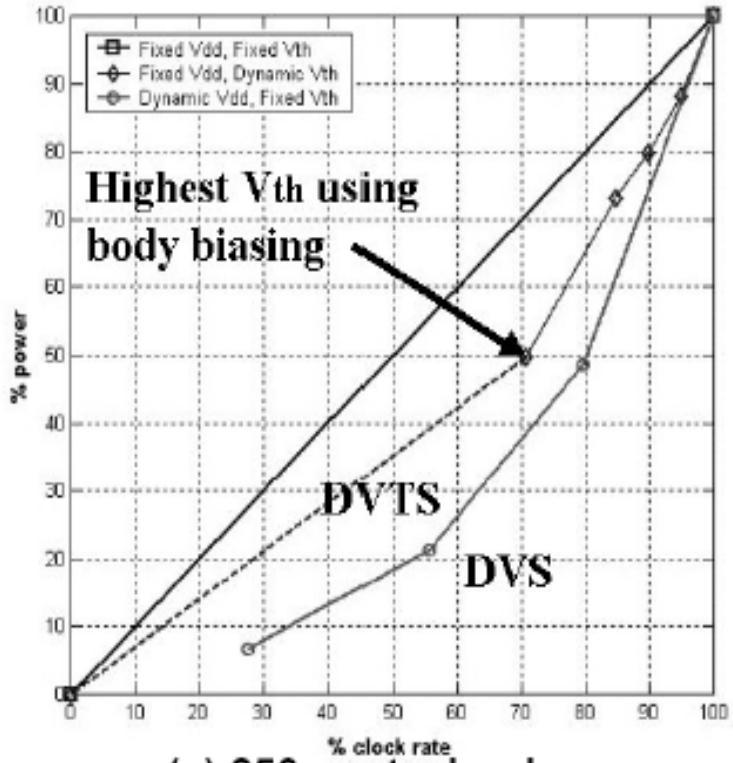


Power Requirements Roadmap for Intel's Microprocessors

CPUの高周波化の破綻

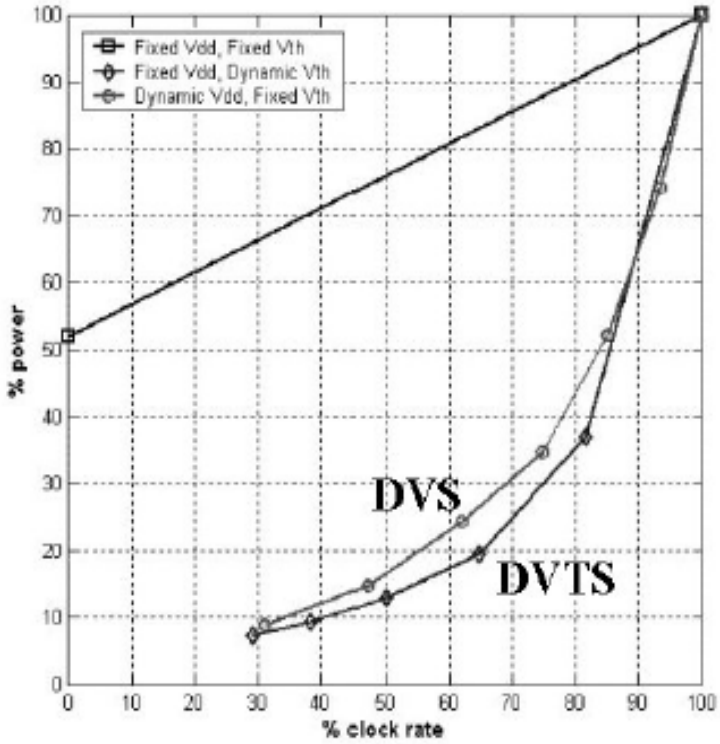


ISPSD'08 Plenary "Environmental Trends and Opportunities for Computer Power Delivery"
Edward Stanford, Intel



(a) 250 nm technology

(nominal VDD = 2.5 V, nominal VTH = 0.50 V)



(b) 70 nm technology

(nominal VDD = 0.9 V, nominal VTH = 0.15 V)

ARM社の「電力半減」技術 試作チップで実証段階へ

電圧調整の中核部はFPGAに実装

英ARM Ltd.は，米National Semiconductor Corp.（NS社）と共同開発中の電力制御技術「Intelligent Energy Management（IEM）」を実装したマイクロコントローラを試作した[注1]。2003年8月18日～19日に米Stanford Universityで行われた半導体関連技術のシンポジウム「A Symposium on High Performance Chips 15（HOT Chips 15）」で明らかにしたものである（図1）。

IEMの特徴は，チップの製造時に発生するトランジスタ特性のバラつきを個々のマイクロコントローラが自ら測定しつつ，動的に電源電圧と動作周波数を自動調整すること[注2]。米Transmeta Corp.の「Crusoe」や米Intel Corp.の「Pentium M」では，通常すべてのチップに同じ制御パラメータを適用して電源電圧と動作周波数を切り替え，消費電力を下げる。個体差を考慮しないので，出来がよくないチップでも正常に動くよう電源電圧の下限値などを高めに設定せざるを得ない。こうした現行技術に比べてIEMでは消費電力を6割以上減らせる場合があるとNS社はみる。

ARM社はIPコアを提供する事業形態を採るので，チップの製造技術はライセンス先によってまちまちである。IEMは，こうした製造技術の違いを超えて省電力効果を得ることにも役立つ。

肝心の部分はFPGAで実装

IEMを実現するハードウエアは，CPUコアの負荷や動作周波数を監視する「Intelligent Energy Controller（IEC）」や電源電圧を制御する「Adaptive Power Controller（APC）」，APCの指示に応じてクロック周波数を動的に変更する「Dynamic Clock Generator（DCG）」などから成る。ARM社はこのうち，IECとDCGをCPUコア（ARM926EJ-S）と共に試作チップに集積した。IEMの「要」といえるAPCは，外付けのFPGAに実装した。製品化に向けた試行錯誤を容易にするためである[注3]。

試作チップにはこのほかTCMS（tightly coupled memory with state retention）と呼ぶRAMを組み込んだ。CPUコアの電源を一時的に切る際，レジスタ内のデータを退避するのに使う。

ARM社とNS社は，APCと電源回路を結ぶ「PowerWise」と呼ぶ電力制御インタフェースの仕様を2003年9月以降に公開する。2本の信号線を用いて電源回路に対して出力電圧を指示するもので，現在複数のメーカーが採用を検討しているという。

（菊池 隆裕＝シリコンバレー支局，枝 洋樹）

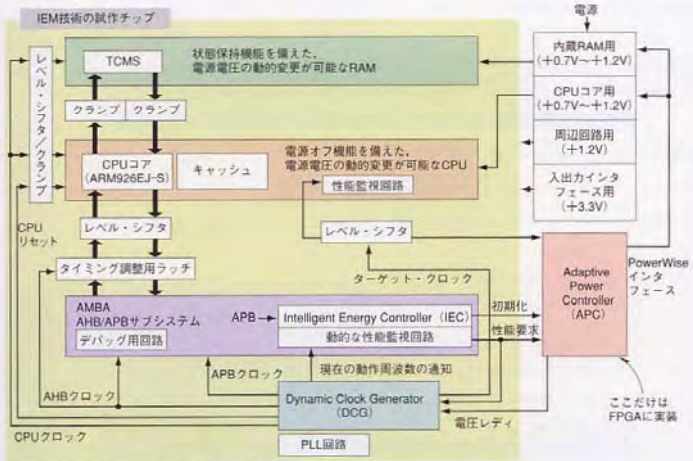


図1　IEM技術を盛り込んだ試作チップのブロック図
CPUコアの負荷状況を監視して動作周波数を決める。その際，Adaptive Power Controller（APC）が製造時のプロセスのバラつきや動作中の温度上昇によるトランジスタ特性の変化を考慮して電源電圧を調整する。詳細は明らかにしていないものの，信号の伝播時間を測定するための専用論理回路をマイクロコントローラに集積し，ある範囲よりも遅延が大きければ電源電圧を上げ，小さければ電源電圧を下げる制御を行うもよう。

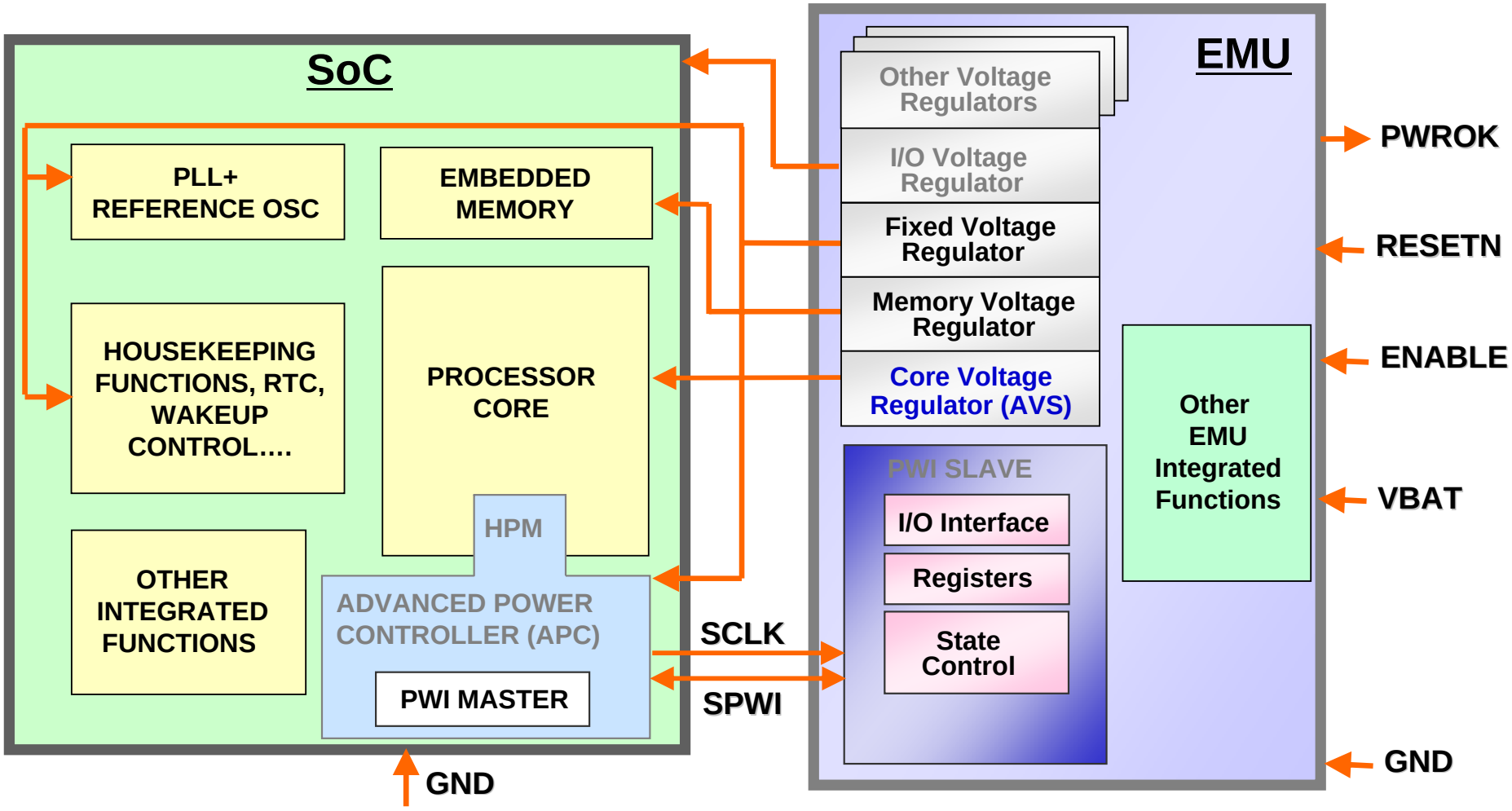
注1）ARM社は2002年11月，National Semiconductor社と共同開発することを発表しており，2003年6月に米国で開かれた「Embedded Processor Forum 2003」などでその概要を明らかにしている。今回の発表は，それに続くものである。

注2）同様な電力制御技術は，ソニーも携帯型情報機器「CLIE（PEG-UX50）」に搭載したマイクロコントローラ「Handheld Engine」に採り入れている。

注3）ARM社は試作チップの消費電力の実測値を今回明らかにしなかった。「製造を委託した台湾Taiwan Semiconductor Manufacturing Co.,Ltd.（TSMC）から先週手に入れたばかり」（発表者の同社Engineering FellowのDavid Flynn氏）で，データの収集はこれから始める。

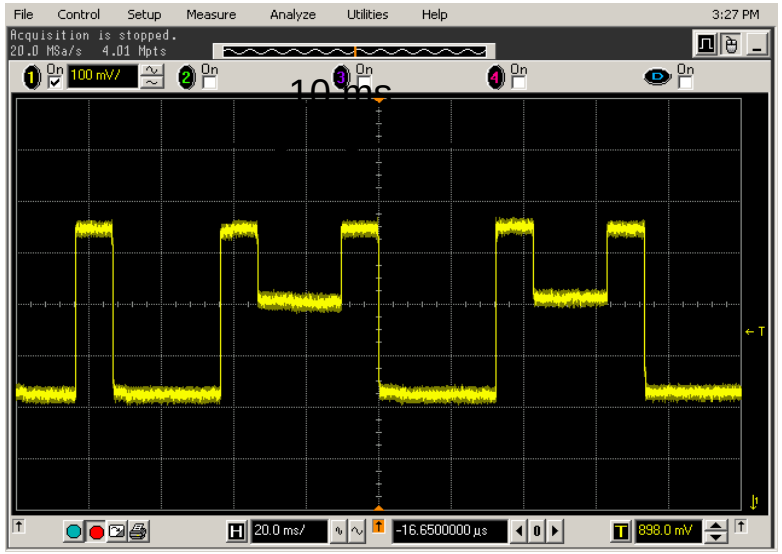
2003.9.1号

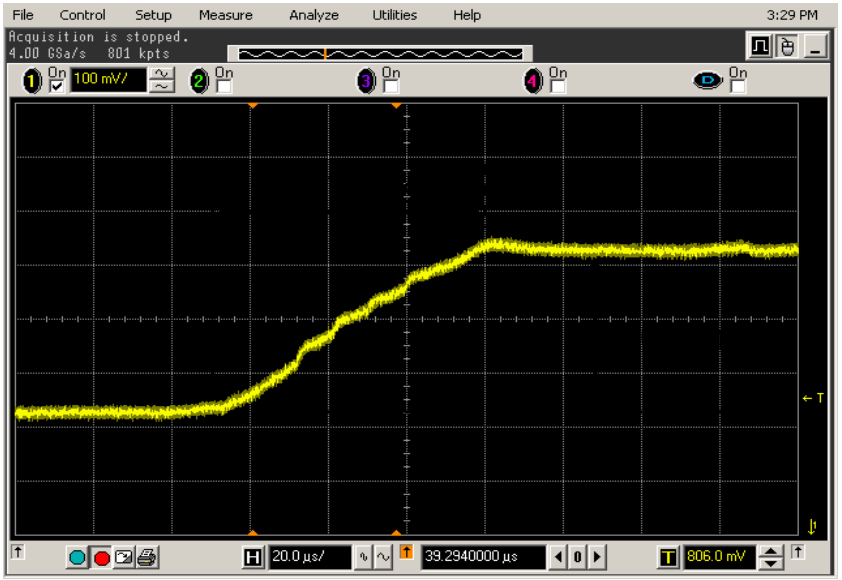
PowerWise™ AVS System

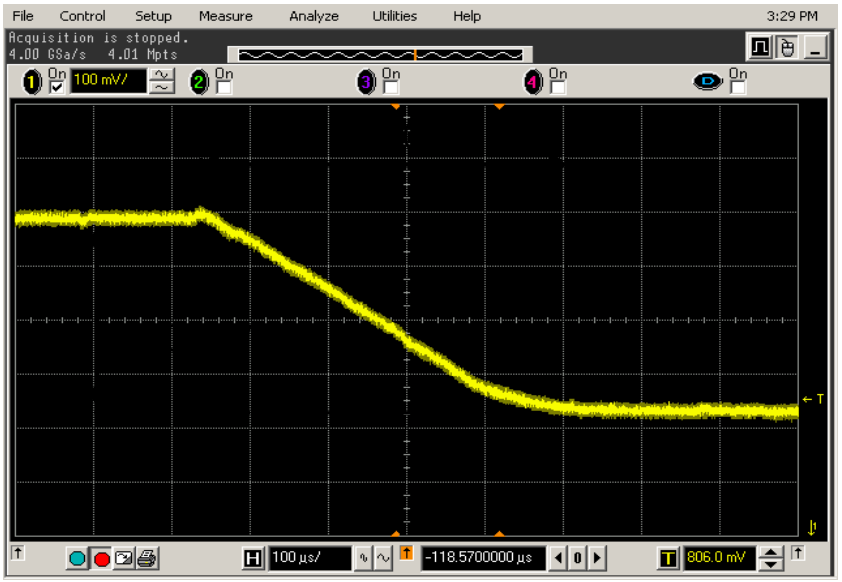


Voltage Slewing

MPEG4 (with IEM)





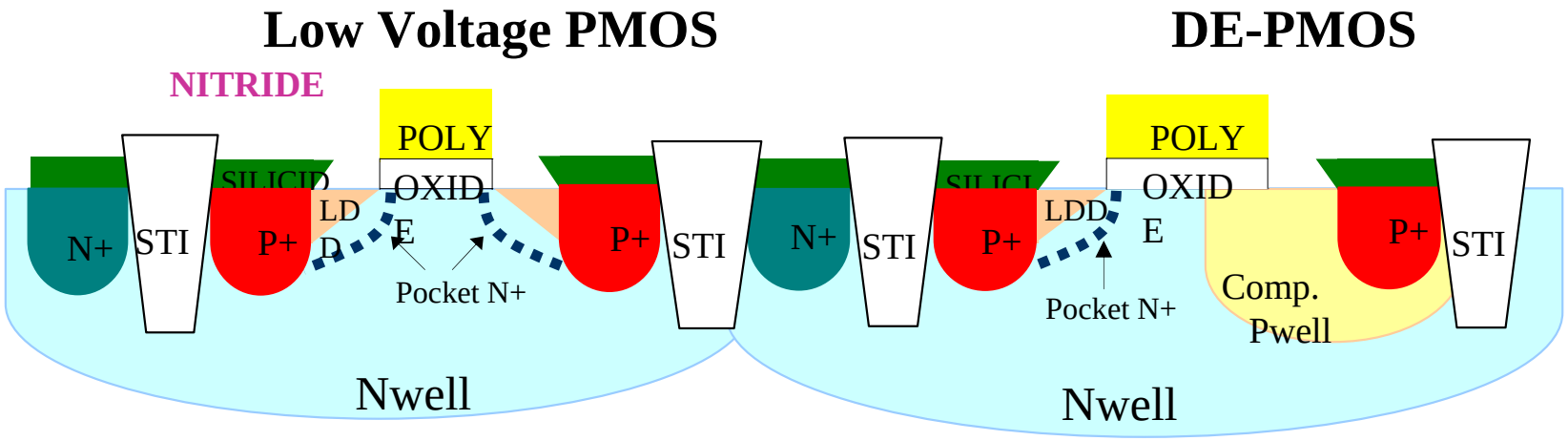


ISPSD'04

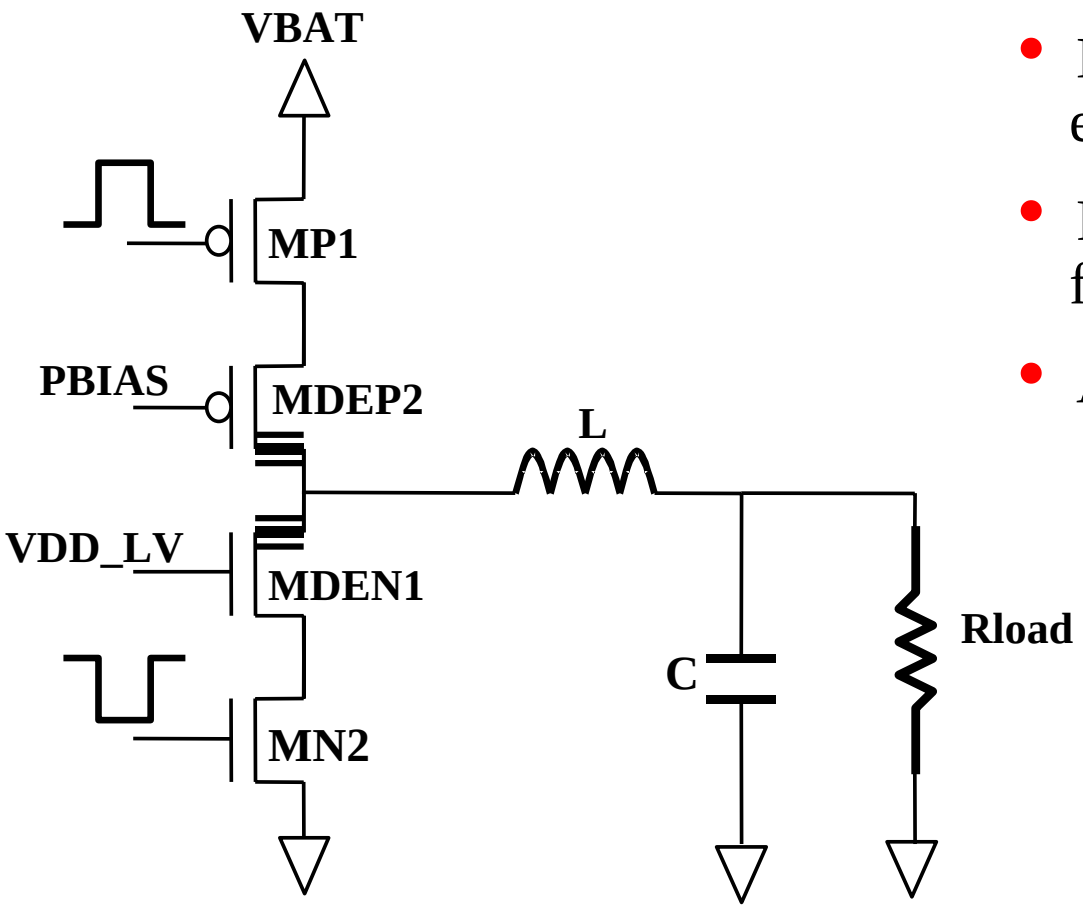
"A High Efficiency Ultra-Deep Sub-Micron DC-DC Converter for Microprocessor Applications"

Byron Reed, Jun Chen, Valerian Mayega, Kevin Ovens, and Sami Issa,
Texas Instruments

- First pass design of the DC-DC converter was done in a baseline 90nm process.
- It is a discrete converter that uses a serial bus for communication of the voltage level to OMAP™.
- For future 90nm and 65nm designs the SmartReflex™ DC-DC converter will be integrated with OMAP™.
- No unique design techniques are used in the 90nm baseline process that will prevent it from being migrated to the 65nm baseline process.

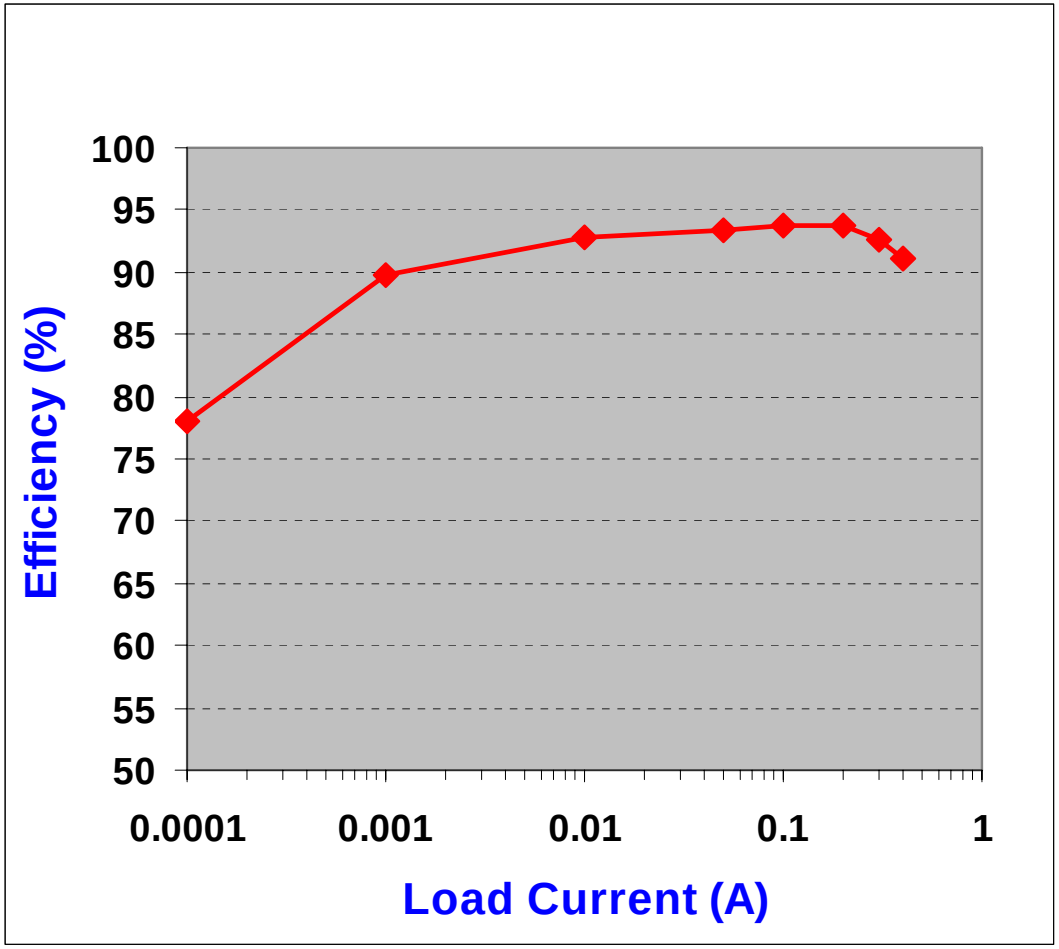


DC-DC Converter Output Stage



- MP1 is an HVG (1.8V) device.
- MN2 is a LV device.
- MDEP2 and MDEN1 are drain extended HVG devices.
- PBIAS is a bias voltage referenced from VBAT.
- Advantages of this cascode structure:
  - Allows high voltage operation.
  - Has less off mode leakage.
  - Has smaller gate capacitance that has to be switched than if a single DE device was used.

Simulated Efficiency VS Load Current



- Vin = 3.6V
- Vout = 1.3V
- PWM mode from 100mA to 400mA
- PFM mode from 100uA to 50mA
- Includes parasitic resistances

IEEE Applied Power Electronics Conference
February 15th to 19th, 2009
Invited Plenary Session

Power Supply on Chip Has the Ship Come In?

Dr. Cian Ó Mathúna

Tyndall National Institute,
Cork, Ireland.

cian.omathuna@tyndall.ie

www.tyndall.ie

Tyndall National Institute

Power supply integrated into system chip (i.e. the load)

- Power on Complex System Chip (e.g. 65nm IC):
  - Analog - 1.8 V
  - I/O - 2.5 V, 1.8 V
  - RF - 3.3 V, 2.5V
  - Digital - 1.2 V

  - Analog - up to 5 isolated supplies to minimise noise

  - Digital - 4 to 5 power domains
    - can be turned on/off independently
    - can be run at lower voltages if less processing power needed (dynamic voltage scaling)

Progression to Power Supply on Chip - PwrSoC

- Trend:
  - Escalating number of power supply rails
  - Need to minimise number of external components on PWB

- **Bottleneck - Integration of Passives onto Silicon**

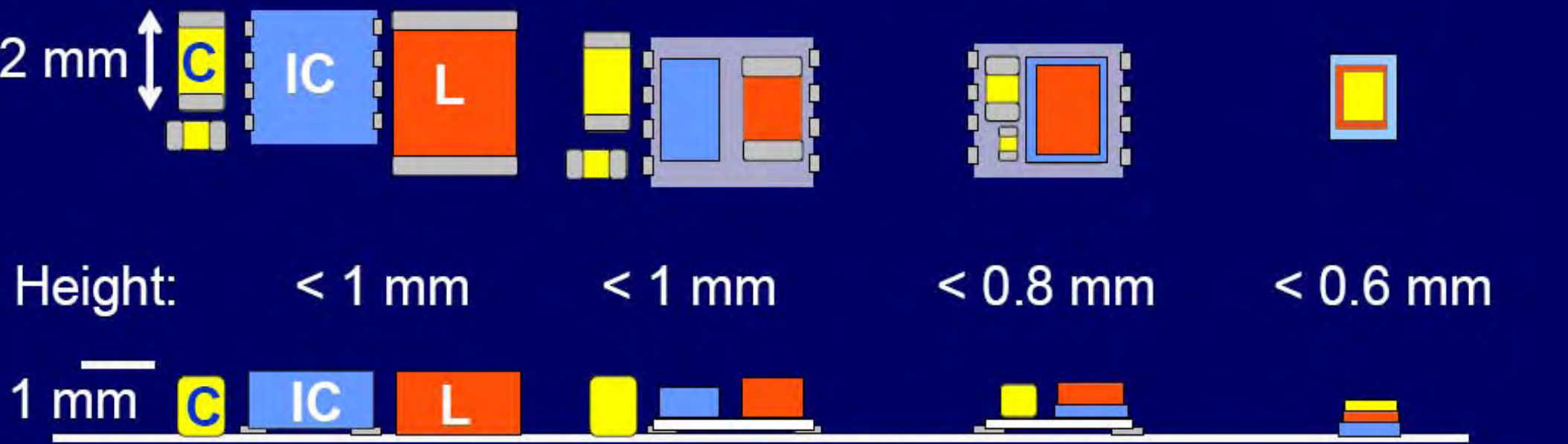
- Issues to be Addressed:
  - Miniaturisation of passives
    - Small Footprint, Low Profile
  - Cost effective production process
    - Compatibility with High Volume Silicon Manufacturing

Tyndall National Institute

Evolution to PwrSoC

Passive Component Size Reduction with Increasing Frequency Enables Functional Integration

Frequency: 2 MHz → 8 MHz → > 20 MHz → ~50MHz+



Height: < 1 mm | < 1 mm | < 0.8 mm | < 0.6 mm

Discrete components on PCB

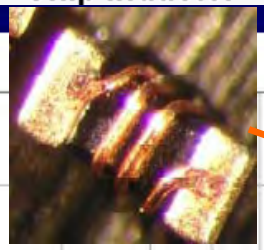
Co-packaged IC + L

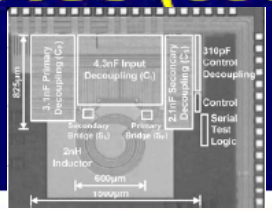
Stacked IC + L Co-packaged C

Chip Scale Package

Multi-MHz Switched-Mode Converters on System ICs (350nm to 90nm)

Off-chip Air-Core Chip Inductor





Novel Multi-Phase Topology
2nH Coupled Inductor
Air-Core

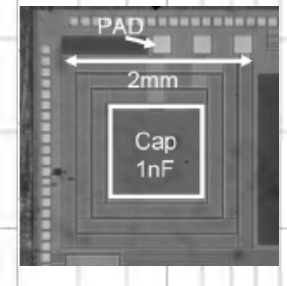
- Intel 2004
- U Minnesota 2008
- KU Leuven 2008
- U Tokyo 2007
- Freescale 2006
- U Brit Columbia 2007
- NXP 2008
- ST Microelectronics 2008

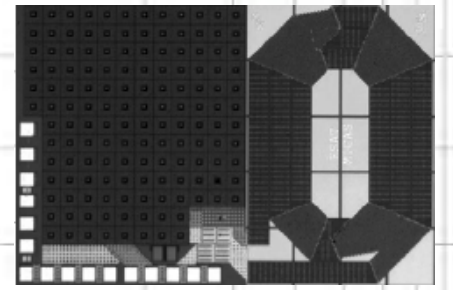
Efficiency %

100
90
80
70
60
50
40
30
20
10
0

10
100
1000
10000

Switching Frequency (MHz)



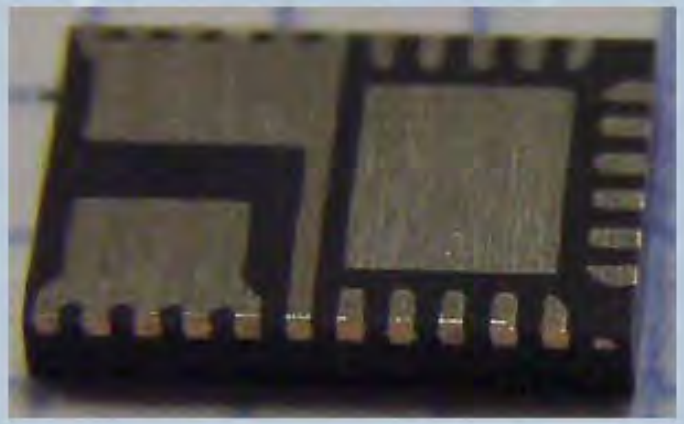


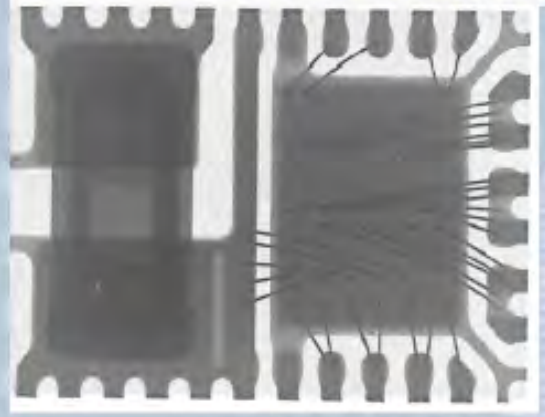
On-chip
Air-core Inductor

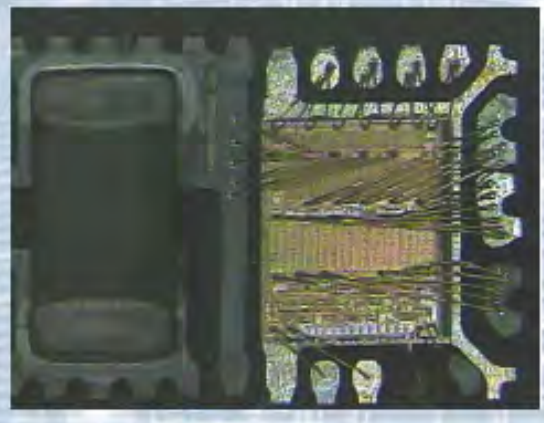
PSiP - Power Supply in Package
Paving the way to PwrSoC?

Power ASIC + Inductor on Leadframe

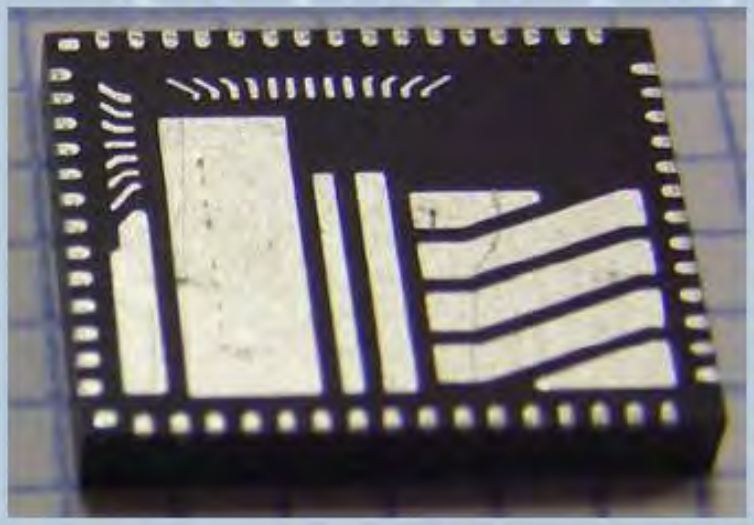
6 x 4 x 0.85mm

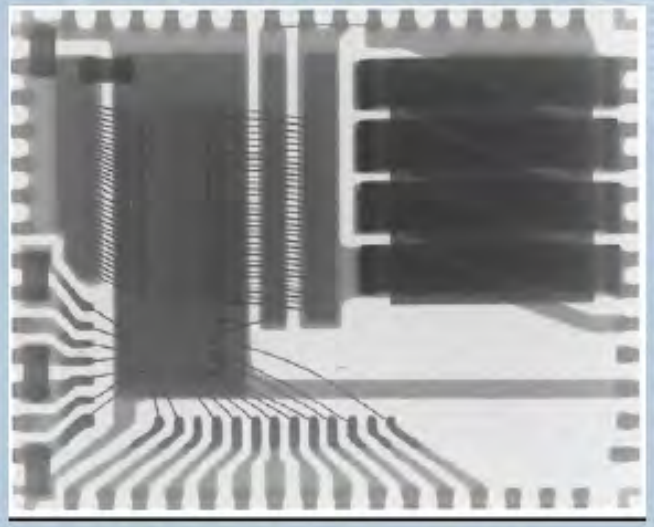


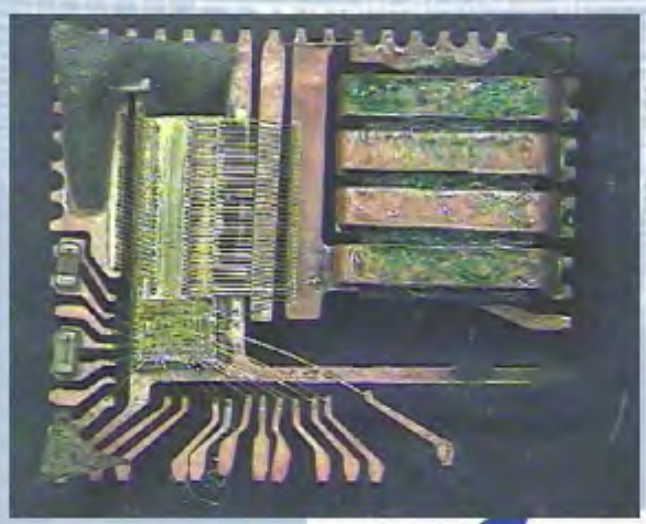




12 x 10 x 1.85mm



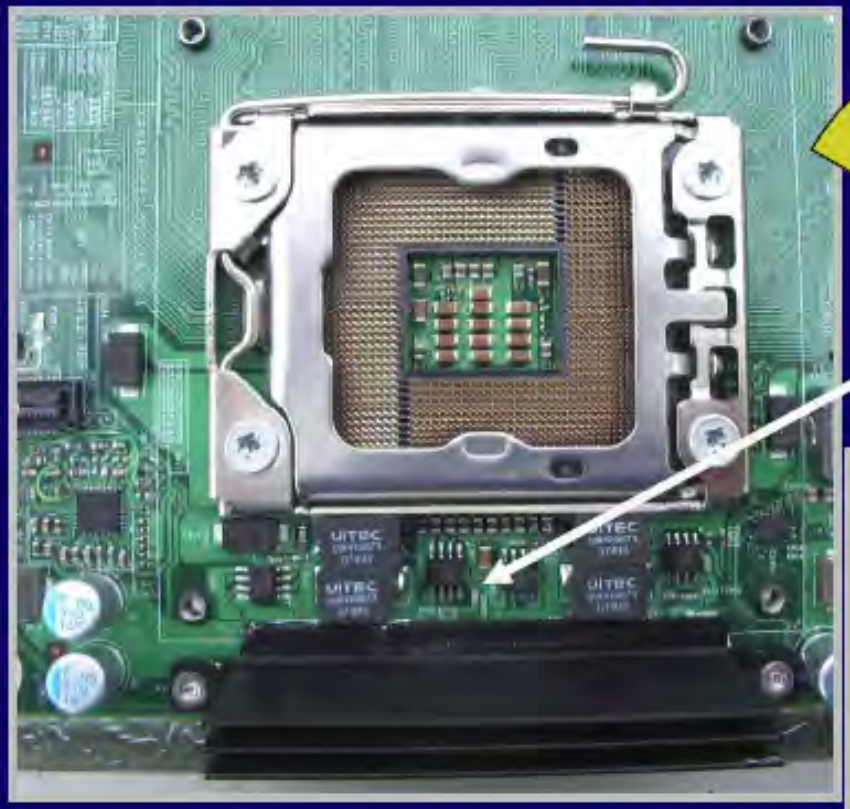




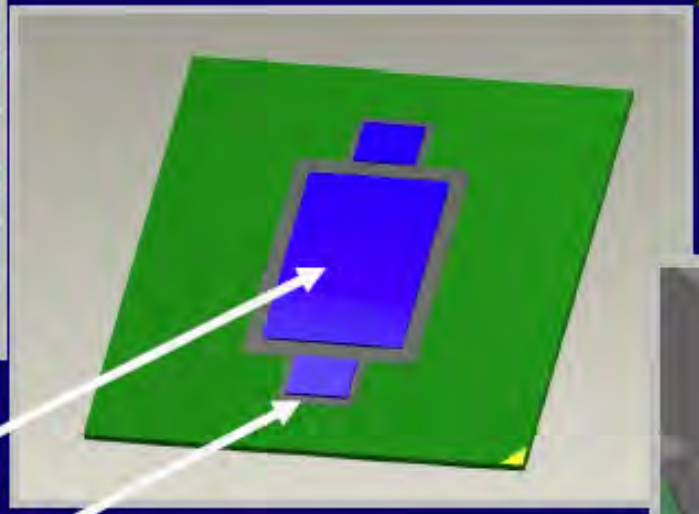
Source: PSMA PSIP2PwrSoC Phase 2 Study

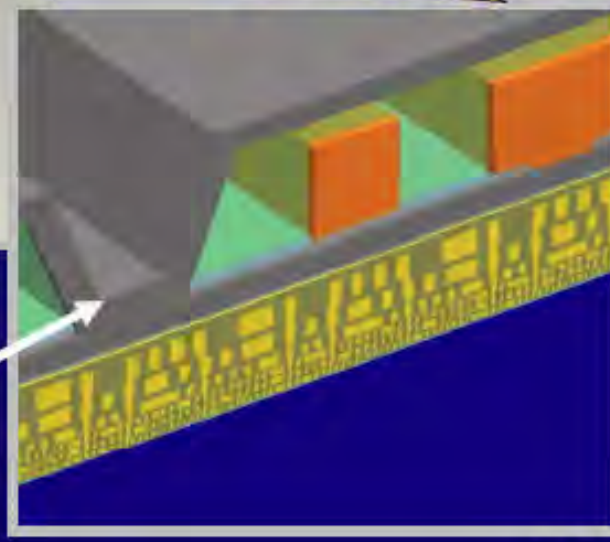
Power Sources Manufacturers Association

Evolution of Technologies for Functional Integration of PwrSoC with Microprocessor



MBVR region



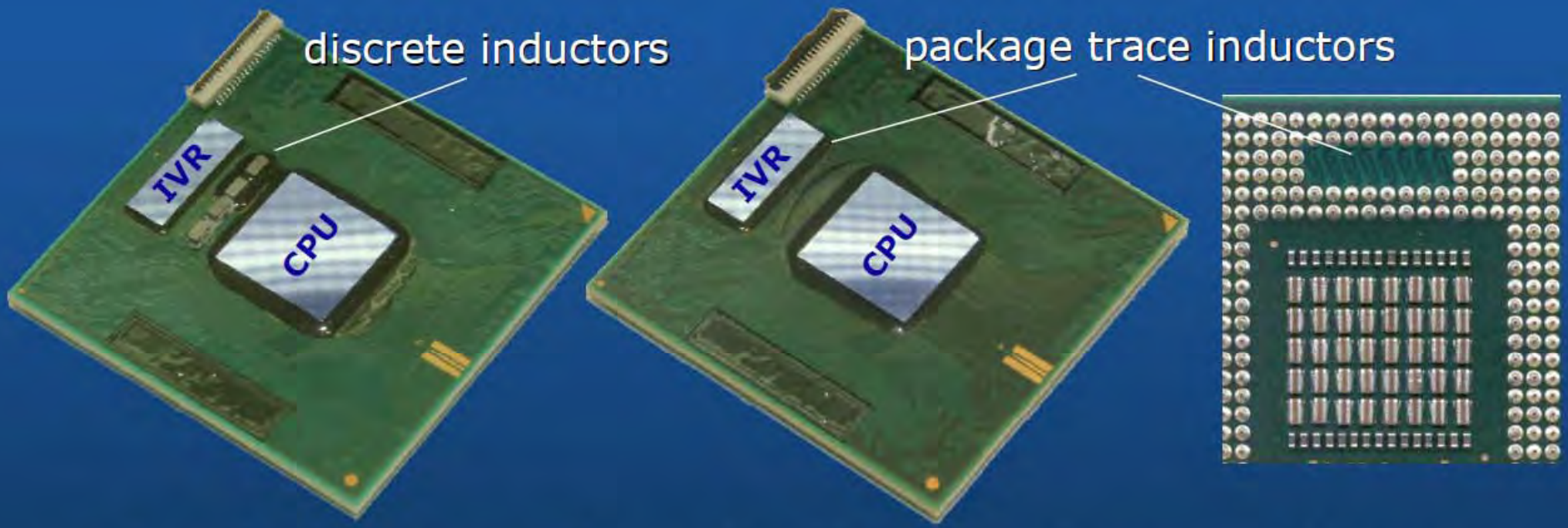


Microprocessor die on package

Power SOC Device next to die

Monolithic PowerSOC Integrated with Microprocessor

Package-Integrated VR with Intel® Core™2 Duo Processor



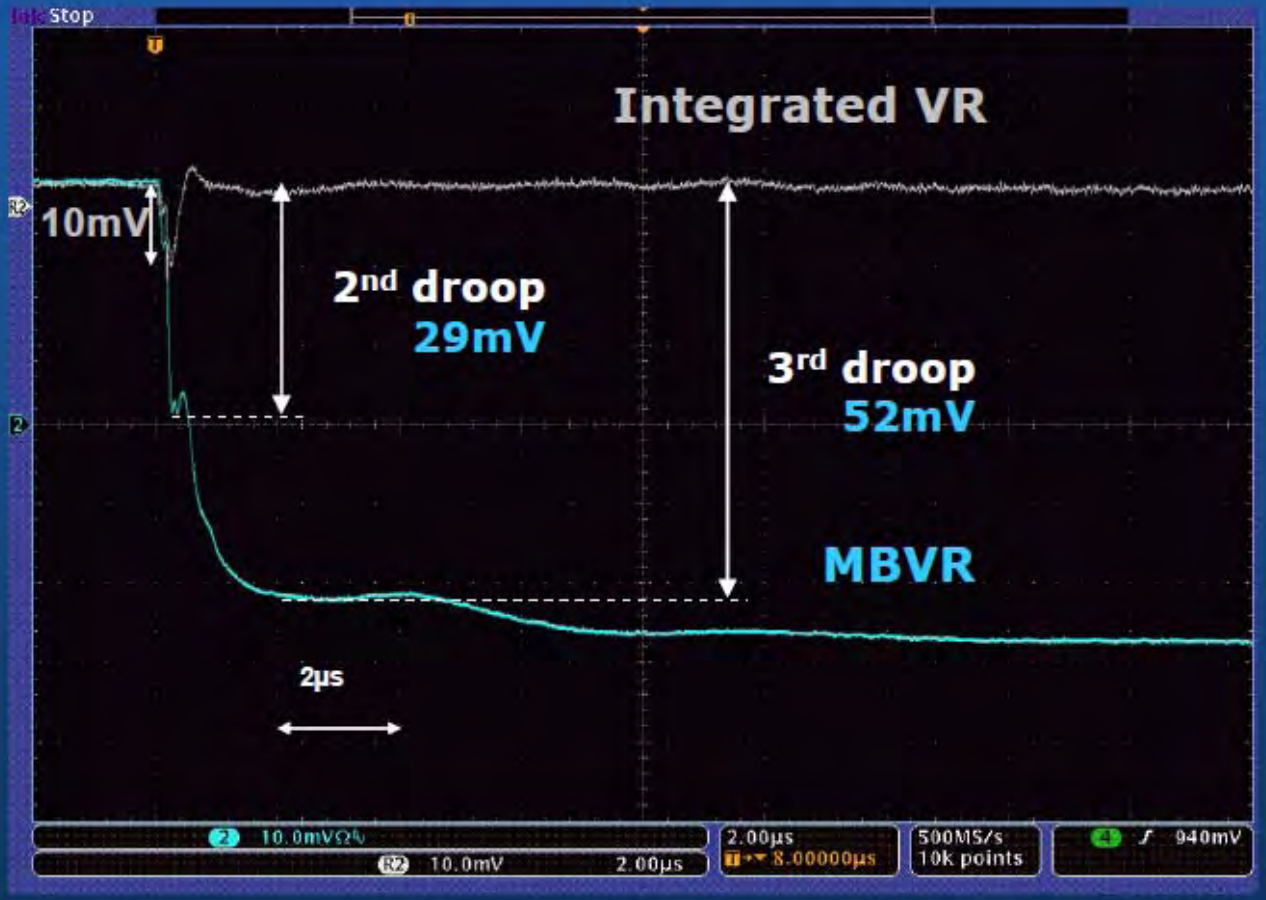
- Vin=3.3V, Vout=0...1.6V (VID), 10MHz...100MHz, TDC=50A / 75A peak, size=37.6mm², 130nm CMOS
- Inductors: 0508-size discrete powdered iron core or package-trace air core

APEC 2010 Special Session 1.4.2
A 60MHz 50W Fine-Grain Package Integrated VR Powering a CPU from 3.3V
G. Schrom, F. Faillet, J. Hahn, Intel, Santa Clara, CA

Package-Integrated VR Proof of Concept

- Advantage of on-package 2nd VR stage
  - Single 3.3V input, lower current going into the package
  - 2-stage conversion is more efficient
  - Near-load VR allows fast response, reduced load line
- VR test chip on the CPU package (MCP)
  - VR chip/w cascode bridges manufactured in 130nm CMOS
  - 60MHz switching frequency allows miniaturization
  - Mounted on modified CPU package/w package trace inductors or powdered-iron core inductors

Transient Performance



Load-line set to "0"

- 2nd droop: reduced to 10mV
- 3rd droop: eliminated
- Reduced load line saves power

結論

・エコ社会実現には既存インフラ・システムの変革が必要であり高耐圧ICが重要な役割を持つ。

・IT社会では多数の電源電圧があり、DCDC変換の効率向上が課題。