5th International Conference on Advanced Micro-Device Engineering (AMDE2013) 参加報告

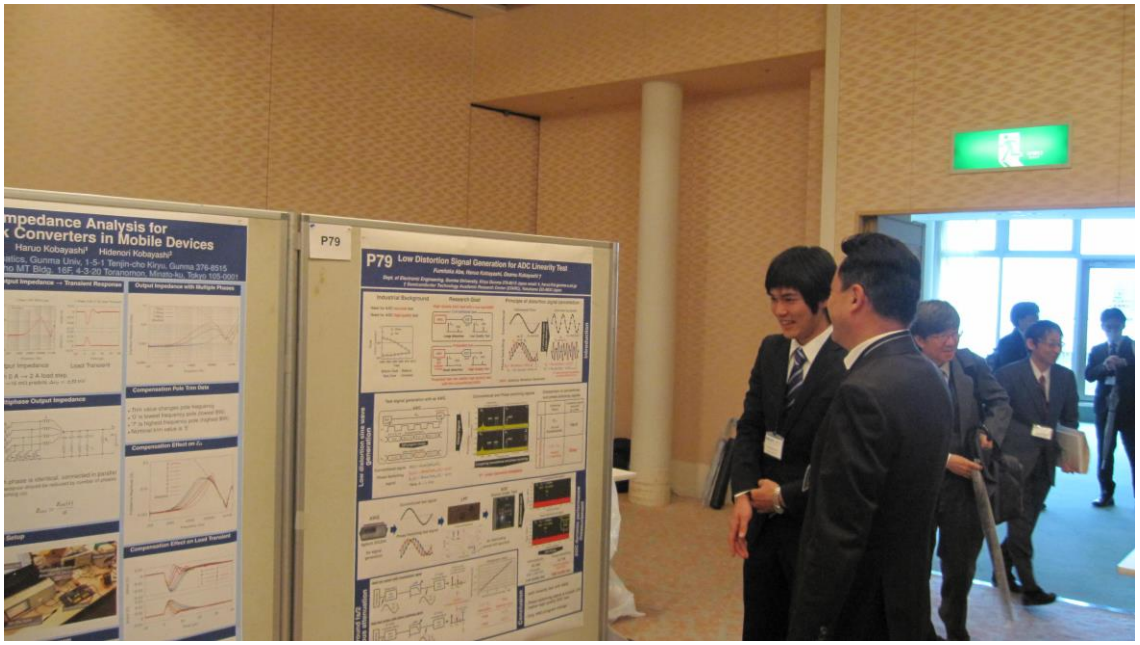
2013 年 12 月 19 日（木）に桐生市民文化会館で開催されました AMDE2013 にて
小林・高井研究室から 26 件（口頭発表 1 件（青木均客員教授）＋
ポスター発表 25 件（学生））の発表を行いました。

● 「研究成果を公表する」ことはアカデミズムの世界では重要である。
新しい知見・研究結果を公開・発表してはじめて意味をもち
成果として認められる。

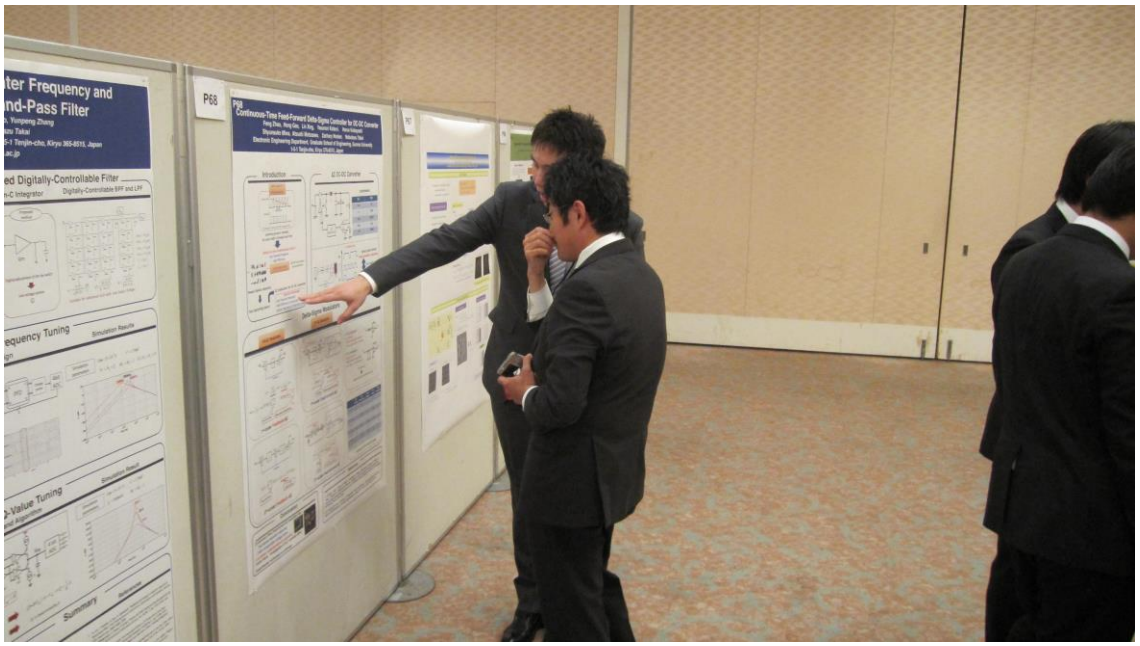
● 大学では学生を、研究を通して教育する。

大学の研究教育 （フンボルトの大学の理念）
「知識は 発展している、作り出されている、進歩している。
大学は 学問をいまだに完全には 解決されていない問題として、
たえず研究されつつあるものとして 扱うことに特色がある。」

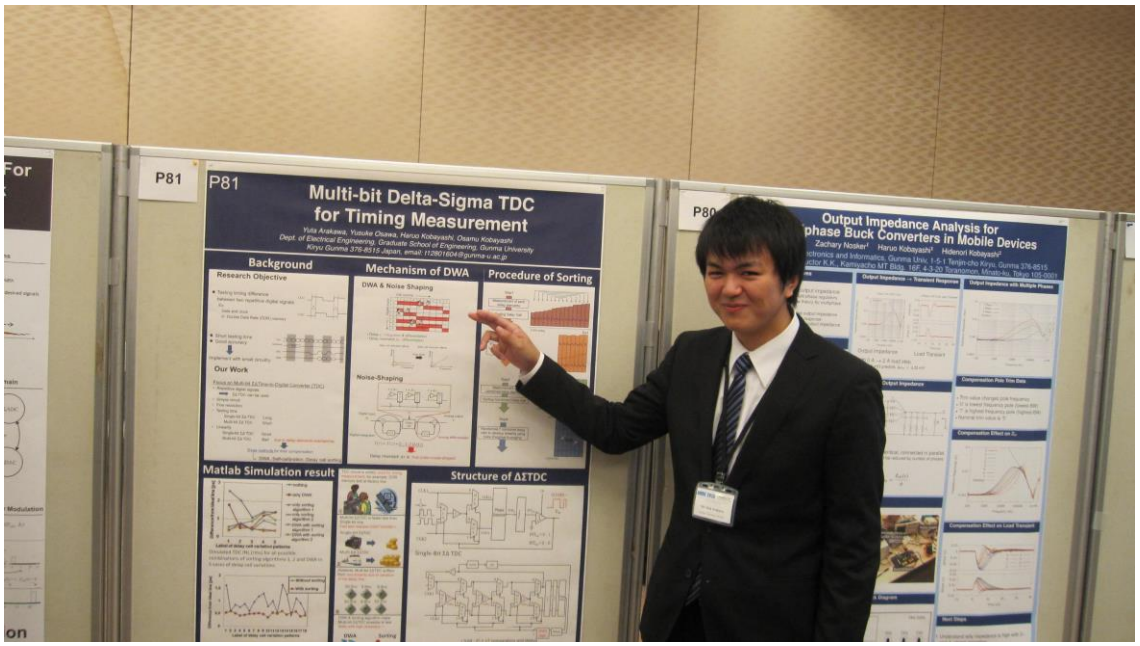
Conclusions
An accurate self-heat model only with equations is developed
The proposed model was implemented into BSIM4 model with Verilog-A language for LDMOS simulations
The proposed model has been verified with DC, transient, and small-signal S-parameter measurements
Because the self-heat model is based on general isothermal and thermal resistance theory, it can be applied for other device models
Since Verilog-A code itself is not so fast for circuit simulation, the proposed model will be converted to a C code model for practical use
28

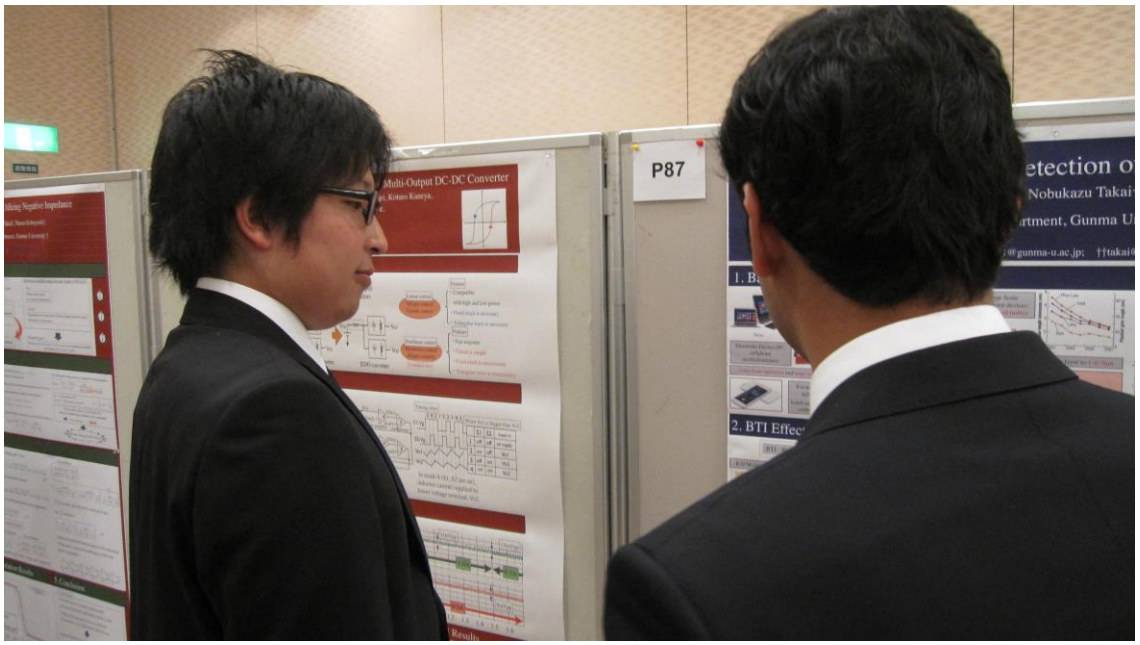

P79
P79 Low Distortion Signal Generation for ADC Linearity Test

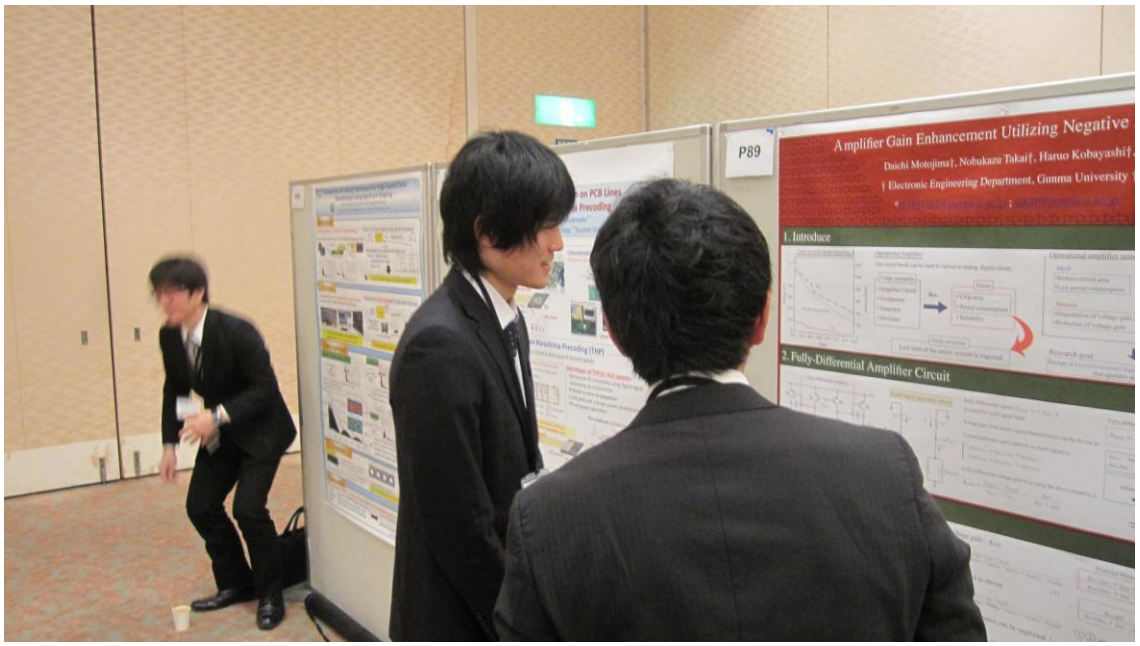
P89

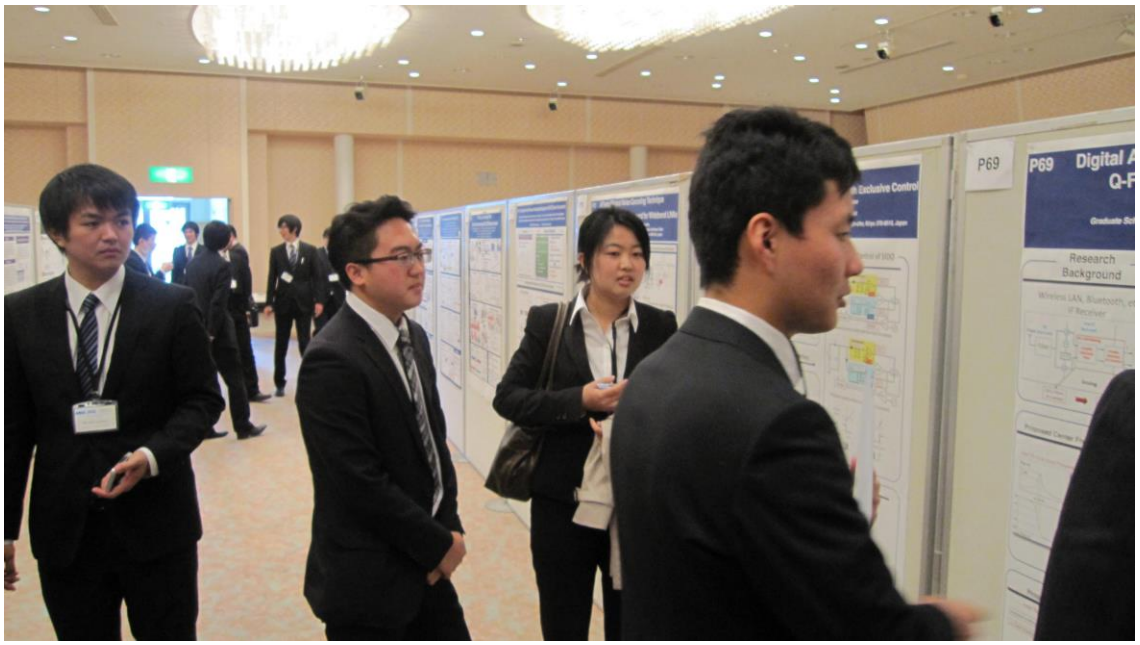

P68

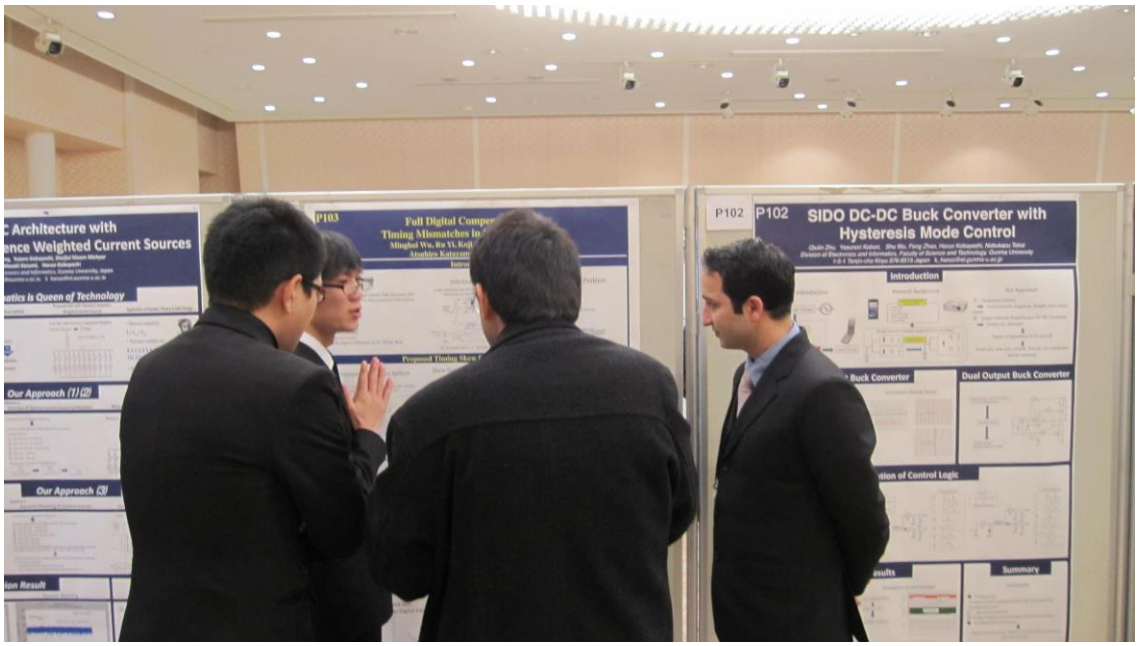
A study of new algorithm
current-steering DAC SFDR improvement
P72
P71

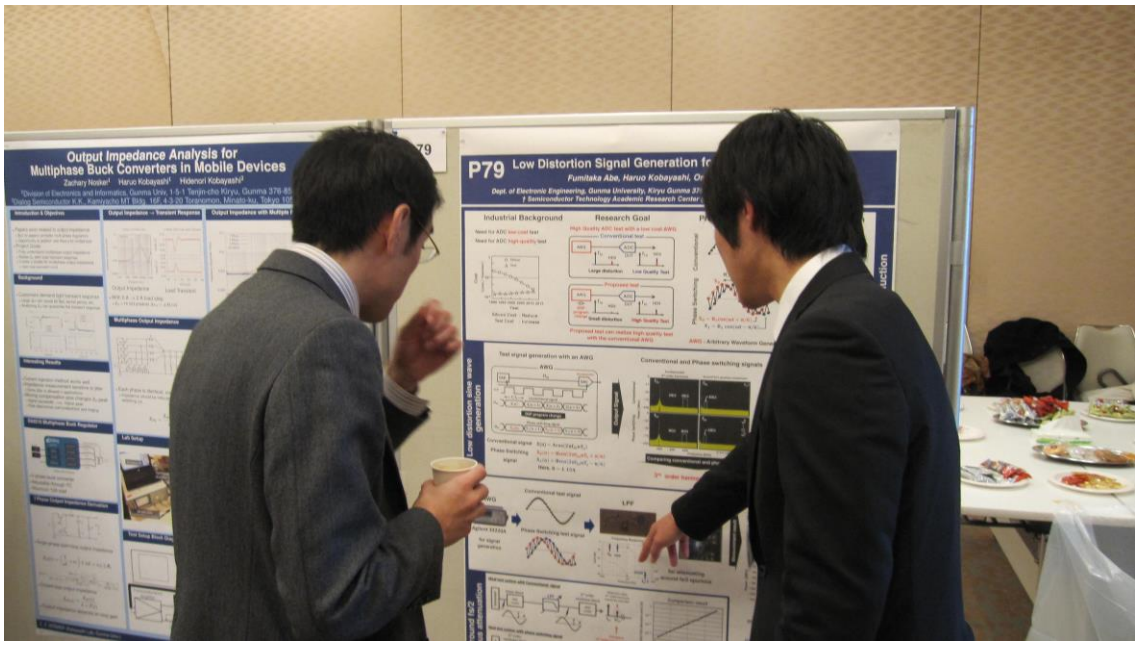

P81
Multi-bit Delta-Sigma TDC
for Timing Measurement
Background
Mechanism of DWA
Procedure of Sorting
Research Objective
Our Work
DWA & Noise Shaping
Noise-Shaping
Matlab Simulation result
Structure of ΔΣTDC
Output Impedance Analysis for
phase Buck Converters in Mobile Devices

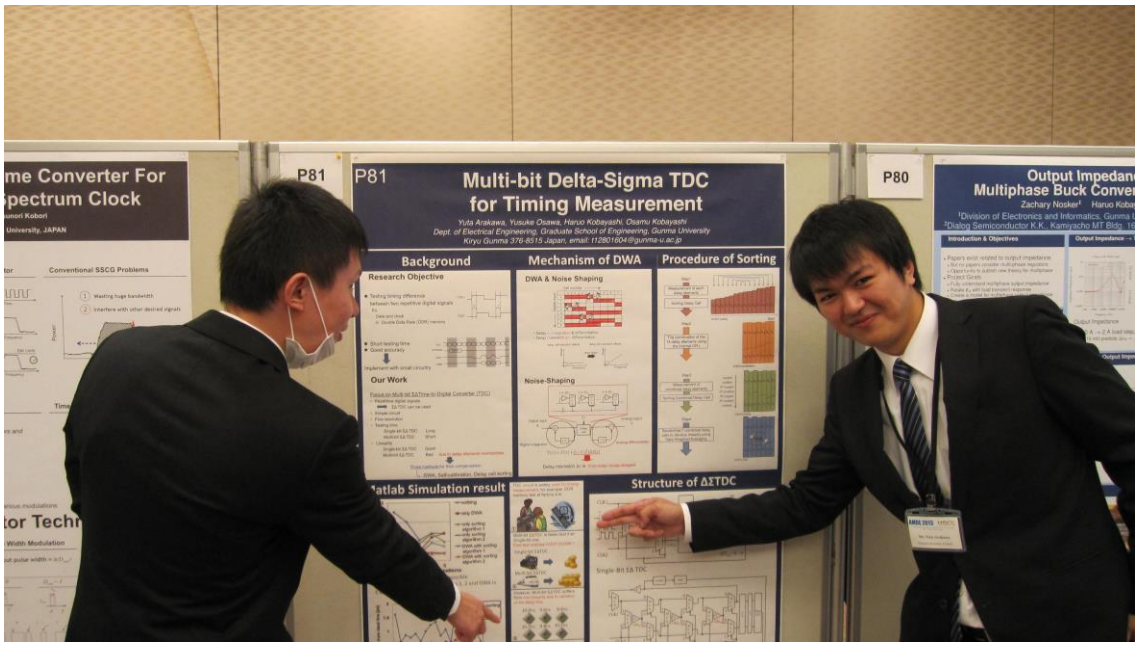

P87
Multi-Output DC-DC Converter


P89
Amplifier Gain Enhancement Utilizing Negative
1. Introduce
2. Fully-Differential Amplifier Circuit

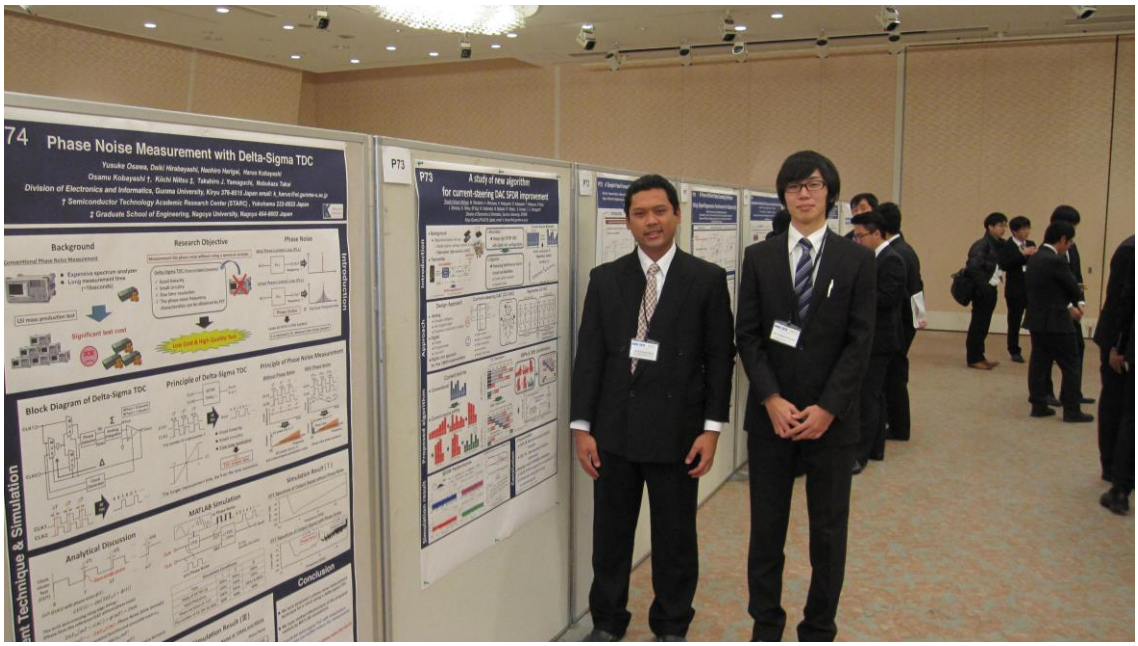

P69
Research
Background

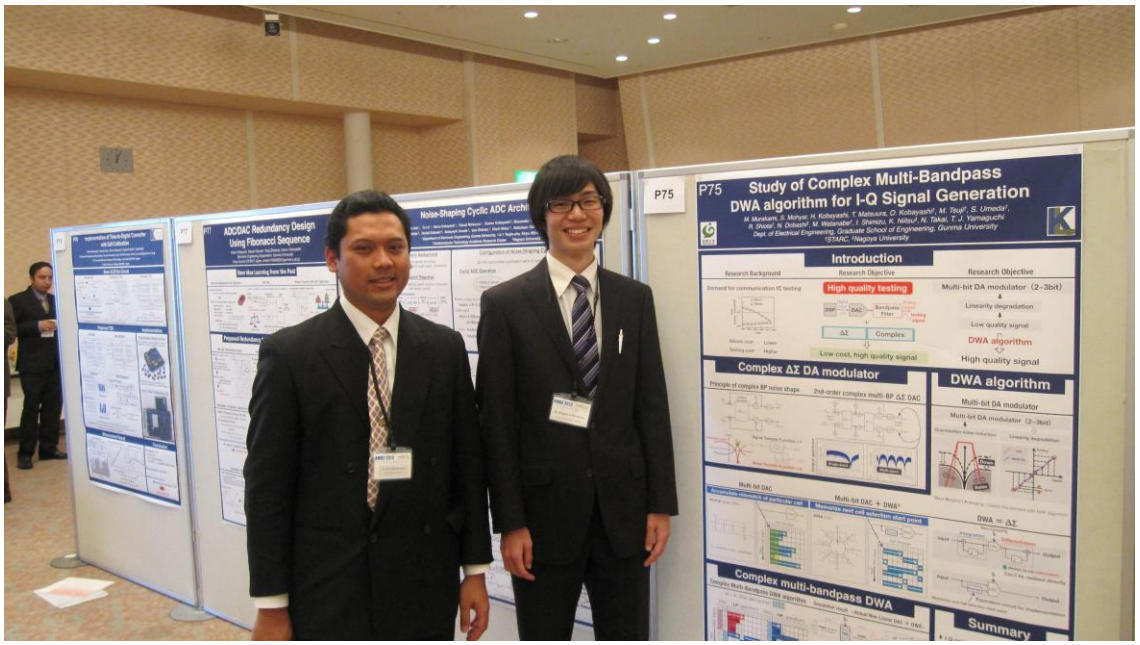

P102
SIDO DC-DC Buck Converter with
Hysteresis Mode Control
Introduction
Dual Output Buck Converter
Summary
Our Approach (1) (2)
Our Approach (3)


Output Impedance Analysis for
Multiphase Buck Converters in Mobile Devices
P79
Low Distortion Signal Generation fo
Industrial Background
Research Goal

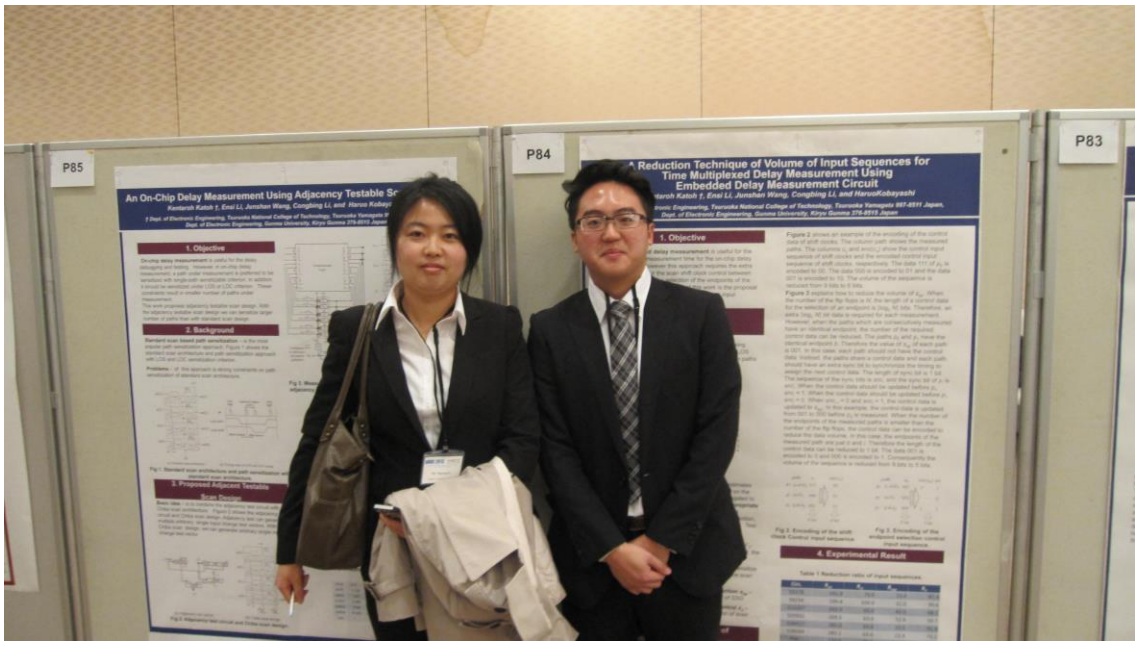

P81
Multi-bit Delta-Sigma TDC
for Timing Measurement
P80
Background
Mechanism of DWA
Procedure of Sorting
Research Objective
DWA & Noise Shaping
Our Work
Noise-Shaping
Structure of ΔΣTDC

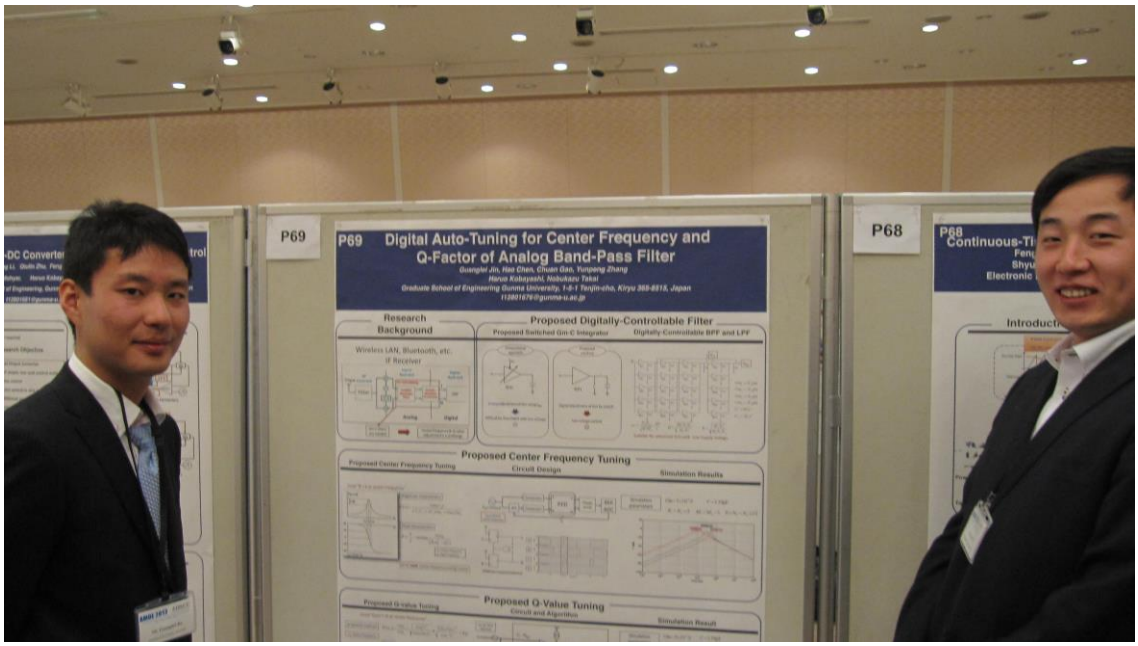
P77
ADC/DAC Redundancy Design
Using Fibonacci Sequence
New Idea Learning from the Past
P76
Noise-Shaping Cyclic
summary

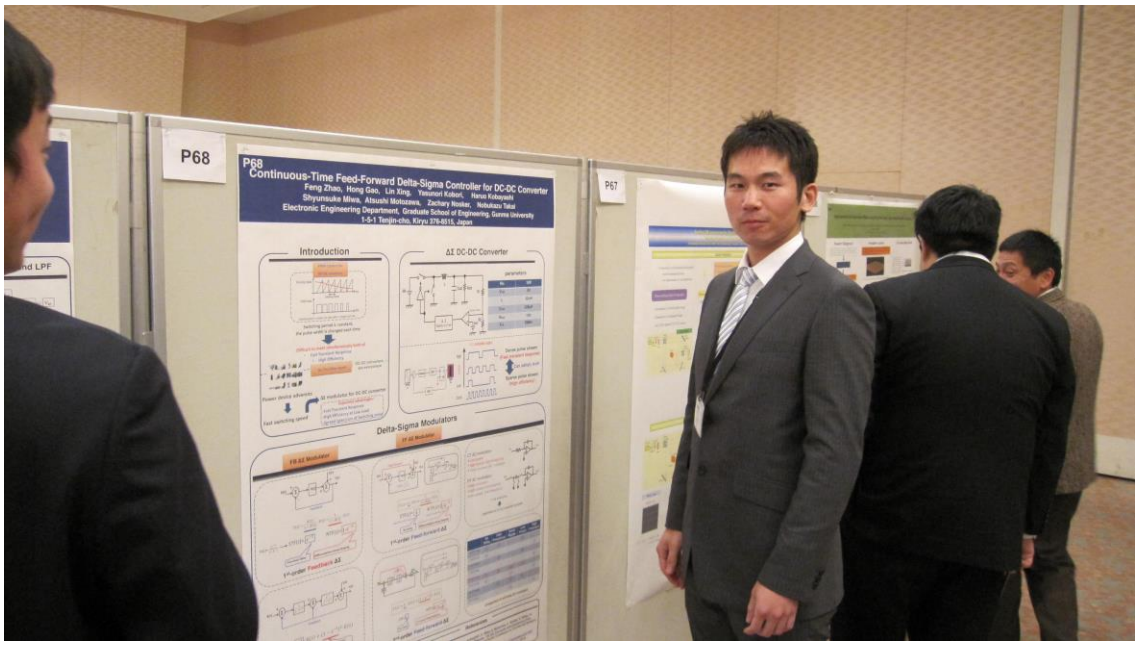

P74
Phase Noise Measurement with Delta-Sigma TDC
P73
A study of new algorithm
for current-steering DAC SFDR improvement


P75
Study of Complex Multi-Bandpass DWA algorithm for I-Q Signal Generation
Introduction
Research Background
Research Objective
Research Objective
High quality testing
Multi-bit DA modulator (2-3bit)
Linearity degradation
Low quality signal
DWA algorithm
High quality signal
Low cost, high quality signal
Complex ΔΣ DA modulator
DWA algorithm
Multi-bit DA modulator
Complex multi-bandpass DWA
Summary

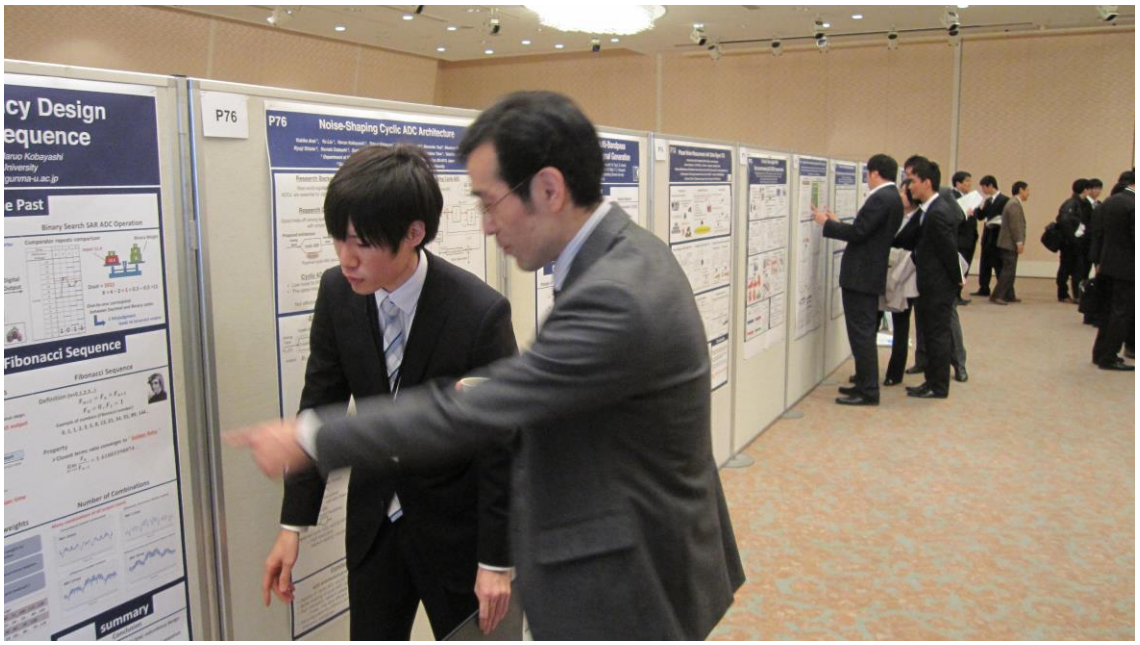
P86

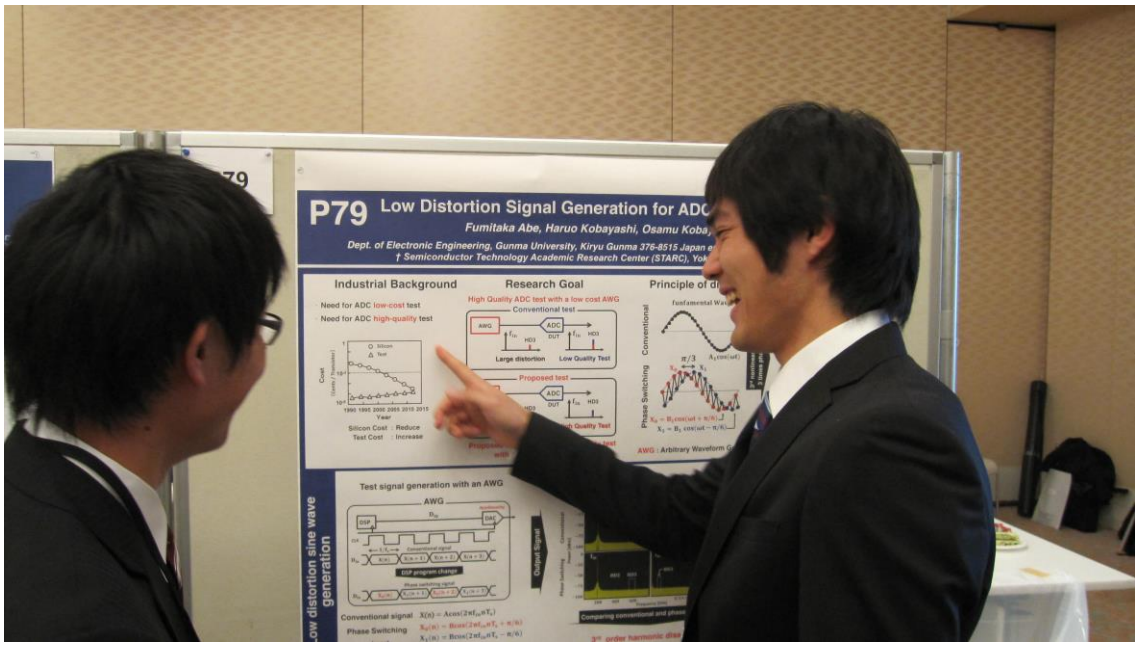

P85
An On-Chip Delay Measurement Using Adjacency Testable Sc
1. Objective
2. Background
3. Proposed Adjacent Testable Scan Design
P84
Reduction Technique of Volume of Input Sequences for Time Multiplexed Delay Measurement Using Embedded Delay Measurement Circuit
1. Objective
4. Experimental Result
P83


P69
P69 Digital Auto-Tuning for Center Frequency and Q-Factor of Analog Band-Pass Filter
Research Background
Wireless LAN, Bluetooth, etc.
IF Receiver
Proposed Digitally-Controllable Filter
Proposed Switched Gm-C Integrator
Digitally-Controllable BPF and LPF
Proposed Center Frequency Tuning
Proposed Center Frequency Tuning
Circuit Design
Simulation Results
Proposed Q-Value Tuning
Proposed Q-Value Tuning
Circuit and Algorithm
Simulation Result
P68
Introduction

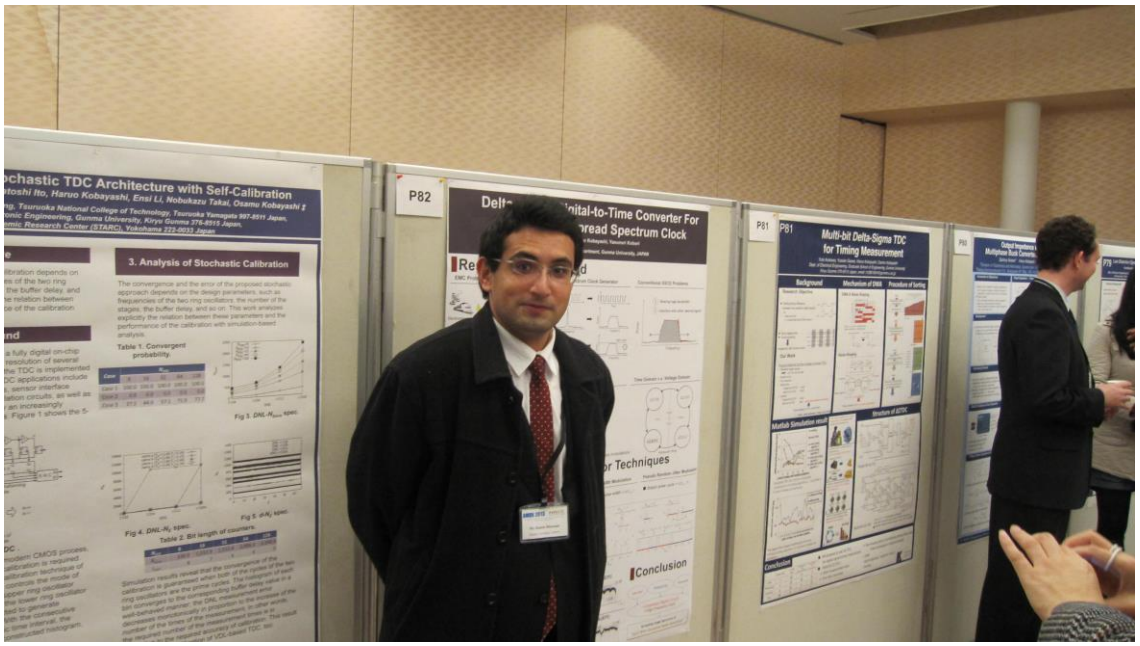

P68
P68
Continuous-Time Feed-Forward Delta-Sigma Controller for DC-DC Converter
Introduction
ΔΣ DC-DC Converter
Delta-Sigma Modulators
P67

P86
Automatic Synthe
Using Genetic Algorithm

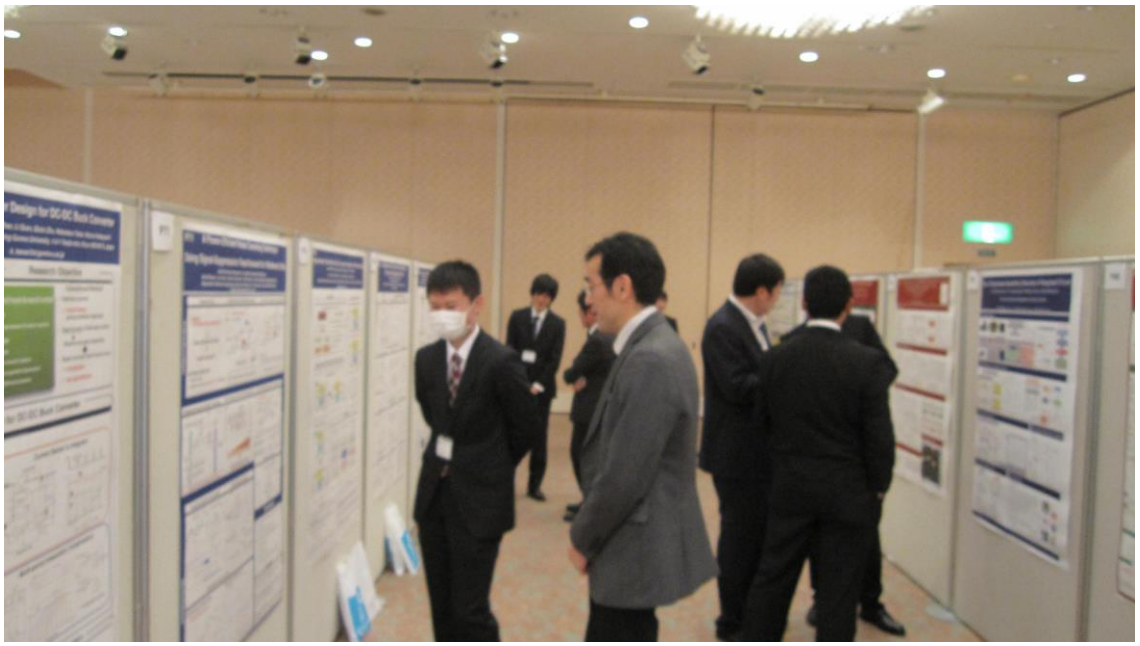

P76
P76 Noise-Shaping Cyclic ADC Architecture
Past
Fibonacci Sequence
summary

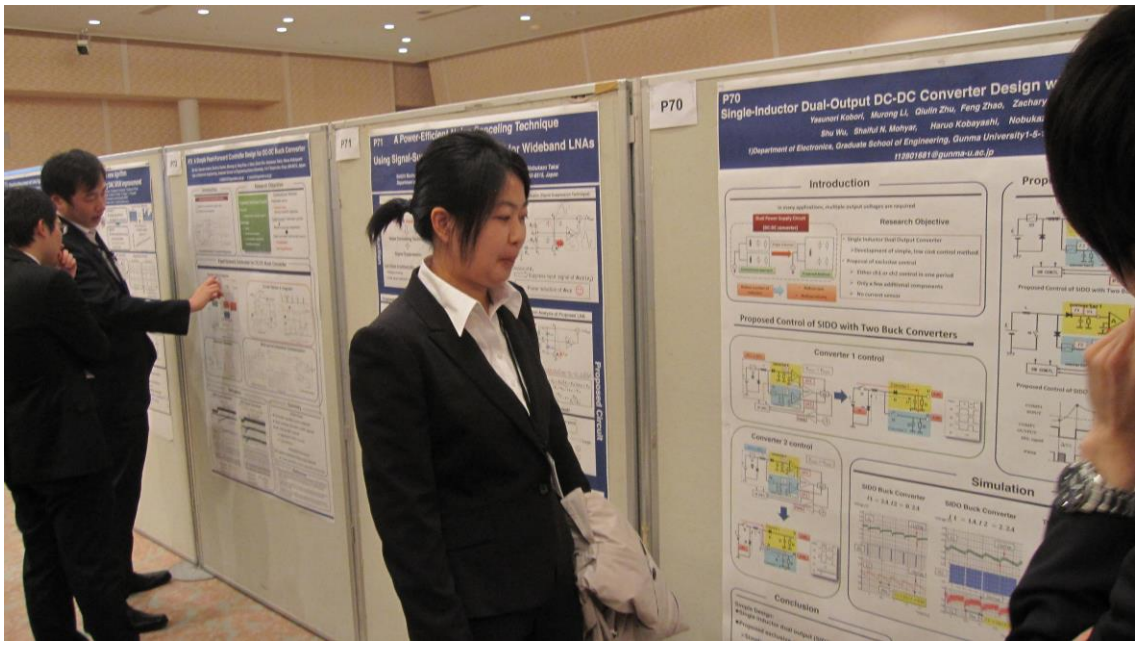

P79 Low Distortion Signal Generation for ADC
Industrial Background
Research Goal
Principle of
Need for ADC low-cost test
Need for ADC high-quality test
High Quality ADC test with a low cost AWG
Conventional test
Large distortion
Low Quality Test
Proposed test
Test signal generation with an AWG
AWG
Low distortion sine wave generation

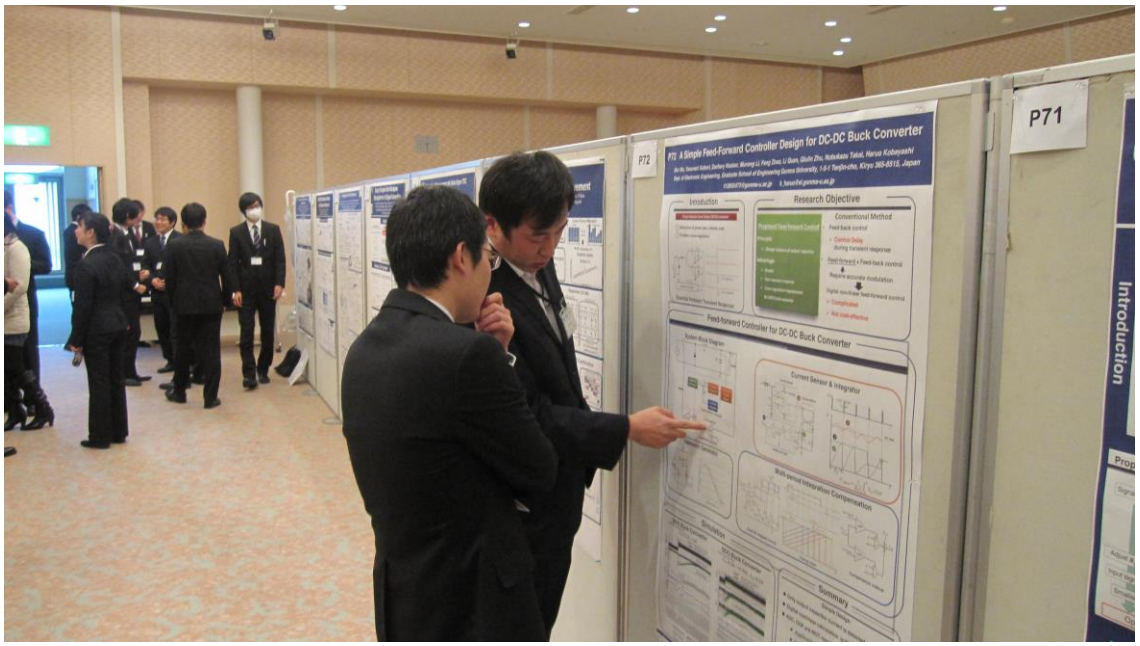
P81
Background

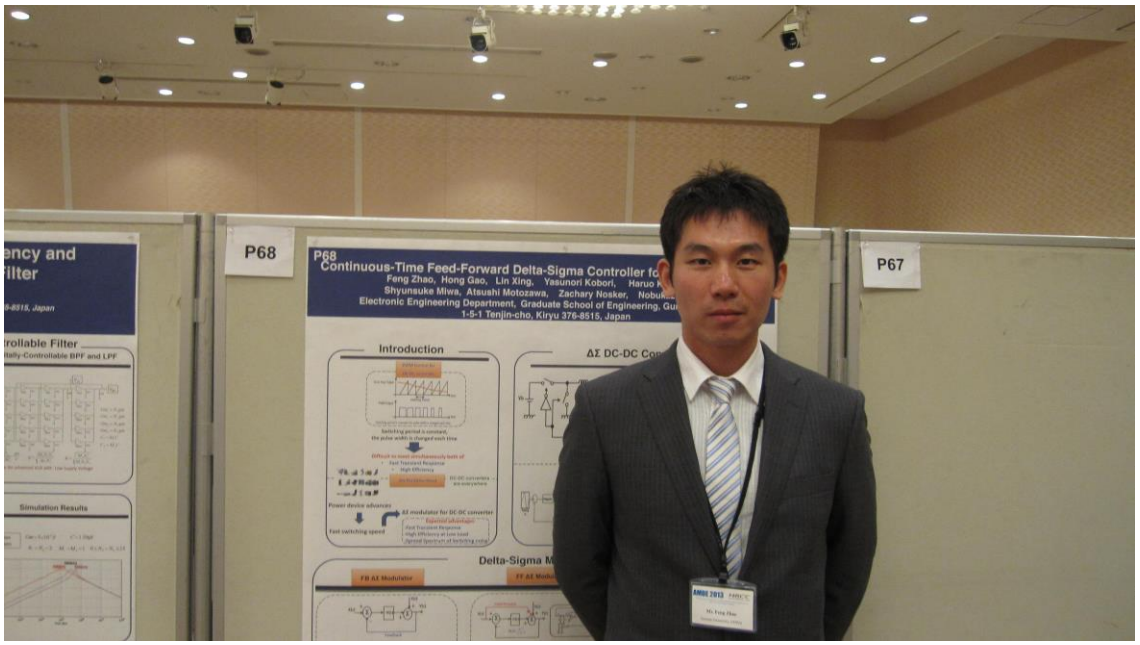

P82
P81
Multi-bit Delta-Sigma TDC
for Timing Measurement
Background
Mechanism of DWA
Procedure of Sorting
Matlab Simulation result
Conclusion
3. Analysis of Stochastic Calibration

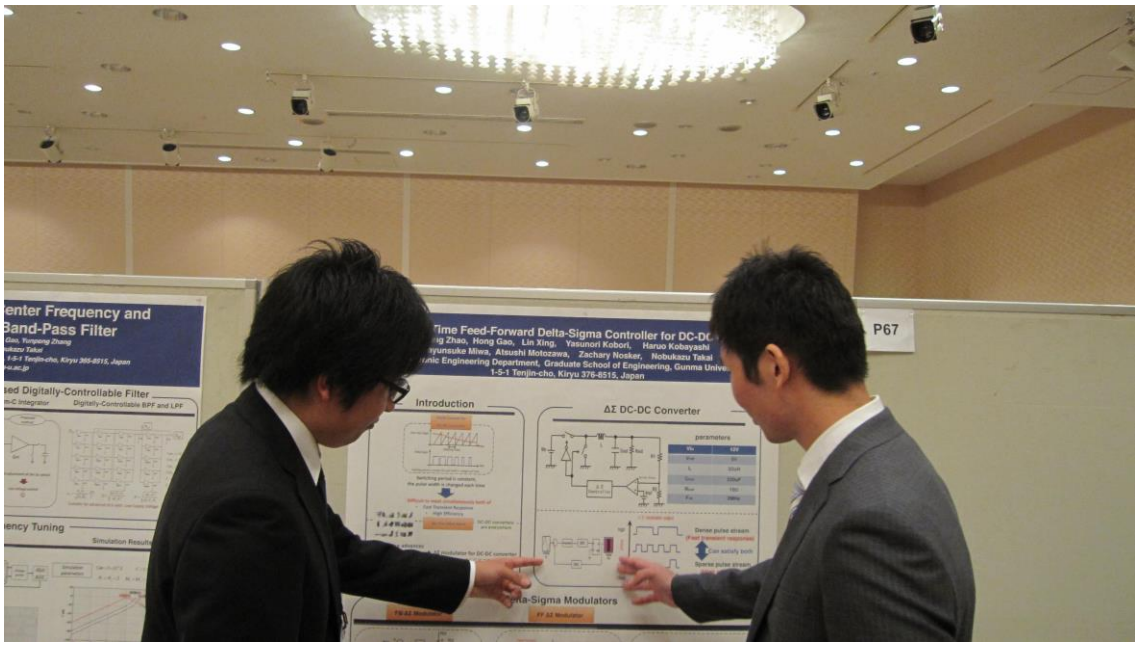
P81
Multi-bit Delta-Sigma TDC
for Timing Measurement
Background
Mechanism of DWA
Structure of ΔΣTDC

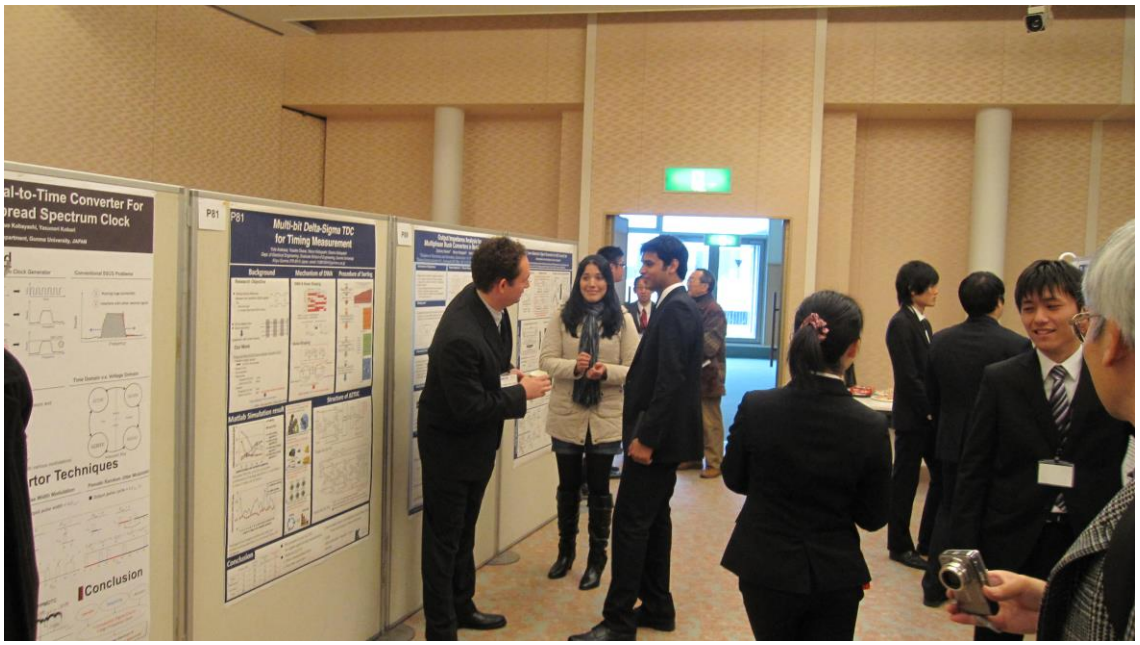


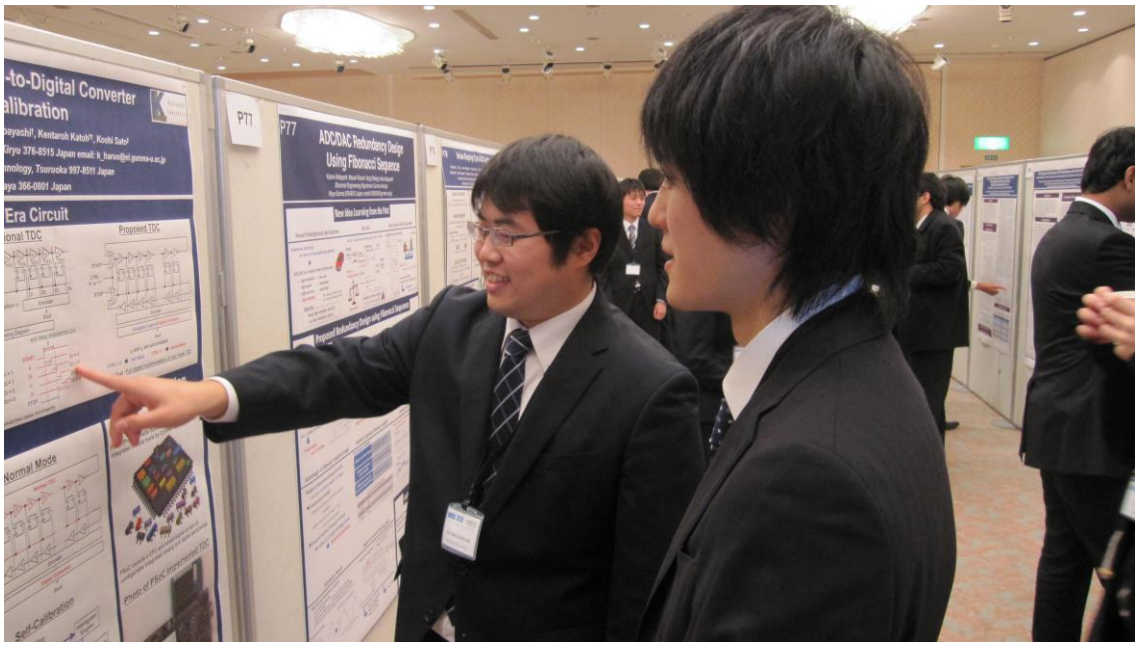

P70
Single-Inductor Dual-Output DC-DC Converter Design w
Introduction
Research Objective
Proposed Control of SIDO with Two Buck Converters
Converter 1 control
Converter 2 control
Simulation
Conclusion
P71
Wideband LNAs
Proposed Circuit


P71
P72
A Single Feed-Forward Controller Design for DC-DC Buck Converter
Introduction
Research Objective
Conventional Method
Feed-forward Controller for DC-DC Buck Converter
Current Sensor & Integrator
Main control Interaction Compensation
Simulation
Summary
Introduction

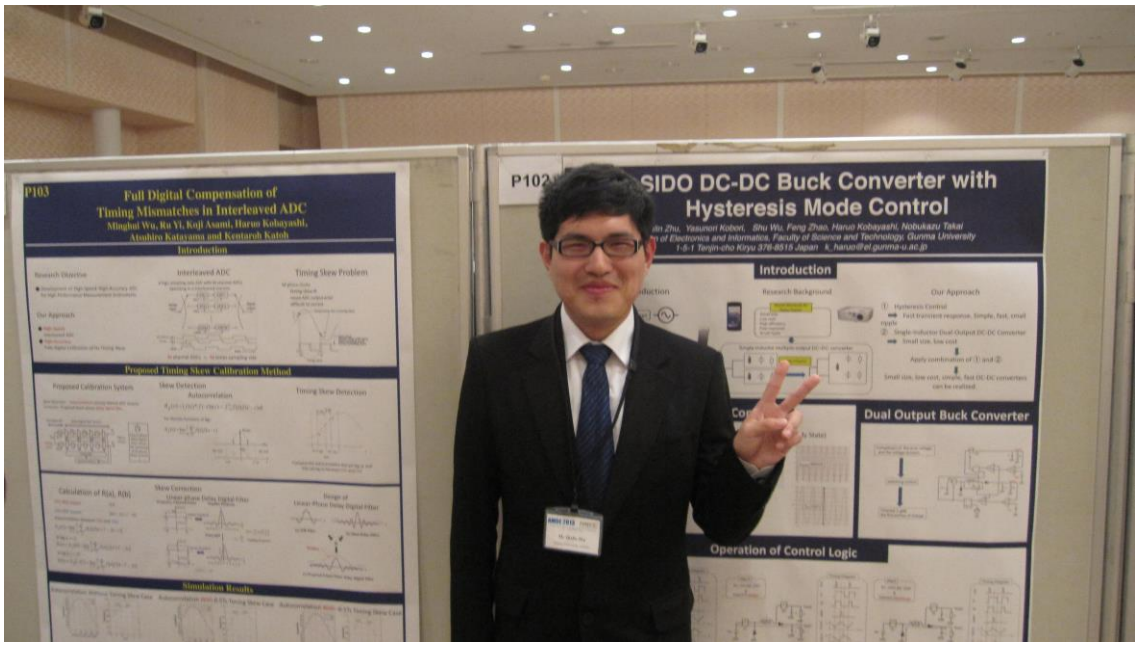

P68
P67
Introduction
ΔΣ DC-DC Converter

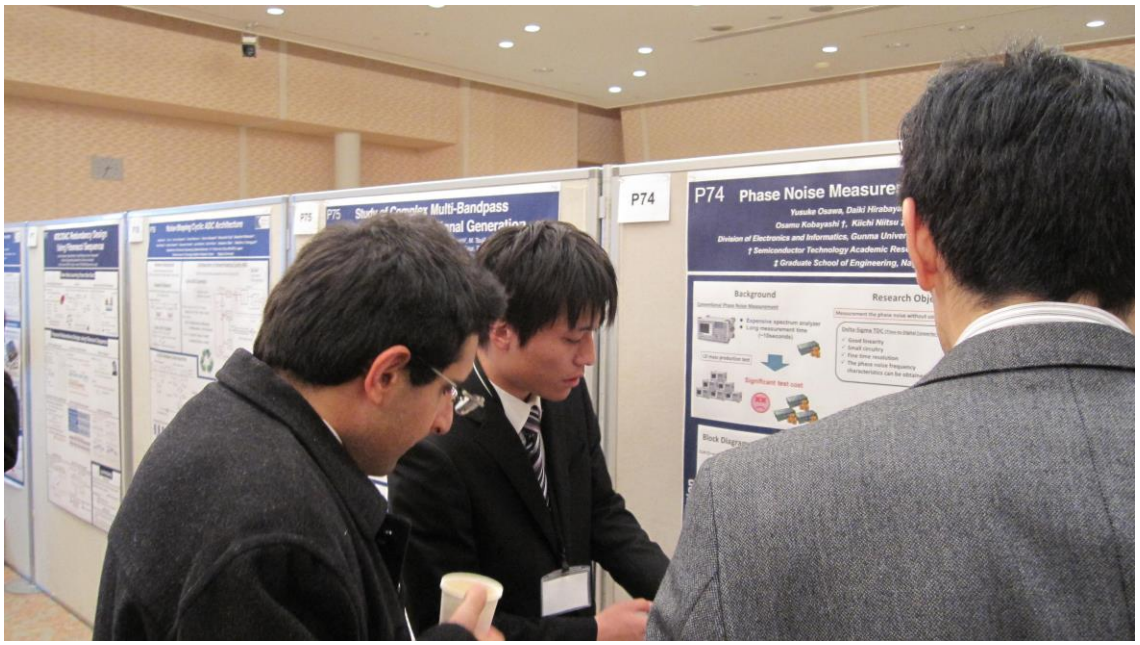

P67
Introduction
ΔΣ DC-DC Converter


P81
Multi-bit Delta-Sigma TDC
for Timing Measurement
Background
Conclusion

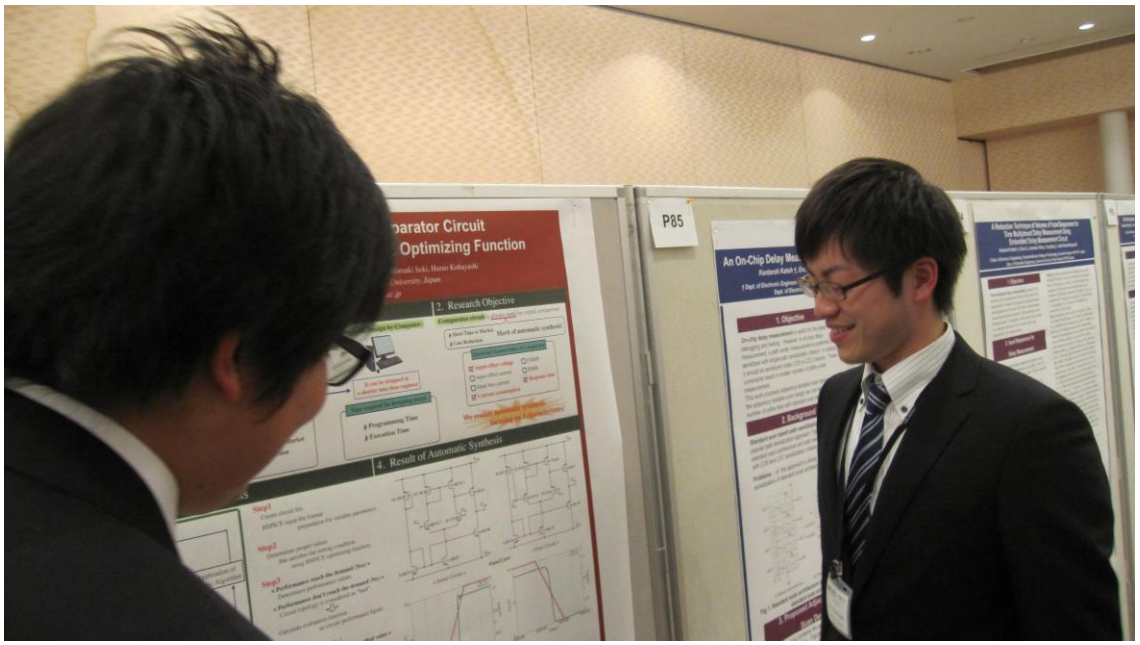

P77
ADC/DAC Redundancy Design
Using Fibonacci Sequence
Era Circuit
Normal Mode

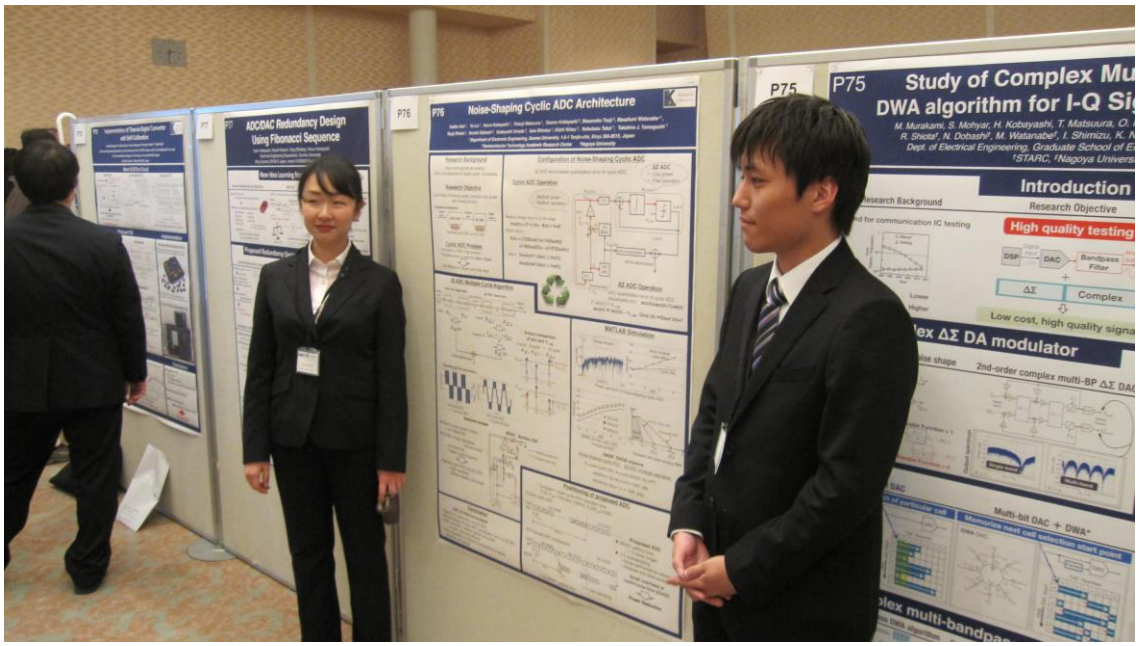
P104
DAC Architecture with
Fibonacci Sequence Weighted Current
Mathematics is Queen of Technology
Our Approach (1) (2)
P103
Introduction

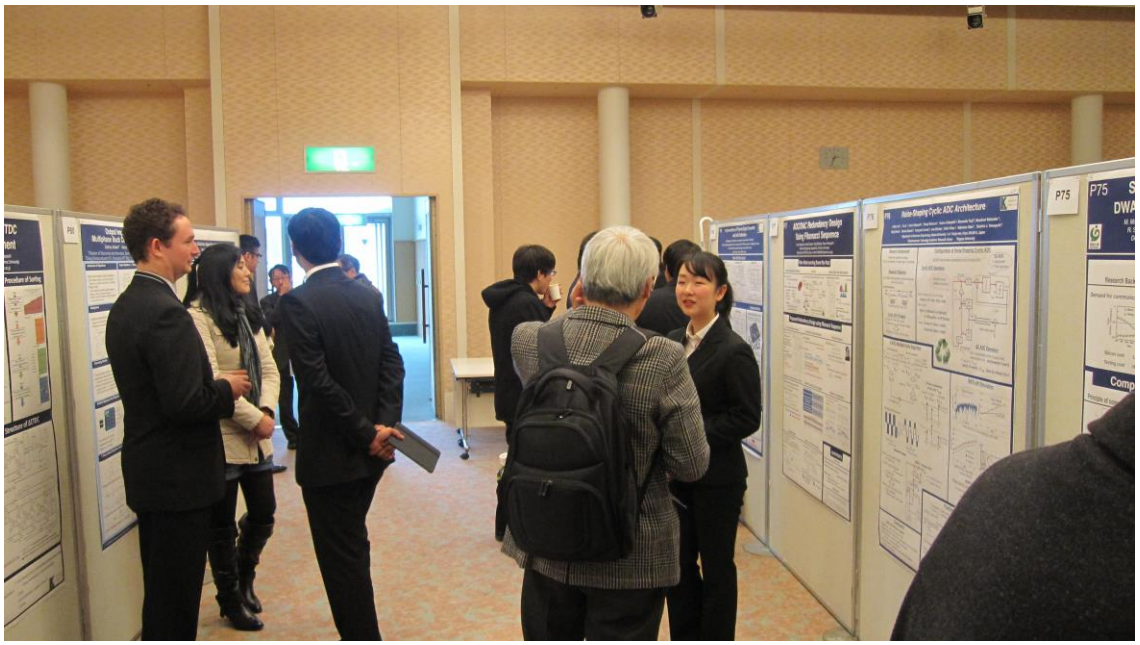

P103
Full Digital Compensation of
Timing Mismatches in Interleaved ADC
Introduction
Proposed Timing Skew Calibration Method
Simulation Results
SIDO DC-DC Buck Converter with
Hysteresis Mode Control
Introduction
Dual Output Buck Converter
Operation of Control Logic

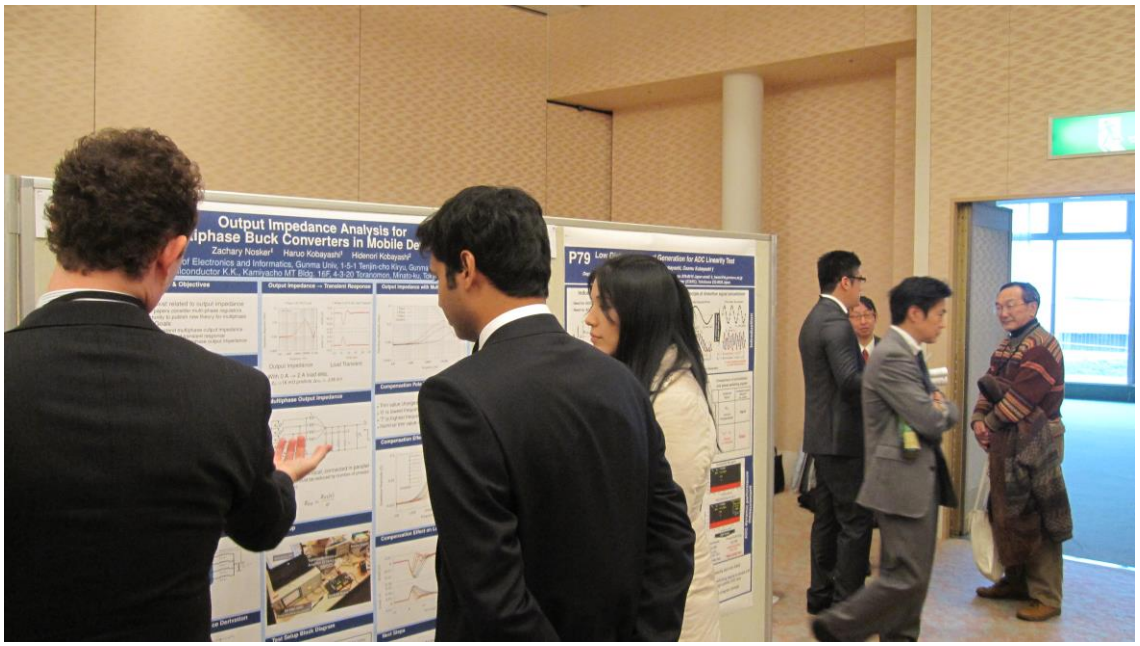

P74
Background
Research Obj

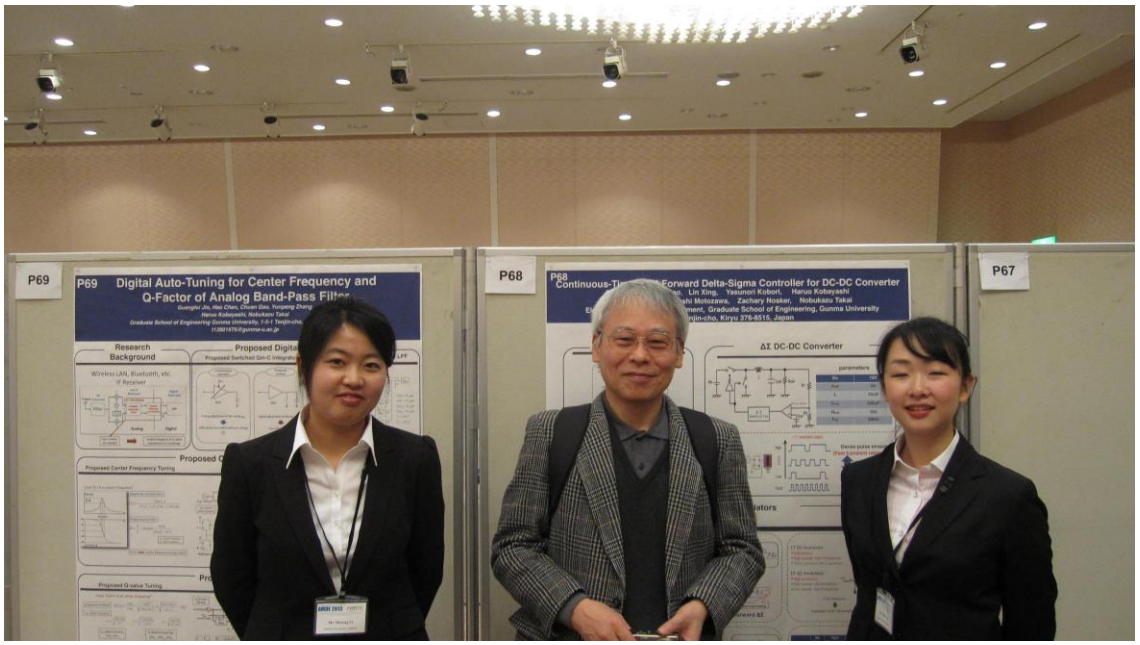
P74
Phase Noise Measurement with
Background
Block Diagram of Delta-Sigma TDC

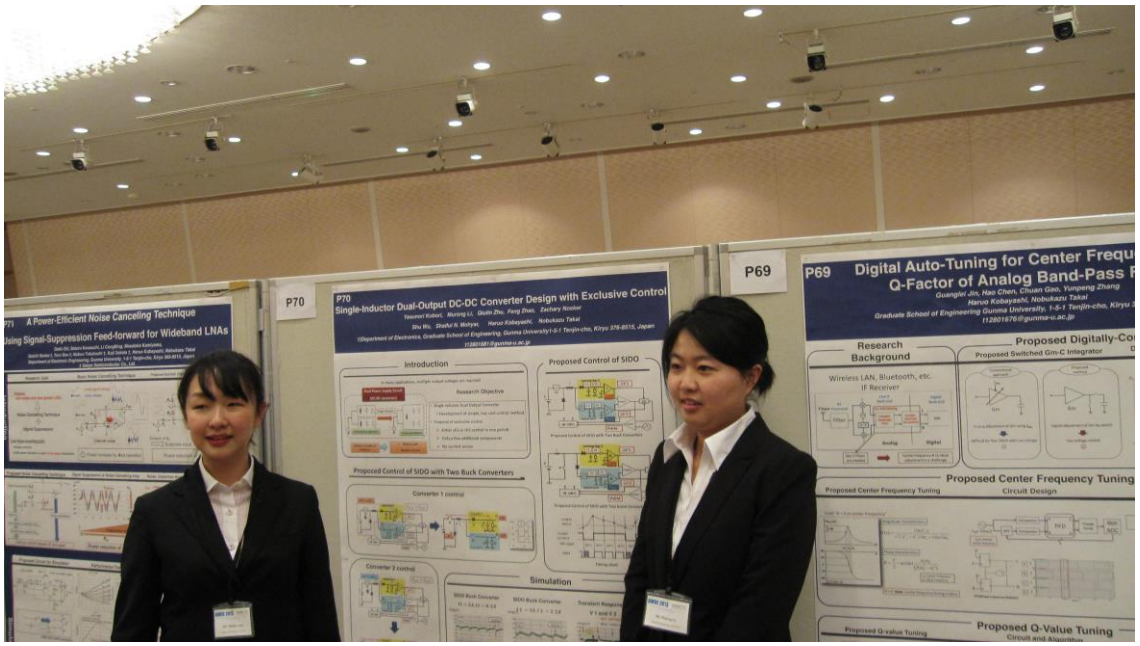

P85
Optimizing Function
2. Research Objective
4. Result of Automatic Synthesis


P75
Study of Complex Mu
DWA algorithm for I-Q Si
Introduction
Research Objective
High quality testing
Low cost, high quality signa
ex ΔΣ DA modulator
2nd-order complex multi-BP ΔΣ DA
Multi-bit DAC + DWA*
P76
Noise-Shaping Cyclic ADC Architecture
P77
ADC/DAC Redundancy Design
Using Fibonacci Sequence


P75


Output Impedance Analysis for
Zachary Noske
Haruo Kobayashi
Hidenori Kobayashi
P79


P69
Digital Auto-Tuning for Center Frequency and
Q-Factor of Analog Band-Pass Filter
Research Background
Wireless LAN, Bluetooth, etc.
IF Receiver
P68
ΔΣ DC-DC Converter
P67


P70
Single-Inductor Dual-Output DC-DC Converter Design with Exclusive Control
Introduction
Proposed Control of SIDO
Proposed Control of SIDO with Two Buck Converters
Simulation
P69
Digital Auto-Tuning for Center Frequ
Q-Factor of Analog Band-Pass
Research Background
Wireless LAN, Bluetooth, etc.
IF Receiver
Proposed Digitally-Co
Proposed Switched Gm-C Integrator
Proposed Center Frequency Tuning
Proposed Center Frequency Tuning
Circuit Design
Proposed Q-Value Tuning

5th International Conference on Advanced Micro-Device Engineering (AMDE2013) Kiryu, Japan (Dec. 19, 2013)

小林・高井研究室からの26件の発表

[1] L09 “A New Self-heat Modeling Approach for LDMOS Devices”
Hitoshi Aoki and Haruo Kobayashi (Gunma University, Japan)

[2] P68 Continuous-Time Feed-Forward Delta-Sigma Controller for DC-DC Converter
Feng Zhao, Hong Gao, Lin Xing, Yasunori Kobori, Haruo Kobayashi,Shyunsuke Miwa, Atsushi Motozawa, Zachary Nosker, Nobukazu Takai (Gunma University, Japan)

[3] P69 Digital Auto-Tuning for Center Frequency and Q-Factor of Analog Band-Pass Filter
Guanglei Jin, Hao Chen, Chuan Gao, Yunpeng Zhang, Haruo Kobayashi, Nobukazu Takai (Gunma University, Japan)

[4] P70 Single-Inductor Dual-Output DC-DC Converter Design with Exclusive Control Design with Exclusive Control
Yasunori Kobori, **Murong Li**, Qiulin Zhu, Feng Zhao, Zachary Nosker, Shu Wu, Shaiful N. Mohyar, Haruo Kobayashi, Nobukazu Takai (Gunma University, Japan)

[5] P71 A Power-Efficient Noise Canceling Technique Using Signal-Suppression Feed-forward for Wideband LNAs

Daiki Oki, Satoru Kawauchi, Li CongBing, Masataka Kamiyama, Seiichi Banba, Toru Dan, Nobuo Takahashi, Koji Sakata, Haruo Kobayashi, Nobukazu Takai
(Gunma University, Sanyo Semiconductor, Japan)

[6] P72 A Simple Feed-Forward Controller Design for DC-DC Buck Converter

Shu Wu, Yasunori Kobori, Zachary Nosker, Murong Li, Feng Zhao, Li Quan, Qiulin Zhu, Nobukazu Takai, Haruo Kobayashi (Gunma University, Japan)

[7] P73 New Digital Algorithm for Current-Steering DAC SFDR Improvement for Communication Application

S. N. Mohyar, M.Murakami, H.Kobayashi, O.Kobayashi, T.Matsuura, N.Takai, I.Shimizu, M.Tsuji, M.Watanabe, N.Dobashi, R.Shiota, S.Umeda, T.Yamaguchi (Gunma University, Semiconductor Technology Academic Research Center (STARC), Japan)

[8] P74 Phase Noise Measurement with Delta-Sigma TDC

Yusuke Osawa, Daiki Hirabayashi, Naohiro Harigai, Haruo Kobayashi, Osamu Kobayashi, Kiichi Niitsu, Takahiro J. Yamaguchi, Nobukazu Takai Gunma
(University, Semiconductor Technology Academic Research Center (STARC), Nagoya University, Japan)

[9] P75 Study of Complex Multi-Bandpass DWA algorithm for I-Q Signal Generation

Masahiro Murakami, Shaiful Nizam Mohyar, Haruo Kobayashi, Tatsuji Matsuura, Osamu Kobayashi, Masanobu Tsuji, Sadayoshi Umeda, Ryoji Shiota, Noriaki Dobashi, Masafumi Watanabe, Isao Shimizu, Kiichi Niitsu, Nobukazu Takai, Takahiro J. Yamaguchi (Gunma University, Semiconductor Technology Academic Research Center (STARC), Nagoya University, Japan)

[10] P76 Noise-Shaping Cyclic ADC Architecture

Yukiko Arai, Yu Liu, Haruo Kobayashi, Tatsuji Matsuura, Osamu Kobayashi, Masanobu Tsuji, Masafumi Watanabe, Ryoji Shiota, Noriaki Dobashi, Sadayoshi Umeda, Isao Shimizu, Kiichi Niitsu, Nobukazu Takai, Takahiro J. Yamaguchi (Gunma University, Semiconductor Technology Academic Research Center (STARC), Nagoya University, Japan)

[11] P77 ADC/DAC Redundancy Design Using Fibonacci Sequence

Yutaro Kobayashi, Masaki Kazumi, Yang Zhixiang, Haruo Kobayashi Gunma University, Japan

[12] P78 Implementation of Time-to-Digital Converter with Self-Calibration
Daiki Hirabayashi, Takeshi Chujo, Haruo Kobayashi, Kentaroh Katoh, Koshi Sato (Gunma University, Hikari Science, Japan)

[13] P79 Low Distortion Signal Generation for ADC Linearity Testing
Fumitaka Abe, Haruo Kobayashi, Osamu Kobayashi
(Gunma University, Semiconductor Technology Academic Research Center (STARC), Japan)

[14] P80 Output Impedance Analysis for Multiphase Buck Converters in Mobile Devices
Zachary Nosker, Haruo Kobayashi and Hidenori Kobayashi
(Gunma University, Dialog Semiconductor, Japan)

[15] P81 Multi-bit Delta-Sigma TDC for Timing Measurement
Yuta Arakawa, Yusuke Oosawa, Haruo Kobayashi, Osamu Kobayashi (Gunma University, Semiconductor Technology Academic Research Center (STARC), Japan)

[16] P82 Delta-Sigma Digital-to-Time Converter For Band-Select Spread Spectrum Clock
Ramin Khatami, Haruo Kobayashi, Yasunori Kobori (Gunma University, Japan)

[17] P83 An Analysis of Stochastic TDC architecture with Self-Calibration
Kentaroh Katoh, **Junshan Wang**,Yuta Doi, Satoshi Ito, Haruo Kobayashi, Ensi Li, Nobukazu Takai and Osamu Kobayashi (Tsuruoka National College of Technology, Gunma University, Semiconductor Technology Academic Research Center (STARC), Japan)

[18] P84 A Reduction Technique of Volume of Input Sequences for Time-Multiplexed Delay Measurement Using Embedded Delay Measurement Circuit
Kentaroh Katoh, Ensi Li, Junshan Wang, Congbing Li and Haruo Kobayashi
Tsuruoka National College of Technology, Gunma University, Japan

[19] P85 An On-Chip Delay Measurement Using Adjacency Testable Scan Design
Kentaroh Katoh, Ensi Li, Junshan Wang, Congbing Li and Haruo Kobayashi
Tsuruoka National College of Technology, Gunma University, Japan

[20] P86 Automatic Synthesis of Comparator Circuit Using Genetic Algorithm and SPICE Optimizing Function **Takayuki Negishi**, Naoki Arai, Nobukazu Takai, Masato Kato, Hiroaki Seki, Haruo Kobayashi (Gunma University, Japan)

[21] P87 Bias Temperature Instability Detection of Integrated Circuit
Sumit Kumar Biswas, Toru Kamiyama, Nobukazu Takai, Haruo Kobayashi
(Gunma University, Japan)

[22] P88 Design of Hysteresis Controlled Single-Inductor Multi-Output DC-DC Converter
Shunsuke Tanaka, Tatsunori Nagashima, Yasunori Kobori, Kotaro Kaneya, Takashi Okada, Takahiro Sakai, Biswas Sumit Kumar, Nobukazu Takai, Haruo Kobayashi
(Gunma University, Japan)

[23] P89 Amplifier Gain Enhancement Utilizing Negative Impedance
Daichi Motojima, Nobukazu Takai, Haruo Kobayashi (Gunma University, Japan)

[24] P102 SIDO DC-DC Buck Converter with Current Mode Control
Qiulin Zhu, Yasunori Kobori, Shu Wu, Feng Zhao, Haruo Kobayashi, Nobukazu Takai
(Gunma University, Japan)

[25] P103 Full Digital Compensation of Timing Mismatches in Interleaved ADC
Minghui Wu, Ru Yi, Koji Asami, Haruo Kobayashi, Atsuhiro Katayama, Kentaroh Katoh
(Gunma University, Advantest Corporation, Tsuruoka National College of Technology, Japan)

[26] P104 DAC Architecuture with Fibonacci Sequence Weighted Current Sources
Zhixiang Yang, Yutaro Kobayashi, Shaiful Nizam Mohyar, Masaki Kazumi, Haruo Kobayashi
(Gunma University, Japan)

「人間は意欲し、創造することによってのみ幸福である。」

（アラン 幸福論）

（文責 群馬大学 小林春夫）