20th International Mixed-Signals Testing Workshop

Paris, France
Université Pierre et Marie Curie
24-26 June 2015
http://tima.imag.fr/conferences/imstw/

Call for Papers

The role of nano-electronic systems is rapidly expanding in every facet of modern life. One of the major bottlenecks nowadays for such systems is the post-manufacturing testing of their analog, mixed-signal, RF, and MEMS functions, in order to guarantee outgoing quality while not sacrificing yield. Testing such functions is accounting for a large portion of the overall manufacturing cost. The main reasons include the pressing demand for zero defective parts-per-million, the increasing frequency of operation, the high levels of integration, the limited controllability and observability of embedded blocks, the integration of heterogeneous devices onto the same substrate, the requirement for specialized, high-cost equipment, the new defect mechanisms and excessive process variations occurring in advance technology nodes, the long test times, etc. In addition to the post-manufacturing testing problem, modern safety-critical, mission-critical, and remote-controlled systems need to be equipped with self-test, concurrent error detection, and fault-tolerance capabilities so as to detect early reliability hazards and guarantee reliable operation even in harsh environments. For such systems, diagnosing the sources of failures occurring in the field of operation is of vital importance, in order to apply corrective actions and to prevent failure reoccurrence. Diagnosis is also of vital importance to quickly identify failures in the first prototypes, in order to reduce design iterations, and for shedding light on the underlying failure mechanisms, in order to enhance yield for future product generations.

The International Mixed-Signals Testing Workshop is one of the main forums that bring together the test community to discuss ideas and views on the above challenges. The scope of the workshop includes, but is not limited to, the following topics:

- Test generation
- Fault modeling and simulation
- Test metrics estimation
- Self-healing and self-adaptation
- Built-in self-test
- Design-for-test
- Fault diagnosis
- Failure analysis
- Defect characterization
- ATE technology
- Economics of test and yield optimization
- On-line test
- Fault tolerance
- Reliability and design-for-reliability

Submissions should be via the workshop web-site and consist of either an extended summary of at least 750 words or preferably a complete 6-page paper. The workshop will produce electronic formal proceedings with an ISBN number which will become available in the IEEE Xplore digital library. A selection of papers will be invited to a special issue of Springer Journal of Electronic Testing: Theory and Applications.

Key Dates

Submission deadline: March 6, 2015
Notification of acceptance: April 24, 2015
Camera-ready full papers: May 15, 2015

General Information

H.-G. Stratigopoulos
TIMA Laboratory
Tel: +33 6 83 19 33 88
stratigo@imag.fr

Program Information

G. Léger
IMSE-CNM-CSIC
Tel: +34 954 466 660
leger@imse.cnm.es

C. Wegener
Dialog Semiconductor
Tel: +49 89 841029835
Carsten.Wegener@diasemi.com