CALL FOR PAPERS

21st International Mixed-Signal Testing Workshop

Hotel Eden Roc, Sant Feliu de Guixols, Catalunya, Spain
July 4-6, 2016
http://tima.imag.fr/conferences/imstw/imstw16/

under the umbrella of
1st IEEE Federative Event on Design for Robustness
http://tima.imag.fr/conferences/fedfro/fedfro16

General Chair
S. Bernard, LIRMM, FR

Program Chairs
M. Barragan, TIMA, FR
W. Eisenstadt, U. Florida, USA

Local Chair
L. Balado, UPC, ES

Special Session
M. Comte, LIRMM, FR
H.-G. Stratigopoulos, LIP6, FR

Publication
K. Huang, SDSU, USA

Finance
V. Kerzérho, LIRMM, FR

Publicity
S. Mir, TIMA, FR
A. Todri-Sanial, LIRMM, FR

Program Committee
J. Altet, UPC, ES
F. Azaïs, LIRMM, FR
L. Balado, UPC, ES
I. Bell, U. of Hull, UK
A. Bounceur, U. of Brest, FR
A. Chatterjee, Georgia Tech, USA
M. Comte, LIRMM, FR
J. Dabrowski, Linkoping U, SE
O. Eliezer, EverSet Tech., USA
A. J. Gines, IMSE, ES
J. Goes, U. Nova de Lisboa, PT
N. Horta, IST Lisboa, PT
J. Huang, Nat. Tawan U., TW
H. Kerkhoff, U. Twente, NL
V. Kerzérho, LIRMM, FR
H. Kobayashi, Gunma U., JP
Y. Lechuga, U. Cantabria, ES
G. Leger, IMSE, ES
J. Machado da Silva, U. Porto, PT
Y. Makris, U. Texas Dallas, USA
L. Milor, Georgia Tech, USA
S. Mir, TIMA, FR
S. Natarajan, Intel, USA
S. Sattler, Erlangen U., DE
M. Slamani, Global Foundries, USA
H. Stratigopoulos, LIP6, FR
H. M. von Staudt, Dialog Sem., DE
S. Sunter, Mentor Graphics, USA
F. Taenzler, TI, USA
Y. Tsiatouhas, U. of Ioannina, GR
D. Vazquez, U. Sevilla, ES
T. Yamaguchi, Advantest, JP

Steering Committee
F. Azais, LIRMM, FR
K. Chakrabarty, Duke U., USA
J. Abraham, U. Texas Austin, USA
A. Chatterjee, Georgia Tech, USA
K.-T. Cheng, UCSB, USA
B. Courtois, CMP, FR
J.-L. Huang, N. Taiwan U., Tw
A. Ivanov, UBC, CA
B. Kaminska, Simon Frazer U., CA
H. Kerkhoff, U. Twente, NL
J. Machado da Silva, U. Porto, PT
S. Mir, TIMA, FR
M. Renovell, LIRMM, FR
A. Richardson, U. Lancaster, UK

The role of nano-electronic systems is rapidly expanding in every facet of modern life. To interact with environment and users the Integrated Circuits need **analog, mixed-signal, RF or MEMS** blocks. These blocks could represent a low part of the chip area but have a major impact on IC Yield and reliability. Indeed, one of the major bottlenecks nowadays for nano-electonics systems is the post-manufacturing testing of their **analog**, **mixed-signal, RF, and MEMS** functions, in order to guarantee outgoing quality while not sacrificing yield. Testing such functions is accounting for a large portion of the overall manufacturing cost.

The main reasons include the pressing demand for zero defective parts-per-million, the increasing frequency of operation, the high levels of integration, the limited controllability and observability of embedded blocks, the integration of heterogeneous devices onto the same substrate, the requirement for specialized, high-cost equipment, the new defect mechanisms and excessive process variations occurring in advance technology nodes, the long test times, etc.

In addition to the post-manufacturing testing problem, modern safety-critical, mission-critical, and remote-controlled systems need to be equipped with self-test, concurrent error detection, and fault-tolerance capabilities so as to detect early reliability hazards and guarantee reliable operation even in harsh environments.

For such systems, diagnosing the sources of failures occurring in the field of operation is of vital importance, in order to apply corrective actions and to prevent failure reoccurrence.

The **International Mixed-Signal Testing Workshop (IMSTW)** is one of the main forums that bring together analog, mixed-signal, RF, and MEMS the test community to discuss ideas and views on the above challenges. The scope of the workshop includes, but is not limited to, the following topics:

- Test generation
- Fault modeling and simulation
- Test metrics estimation
- Self-healing and self-adaptation
- Built-in self-test
- Design-for-test
- Fault diagnosis
- Failure analysis
- Defect characterization
- ATE technology
- Economics of test and yield optimization
- On-line test
- Fault tolerance
- Reliability and design-for-reliability

Submissions: Submissions should be via the workshop web-site and consist of either an extended summary of at least 750 words or preferably a complete 6-page paper. The workshop will produce electronic formal proceedings with an ISBN number which will become available in the **IEEE Xplore digital library**.

A selection of papers will be invited to a special issue of **Springer Journal of Electronic Testing: Theory and Applications (JETTA).**

Key dates

Submission deadline: **March 25, 2016**
Notification of acceptance: **May 13, 2016**
Camera-ready full papers: **June 3, 2016**

General Information

Serge Bernard
LIRMM
Montpellier, France
Tel: +33 (0) 4 67 41 86 66
serge.bernard@lirmm.fr

Program Information

Manuel Barragan
TIMA
Grenoble, France
Tel: +33 (0) 4 76 57 46 81
Manuel.Barragan@imag.fr

William Eisenstadt
U. Florida
Florida, USA
Tel: +1 352-392-4946
wre@tec.ufl.edu

For all updated information, please visit the event web site:
http://tima.imag.fr/conferences/imstw/imstw16