Successive Approximation Time-to-Digital Converter With Full Digital Self-Calibration

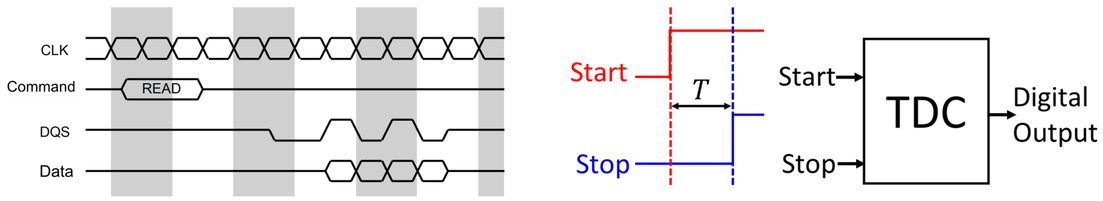
[1)]Yuki Ozawa, [1)]Congbing Li, [1)]Haruo Kobayashi, [1)]Nobukazu Tsukiji,
[2)]Ryoji Shiota, [1)]Kazumi Hatayama

1) Gunma University *2) Socionext Inc.,*

Introduction

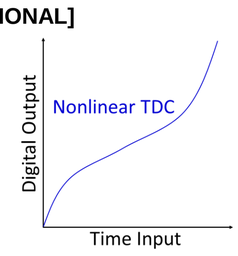
Our Target Application and Innovation

Application: High-speed I/O Interface Signal Timing Testing

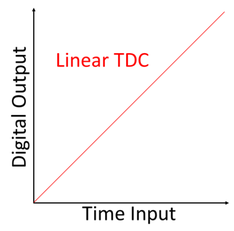


Innovation: Fine Time Resolution & High Linearity Timing Measurement Circuit with Full Digital Self-Calibration Method

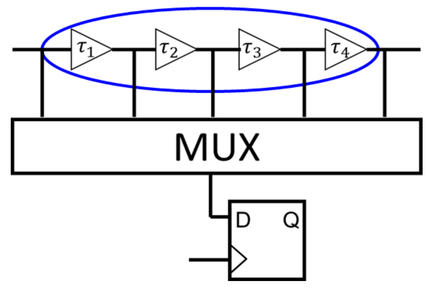
[CONVENTIONAL]



[NEW]



Research Objective



- Delay τ variation
  - Relative variation
    - ➡ TDC nonlinearity
  - Absolute(average value) variation
    - ➡ TDC input range & time resolution
- Focus on relative variation here.

Our Approach

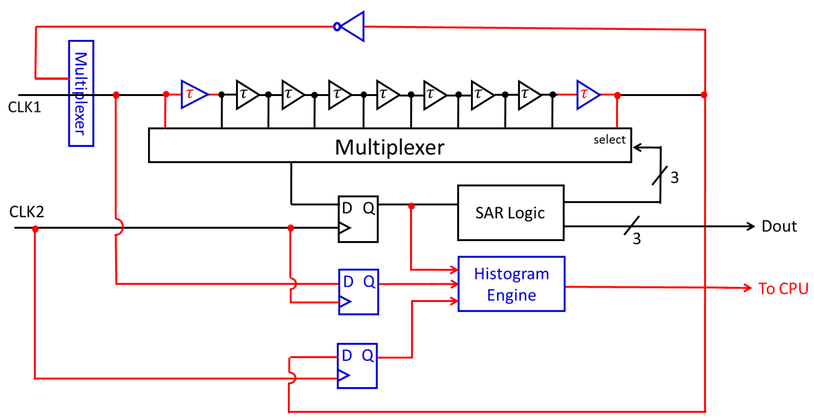
SAR-TDC with Histogram Method

- SAR TDC
  - ➡ All Digital Circuit
    - Small circuit
    - Digital output
    - FPGA
- Histogram Method
  - ➡ High linearity

Proposed Circuit

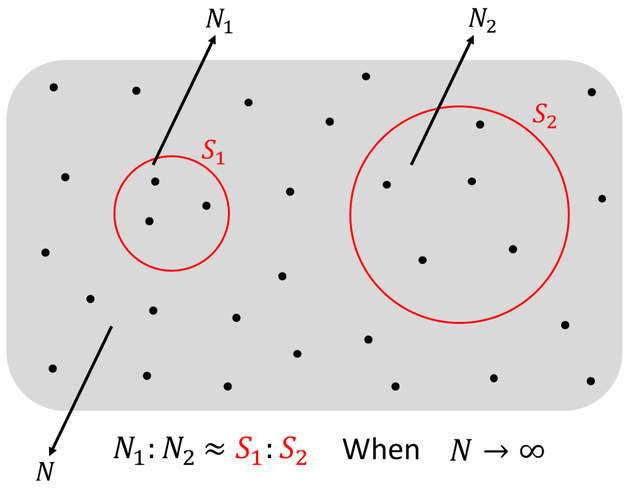
SAR-TDC Design with Calibration Circuit

SAR : Successive Approximation Register



Addition of calibration circuit, interconnection

Principle of Histogram Method



$N_1 : N_2 \approx S_1 : S_2$ When $N \to \infty$

CLK1, CLK2 are NOT correlated. ⟺ Random dots

Digital Error Correction

- TDC linearity self-calibration with histogram

Dout(0)=1	Calibration ➡	Dout(0)=0.3
Dout(1)=3		Dout(1)=2.8
Dout(2)=5		Dout(2)=4.5
Dout(3)=8		Dout(3)=7.3
⋮		⋮

Corrected based on delay variation estimation

estimating delay variation with histogram

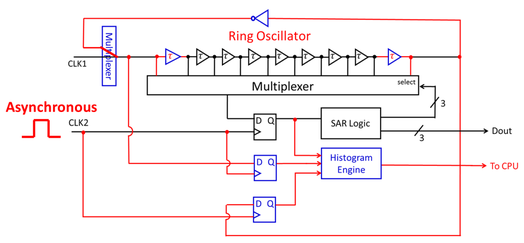
&

correcting raw TDC digital output based on estimated data

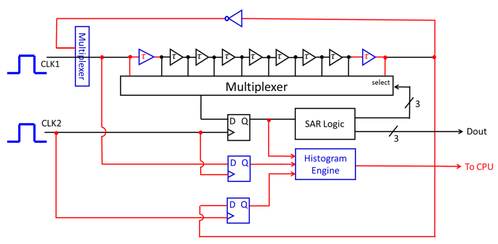
Consideration

Normal & Calibration Modes

Normal Operation Mode

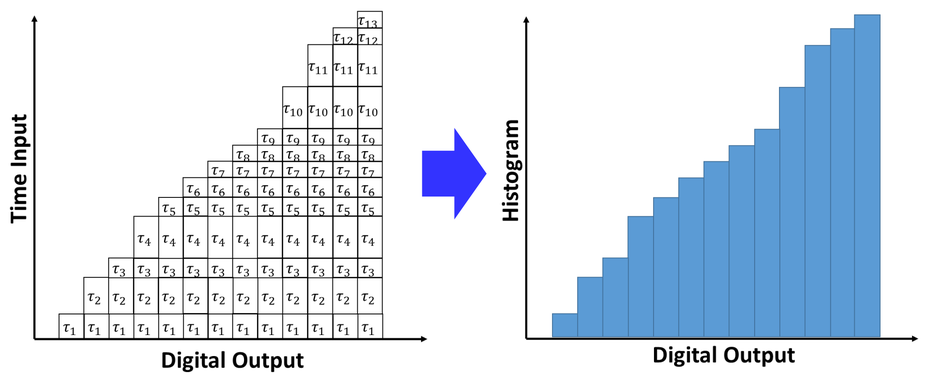


Calibration Mode

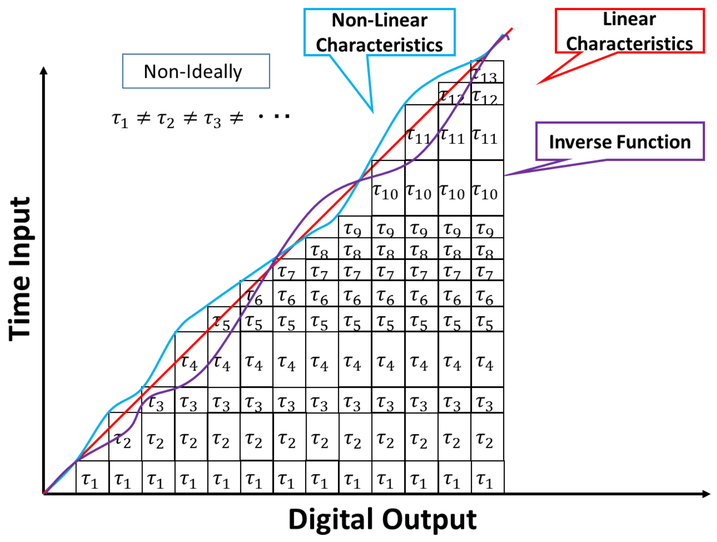


Measurement of Delay Values

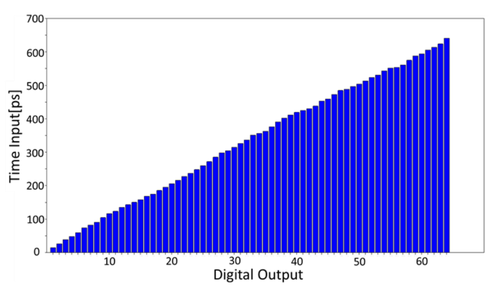
By statistical processing in Histogram Engine,
it becomes possible to indirectly know TDC characteristics



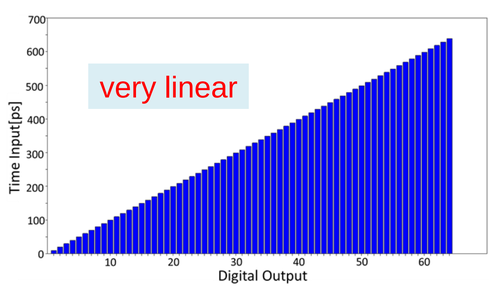
Digital Correction of TDC Nonlinearity

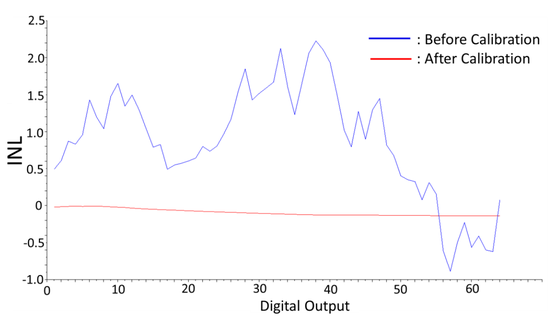


Simulation Results



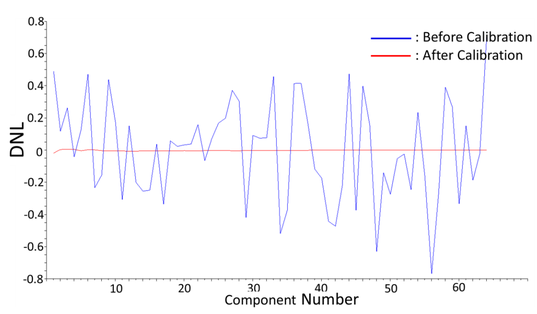
Calibration





Before Calibration
INL=2.22LSB*

After Calibration
INL=0.13LSB*



Before Calibration
DNL=0.76LSB*

After Calibration
DNL=0.02LSB*

*Worst Case

Summary

- We have implemented SAR-TDC with self-calibration by simulation.
- We have confirmed its operation, and Histogram Method effectiveness.
- It can be timing testing BOST
  - full digital
  - suitable for FPGA implementation
  - high linearity
  - small circuit.

References

[1] T. Chujo, D. Hirabayashi, K. Kentaroh, et al.,
"Experimental Verification of Timing Measurement Circuit With Self-Calibration",
IEEE IMS3TW, Brazil (Sept. 2014).

[2] R. Jiang, C. Li, M. Yang, H. Kobayashi, Y. Ozawa, R. Shiota, K. Hatayama, et al.,
"Successive Approximation Time-to-Digital Converter with Vernier-level Resolution",
IEEE IMSTW, Spain（July 2016).

[3] S. Ito, S. Nishimura, H. Kobayashi, et al.,
"Stochastic TDC Architecture with Self-Calibration,"
IEEE Asia Pacific Conf. Circuits and Systems, Kuala Lumpur, Malaysia (Dec. 2010).