3rd IEEE International Workshop on
Test and Validation of High Speed Analog Circuits
Disneyland Hotel, Anaheim, California, USA
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Held in conjunction with IEEE International Test Conference 2013

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Call for Papers

Scope

Demand for higher bandwidths never lets up in the world of communication and networks. While we struggle today to make 40Gbps line-rates a reality, plans are already afoot for 400Gbps. Similarly in wireless communications, 60Ghz is coming on-line today, but designers are already planning the next few generations up to Thz. *What is high-speed?* It clearly depends: on the medium of transmission, on power constraints, on process technology, on link parallelism, on cost and quality requirements and on the electrical and thermal environment of operation. These constraints define a multi-dimensional box that designers are placed in and asked to provide the highest bandwidth they can, inside a room whose walls seem constantly to move inwards. A lot of the functionality is increasingly analog with strict standards regulating their design and use. And it is a race with no end in sight.

The IEEE Workshop on Test and Validation of High Speed Analog Circuits is designed to address a big aspect of this race: *cost and quality*. Increasing speed has given rise to a spike in complexity of analog circuits. This has been further stressed by the need for integrating with digital functionality in SOCs. Whether embedding in monolithic dice or integrating in a SiP, integration has thrown its share of problems. Defect coverage alone is no longer sufficient to qualify a die. We need parametric coverage, as early in the manufacturing flow, as possible. This workshop addresses defect and parametric coverage of all analog circuits involved in making high bandwidth communications a reality. The scope of the workshop includes:

- SERDES test and characterization
- RF circuits test and characterization
- Self-healing, self-calibration and self-adaptation techniques
- Built-in test and design-for-test
- High speed data converter test and characterization
- 3D and KGD considerations
- High speed PLL test and characterization
- Clock jitter and skew measurement
- Phase noise measurement
- Precision delay-line test and characterization
- AC and DC supply noise measurement
- Analog fault modeling and fault simulation
- Analog test bus design
- ATE technology
- Board technology
- Economics of test and yield optimization

Author information

Prospective authors are invited to submit extended summaries or full papers up to 6 pages. Proposals for special sessions, hot topics, and panel sessions are also invited. Submissions are due no later than **June 15th, 2013**. Submissions should be made by e-mail to

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Notification e-mails of acceptance will be sent by **July 15th, 2013**.

Authors of accepted papers, special sessions, hot topics, and panel sessions should submit final manuscripts by **July 31, 2013** for inclusion in the Workshop Digest of Papers, which will be provided to the attendees.