Technical Program

35th IEEE VLSI TEST SYMPOSIUM (VTS 2017)

http://www.tttc-vts.org

IEEE Philadelphia Section

IEEE COMPUTER SOCIETY

Caesars Palace
Las Vegas, Nevada, USA
April 9th - April 12th, 2017

35th IEEE VLSI Test Symposium (VTS 2017)
Las Vegas, Nevada, USA, April 9 - 12, 2017

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35th IEEE VLSI Test Symposium (VTS 2017)
Welcome Message

Welcome to VTS 2017, the thirty-fifth in a series of annual symposia that focuses on innovation in the field of testing of integrated circuits and systems.

The VTS 2017 program will be kicked off with a plenary keynote address from a very distinguished and influential speaker in the semiconductor industry - Dr. Ahmad Bahai, who is the Chief Technology Officer of Texas Instruments and director of TI Corporate Research, Kilby Labs as well as a consulting professor at Stanford University. This will be followed by an invited keynote address, which this year will be in the form of a keynote tribute to a luminary in our field - the late Prof. Melvin Breuer.

The core of VTS 2017, the three day technical program, responds to the many trends and challenges in the semiconductor design and manufacturing industries, with papers and presentations in the research paper sessions covering the core set of test topics: Analog, Mixed-Signal & RF Test; Delay and Performance Testing; ATPG & Test Compression; Design for Test, Debug and Reliability; Memory Testing and Repair; Reliability Analysis and Yield Optimization; Hardware Security; Test Economics and Test Standards; Test Quality and Reliability. VTS also hosts the E.J. McCluskey Doctoral Thesis Competition to showcase the exciting student research in test. VTS also continues a recent NSF-supported student-focused initiative this year – Student Activities Program – to encourage Masters and early Ph.D. students to participate in the conference.

VTS continues its tradition of drawing the leading test practitioners and researchers in both industry and academia to contribute to the innovative practices (IP), special sessions, and new topic sessions, enabling it to be the venue where future technology trends and test challenges are deliberated, test practices are shared, and test research roadmap is chartered. This year, we have a rich offering of diverse topics in the IP and special sessions: Layout Sensitive Defect Screening, Analog Test Simplification in Industry; Intelligent Physical Systems; Hardware Security and Physical Tamper Attacks; Variation-tolerant Design; Early Life Failures; Test Data Analytics; Automotive Testing and Functional Safety; MEMS Testing; IEEE Test Standards Future Extensions; Innovative Practices in Asia from Cost and Quality Perspectives; Diagnostics; Formal Verification; Autonomous Cars; 5G Test Challenges; Software Testing; Emerging Non-volatile Memories.

Welcome Message

Two new topic sessions are offered with focus on emerging systems namely Internet of Things (IoT) as well as the foundry perspective on designing versatile semiconductor solutions.

The highly popular Monday Evening Wine-and-Cheese Panel takes a different path this year - a Test Trivia Game that promises to engage and challenge the gray cells of the very best in test! Prior to the start of the conference program, two half-day tutorials will also be offered on Mixed-signal DFT & BIST and Automotive Reliability & Test Strategies.

VTS is also organizing an exciting social program which starts with an early-evening reception at the Madame Tussauds Las Vegas museum, which will provide access to the exhibits and an opportunity for informal discussions among participants in a relaxed setting, followed by a stroll down the Las Vegas strip, and finishes with a viewing of the show KA by Cirque du Soleil.

VTS is the result of the work of many dedicated volunteers: the reviewers, the best paper award judges, the Program Committee, the Organizing Committee, and the Steering Committee. We wholeheartedly thank them all. We also wish to thank all the authors who submitted their work to VTS 2017, and the program participants for their contributions to the Symposium. We thank the IEEE Computer Society, the IEEE Philadelphia Section and the IEEE Computer Society Test Technology Technical Council for the continued technical sponsorship and support. Furthermore, we are indebted to ams AG and Tessolve, the Elite Corporate Supporters for VTS 2017, as well as our our Premier Corporate Supporters (Cisco, Qualtera, Synopsys, Qualcomm and Cadence) and our Corporate Supporters (Mentor Graphics and Advantest) for their partnership and continued support of this symposium.

We hope that you will find VTS 2017 enlightening, thought-provoking, rewarding, and enjoyable. We wish you all a fun-filled and productive week in the Las Vegas area and we hope that you will keep making VTS a success by actively participating in it, assisting in its organization, and letting us always know how we can improve the symposium experience and increase its value for its audience.

Thank you all for coming!

General Chair
Yiorgos Makris

Program Chairs
Srivaths Ravi
Amit Majumdar

The VLSI Test Symposium is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society

The IEEE promotes the engineering process of creating, developing, integrating, sharing, and applying knowledge about electronic and information technologies and sciences for the benefit of humanity and the profession

IEEE
Philadelphia Section

The purposes of this IEEE Society shall be scientific, literary, and educational in character. The Society shall strive to advance the theory, practice, and application of computer and information processing science and technology and shall maintain a high professional standing among its members. The scope of the Society shall encompass all aspects of theory, design, practice, and application relating to computer and information processing science and technology

IEEE COMPUTER SOCIETY

TTTC's goals are to contribute to our members' professional development and advancement, to help them solve engineering problems in electronic test, and to help advance the state of the art. In particular, TTTC aims at facilitating the knowledge flow in an integrated manner, to ensure overall quality in terms of technical excellence, fairness, openness, and equal opportunities

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REGISTRATION

The IEEE VLSI Test Symposium explores emerging trends and novel concepts in the testing of integrated circuits and systems. The symposium is a leading international forum where many of the world's leading test experts and professionals from both industry and academia join to present and debate key issues in testing. VTS 2017 addresses key trends and challenges in the semiconductor design and manufacturing industries through an exciting program that includes Keynote and Plenary Talks, Technical Paper Sessions, Embedded Tutorials, Panels, Hot Topic Sessions, Half-day Tutorials, and the Innovative Practices Track.

SYMPOSIUM REGISTRATION

Full registration *includes breakfasts, lunches, coffee breaks, social event and electronic distribution of the symposium proceedings.*
Student registration *includes all of the above except the social event.*

VTS 2017 April 9 - 12	Advance Rate (March 20, 2017, midnight PDT)	Onsite Rate (After March 20, 2017)
IEEE Member Registration (Member rates are available only to current members of IEEE. Please enter your valid membership number in order to qualify!)	$650.00	$770.00
IEEE Lifetime Member Registration	$350.00	$425.00
IEEE Non-Member Registration	$780.00	$925.00
IEEE Student Member Registration (Valid student ID may be required at onsite registration check-in.)	$350.00	$425.00
Student IEEE Non-Member Registration (Valid student ID may be required at onsite registration check-in.)	$500.00	$600.00
Social Event and Dinner Ticket (One Ticket is included for those paying IEEE Member or Non-Member VTS rates). Students and companions of registered attendees may select to purchase a social ticket at the end of the registration process.	$125.00	$125.00
Additional Lunch Ticket (Lunch is included for those paying IEEE/CS Member or Non-Member VTS rates). Companions of registered attendees may select to purchase lunch tickets at the end of the registration process.	$65 per day	$65 per day

TTEP Tutorials Registration

April 9th, 8:30 a.m. - 04:30 p.m.

	Advance Rate (March 20, 2017, midnight PDT)	Onsite Rate (After March 20, 2017)
Single Tutorial (morning or afternoon) April 9		
IEEE Member, Student or Lifetime Member	$200.00	$250.00
IEEE Non-Member	$240.00	$300.00
Two Tutorials (morning and afternoon) April 9		
IEEE Member, Student or Lifetime Member	$300.00	$375.00
IEEE Non-Member	$360.00	$450.00

TRAVEL INFO:

Las Vegas is the largest city in the U.S. state of Nevada. Nicknamed the Entertainment Capital of the World, it is situated in the Mojave Desert of Southern Nevada. The city features many mega-hotel/casino complexes decorated with lavish care and attention to detail creating a fantasy-like environment. The casinos often have names and themes that evoke romance, mystery, and exotic destinations.

McCarran International Airport (IATA: LAS) is the main airport serving the Las Vegas area. There are many airport bus lines which run between airport and city.

In addition, shuttle buses also operate between McCarran International Airport and the Caesars Palace Hotel, where the symposium is held.

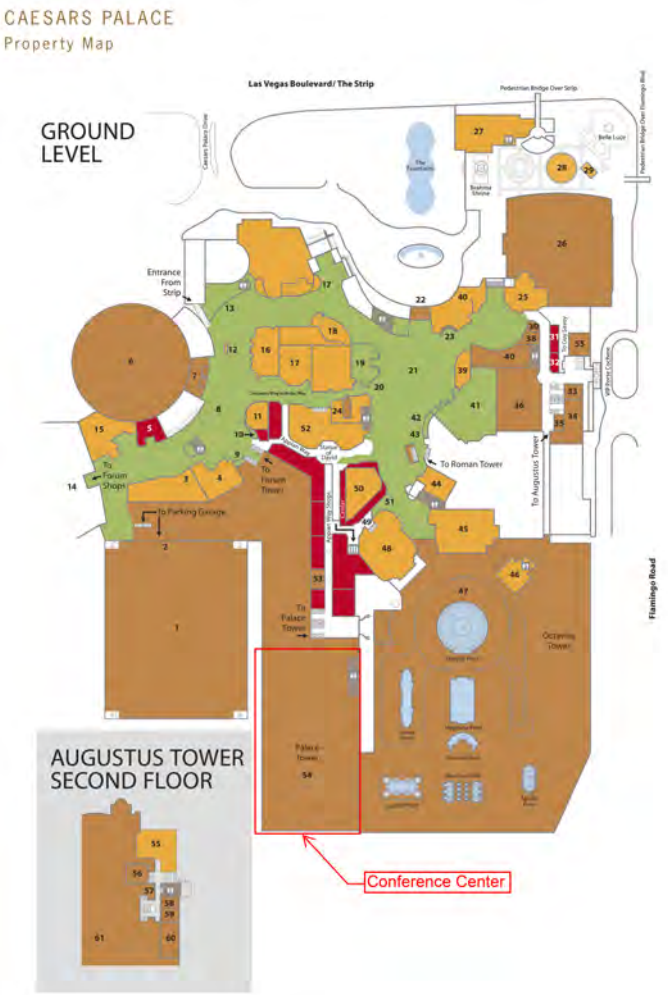
The 35th IEEE VLSI Test Symposium will be held at the Caesars Palace. From the moment you walk through the doors of Caesars Palace, you'll understand why this iconic Las Vegas luxury hotel sets the standard for opulent details, impeccable service and lavish Las Vegas accommodations. Special touches make the difference between an ordinary visit to Las Vegas and a spectacular experience. Caesars Palace is one of the most prestigious casino hotels in the world and one of Las Vegas's largest and best known landmarks.

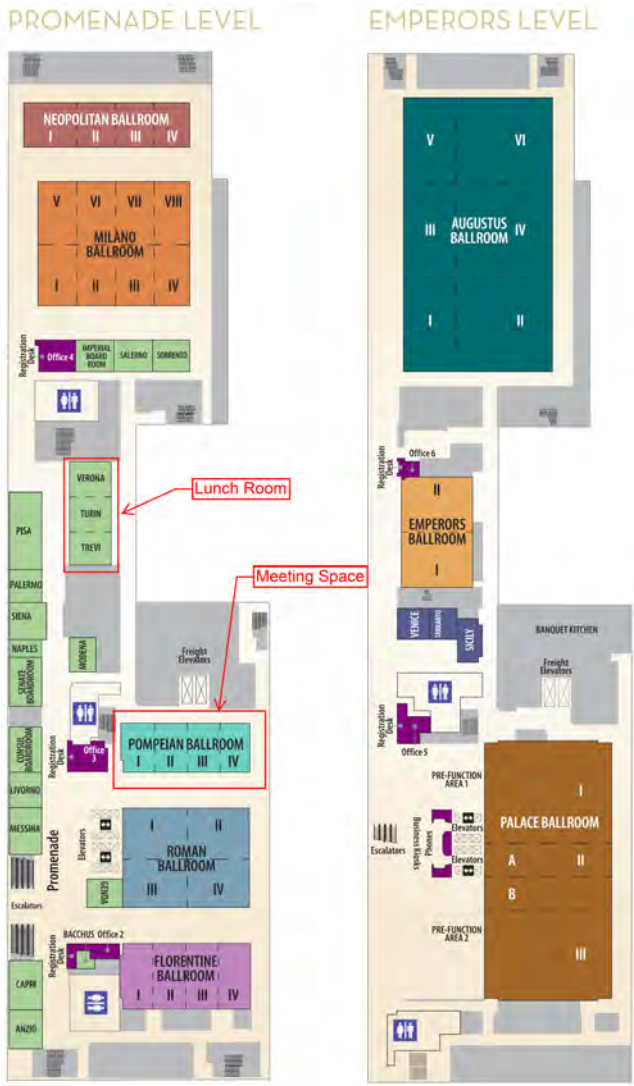
Hotel Reservation Procedure:

Discounted rates of **$150** and **$173** for Forum Classic and Palace Deluxe rooms, respectively, have been made available to VTS 2017 attendees until March 20, 2017 at 5pm PDT or until the room block is sold out, whichever comes first. Applicable room taxes of 12.5% and a $32 daily resort fee are not included in this price.

Visit the following web-site to reserve a room:
https://aws.passkey.com/go/SCIEE7

Hotel Home Page: https://www.caesars.com/caesars-palace
Address: 3570 S Las Vegas Blvd, Las Vegas, NV 89109
Telephone: +1 (866) 227-5938


CAESARS PALACE
Property Map
GROUND LEVEL
Las Vegas Boulevard/ The Strip
Entrance From Strip
To Forum Shops
To Parking Garage
To Forum Tower
To Roman Tower
To Augustus Tower
To Palace Tower
Flamingo Road
AUGUSTUS TOWER SECOND FLOOR
Conference Center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Office 4
IMPERIAL BOARD ROOM
SALERNO
SORRENTO
VERONA
TURIN
TREVI
Lunch Room
Meeting Space
PISA
PALERMO
SIENA
NAPLES
ESTATE BOARDROOM
MODENA
Freight Elevators
POMPEIAN BALLROOM
I II III IV
Office 3
CORFU BOARDROOM
LIVORNO
MESSINA
Promenade
Elevators
ROMAN BALLROOM
I II III IV
VENUS
Escalators
BACCHUS Office 2
CAPRI
ANZIO
FLORENTINE BALLROOM
I II III IV
AUGUSTUS BALLROOM
V VI III IV I II
Office 6
EMPERORS BALLROOM
II I
VENICE
FERRARA
SICILY
BANQUET KITCHEN
Office 5
PRE-FUNCTION AREA 1
PALACE BALLROOM
I A II B III
Elevators
Escalators
Banquet Kitchen
PRE-FUNCTION AREA 2

The Tutorials and Education Group of the IEEE Computer Society Test Technology Technical Council (TTTC) organizes in 2017 a comprehensive set of Test Technology Tutorials to be held in conjunction with TTTC sponsored technical meetings and included in the annual and expanding Test Technology Educational Program (TTEP). TTEP intends to serve the test and design professionals offering fundamental education and expert knowledge in state-of-the-art test technology topics.

VTS 2017 is offering 2 half-day TTEP tutorials, one in the morning and one in the afternoon of Sunday April 9, 2017, for which a separate registration fee is required. Attendees who register for the tutorials may select either one or both of the offered tutorials. Registration includes a hard copy of the tutorial material, breakfast, coffee breaks and lunch. The two tutorials are:

Morning Tutorial (8:30 a.m. – 12:00 p.m.)

Tutorial #1: Mixed-signal DFT & BIST: Trends, Principles, and Solutions
Instructor: *Stephen Sunter (Mentor Graphics)*
Room: Pompeian III

Afternoon Tutorial (1:00 p.m. – 4:30 p.m.)

Tutorial #2: Automotive Reliability & Test Strategies
Instructor: *Yervant Zorian (Synopsys)*
Room: Pompeian III

Monday, April 10, 2017

07:30AM - 08:30AM	Registration and Breakfast
08:30AM - 10:30AM	**Plenary Session** HALL : Pompeian I/II **Welcome Message:** Y. Makris (U. of Texas at Dallas), General Chair **Program Introduction:** S. Ravi (Texas Instruments), A. Majumdar *(Xilinx)*, Program Co-Chairs **Opening Keynote:** *Dr. Ahmad Bahai, (CTO, Texas Instruments)* **Keynote Tribute to Professor Melvin Breuer - Contributions to CAD and Test** **Organizer:** *Sandeep Gupta, U. of Southern California* **Speakers:** *Miron Abramovici (Miron PhotoArt), Magdy Abadir (Helic Inc.), Sridhar Narayanan (Apple Inc.)*
10:30AM - 11:10AM	Break
11:10AM - 12:10PM	**Sessions 1**
	Session 1A: Analog, Mixed-Signal and RF Test I HALL : Pompeian I **Moderator:** Stephen Sunter *(Mentor Graphics)* • **A Technique for Dynamic Range Improvement of Intermodulation Distortion Products for an Interpolating DAC-based Arbitrary Waveform Generator Using a Phase Switching Algorithm** *Peter Sarson (ams AG), Shohei Shibuya, Tomonori Yanagida, Haruo Kobayashi (Gunma U.)* • **Accurate Jitter Decomposition in High-Speed Links** *Yan Duan (Iowa State U.), Degang Chen (Iowa State U.)* **(Best Paper Nominee)** • **Adaptive test flow for mixed-signal ICs** *Haralampos Stratigopoulos (Sorbonne U., UPMC U. Paris 6, CNRS, LIP6), Christian Streitwieser (ams AG)*

Session 1B: Delay and Performance Test
HALL : Pompeian II

Moderator: Purna Mohanty *(Tessolve)*

- **A New Delay Testing Signal Scheme Robust to Power Distribution Network Impedance Variation** *Claude Thibeault, Ali Louati (E. Tech. Sup. Montreal)*
- **Aging Monitor Reuse for Small Delay Fault Testing** *Chang Liu (U. of stuttgart), Michael Kochte, Hans-Joachim Wunderlich (U. of Stuttgart)*
- **An Optimised SDD ATPG and SDQL Computation Method Across Different Pattern Sets** *Wilson Pradeep (Texas Instruments), Prakash Narayanan (Texas Instruments India Pvt. Ltd), Rubin Parekhji (Texas Instruments (India))*

IP Session 1C: Screening for Layout Sensitive Defects
HALL : Pompeian III

Organizers & Moderators: Arani Sinha, Nitin Chaudhary (Intel Corporation)

- **Fast yield learning method using correlation of manufacturing defects on circuits based on DFM rule check** *Tapan Chakraborty (Qualcomm)*
- **Screening Yield Systematics Through Holistic Volume Diagnosis in a Leading-edge Foundry** *Yan Pan (Global Foundries)*
- **Physical pattern analysis to identify test escape risks** *Ya-Chieh Lai (Cadence Design Systems)*

12:30PM - 01:30PM

Lunch (A word from our Elite Supporters)
Speakers: Purna Mohanty *(Tessolve)*,
Peter Sarson *(ams AG)*

01:40PM - 02:40PM

Sessions 2

Session 2A: ATPG I

HALL : Pompeian I

Moderator: Loganathan Lingappan *(Intel Corporation)*

- **Fail Data Reduction for Diagnosis of Scan Chain Faults under Transparent-Scan** *Irith Pomeranz (Purdue U.)*
- **Methodology of Generating Dual-Cell-Aware Tests** *Yu-Hao Huang, Ching-Ho Lu, Tse-Wei Wu, Yu-Teng Nien (National Chiao Tung U.), Ying-Yen Chen, Max Wu, Jih-Nung Lee (Realtek Semiconductor Corp.), Mango Chao (National Chiao Tung U.)* **(Best Paper Nominee)**
- **Test-Set Reordering for Improving Diagnosability** *Cheng Xue, Ronald Blanton (Carnegie Mellon U.)*

Session 2B: New Topic: Innovation for Emerging Smart IoT Systems

HALL : Pompeian II

Organizer & Moderator: *Bozena Kaminska (Simon Fraser U.) and Bernard Courtois (CMP)*

Speaker: *Dr. May Wu (Director of Wireless System Arch, Intel Labs)*

IP Session 2C: How is Industry Simplifying Analog Test?

HALL : Pompeian III

Organizer: *Rubin Parekhji (Texas Instruments)*

Moderator: *Srinivas Modekurty (Intel Corporation)*

- **Analog / Mixed Signal Block Level Structural Test** *Ramana Tadepalli (Texas Instruments)*
- **Test Hardware to Support JESD 204C Converter Test** *Jeff Kennedy (Analog Devices)*
- **An Integrated Approach to Testing Analog Sub-systems in Large Digital SoC** *Thecla Chomicz (NXP Semiconductors)*

02:40PM - 03:00PM	Break
03:00PM - 04:00PM	**Sessions 3**

Session 3A: Design for Test, Debug and Reliability
HALL : Pompeian I

Moderator: *Chennian Di (Xilinx)*

- **Fast WAT Test Structure for Measuring Vt Variance Based on Latch-based Comparators** *Kao-Chi Lee, Kai-Chiang Wu, Chih-Ying Tsai, Mango Chao (National Chiao Tung U.)* **(Best Paper Nominee)**

- **Flip-flop Clustering based Trace Signal Selection for Post-Silicon Debug** *Yun Cheng (The Institute of Computing Technology of the Chinese Academy of Sciences), Huawei Li (Chinese Academy of Sciences), Ying Wang (The Institute of Computing Technology of the Chinese Academy of Sciences), Xiaowei Li (Institute of Computing Technology, CAS), Gao Yingke, Bo Liu (Beijing Institute of Control Engineering)*

- **HLDTL: High-performance, low-cost, and double node upset tolerant latch design** *Aibin Yan (Anhui U.), Zhengfeng Huang, Maoxiang Yi, Jie Cui, Huaguo Liang (Heifei U. of Technology)*

Special Session 3B: Hot Topic: Intelligent Physical Systems: Test, Diagnosis, Reconfiguration and Correction
HALL : Pompeian II

Organizer & Moderator: Abhijit Chatterjee (Georgia Institute of Technology)

- **Context-Aware Self-Optimizing IoT Sensor Nodes** *Shreyas Sen (Purdue U.)*

- **Error Detection and Learning-assisted Correction in Real-time Systems Using Algorithmic Encoding** *Abhijit Chatterjee (Georgia Institute of Technology)*

- **Approximate Computing: Beyond the Tyranny of Digital Abstractions** *Hadi Ismaelzadeh (Georgia Institute of Technology)*

IP Session 3C: Hardware Security
HALL : Pompeian III

Organizer & Moderator: *Jeyavijayan Rajendran (UT-Dallas)*

- **Robust Secure Design by Increasing the Resilience of Attack Protection Blocks** *Sohrab Aftabjahani (Intel Corporation)*
- **System-on-Chip Security for the Internet of Things: Challenges and Recent Trends** *Sandip Ray (NXP Semiconductors)*
- **Establishing a trust chain in electronic manufacturing** *Michael Chen (Mentor)*

04:00PM - 04:20PM — Break

04:20PM - 05:20PM — **Sessions 4**

IP Session 4A: Variation-tolerant design of circuits/systems
HALL : Pompeian I

Organizer & Moderator: *Arijit Raychowdhury (Georgia Institute of Technology)*

- **Adaptive and resilient high performance memory design for dynamic variation tolerance** *Jaydeep Kulkarni (Intel Corporation)*
- **Auto-Calibrating Adaptive Design for Improving Performance and Energy Efficiency while Eliminating Tester Calibration** *Keith Bowman (Qualcomm)*
- **Use of Process monitors in Post silicon validation to reduce TTM (time to market)** *Hemanth Shivalingaiah (Intel Corporation)*

Session 4B: Hot Topic: Early Life Failures
HALL : Pompeian II

Organizer: *Sybille Hellebrand (U. of Paderborn)*
Moderator: *Hans-Joachim Wunderlich (U. of Stuttgart)*

- **Brief introduction to Early Life Failures** *Hans-Joachim Wunderlich (U. of Stuttgart)*
- **Testing and Fault Localization for Embedded Controllers** *Jyotirmoy Deshmukh (Toyota Technical Center)*
- **A HW/SW Cross-Layer Approach for Determining Application-Critical Hardware Faults in Embedded Systems** *Wolfgang Kunz (TU Kaiserlautern)*

IP Session 4C: Data Analytics in Test
HALL : Pompeian III

Organizer: *Suriya Natarajan (Intel Corporation)*
Moderator: *Abhijit Sathaye (Intel Corporation)*

- **Big Data Analytics Engines for End-to-End Supply Chain and Quality Control** *Thomas Harper, Paul Simon (Qualtera)*
- **Data Mining of Defective Parts Investigation in Test** *Rahima Mohammed (Intel Corporation)*
- **Intelligent Data Driven Test Eco-system** *Amit Nahar (Texas Instruments)*

06:00PM - 08:00PM	**TPC Meeting (by invitation only)**
08:00PM - 09:30PM	**Monday Evening "Wine and Cheese" Special Session: Test Trivia Game** HALL : Pompeian I/II **Organizers:** *Rohit Kapur and Anshuman Chandra (Synopsys), and Gaurav Reddy (UT Dallas)*

Tuesday, April 11, 2017

07:30AM - 08:30AM	Registration and Breakfast
08:30AM - 09:30AM	**Sessions 5**

Session 5A: Memory Test and Repair
HALL : Pompeian I

Moderator: *Ramesh Tekumulla (Broadcom)*

- **A Methodology for Estimating Memory Lifetime Using a System-Level Accelerated Life Test and Error-Correcting Codes** *Dae-Hyun Kim, Linda Milor (Georgia Institute of Technology)*
- **At-Speed Capture Global Noise Reduction & Low-Power Memory Test Architecture** *Bonita Bhaskaran (NVIDIA Corp.), Sailendra Chadalavada, Shantanu Sarangi (Nvidia), Nithin Valentine (NVIDIA Corp.), Venkat Abilash Reddy Nerallapally (NVIDIA Corp.), Ayub Abdollahian (Nvidia)*
- **Leveraging Systematic Unidirectional Error-Detecting Codes for fast STT-MRAM Cache** *Nour Sayed (Karlsruhe Institute of Technology), Fabian Oboril, Rajendra Bishnoi, Mehdi Tahoori (Karlsruhe Institute of Technology)*

Session 5B: Reliability Analysis and Yield Optimization
HALL : Pompeian II

Moderator: *Ujjwal Guin (Auburn U.)*

- **An Analytical Model for Predicting the Residual Life of an IC and Design of Residual-Life Meter** *Md Nazmul Islam, Sandip Kundu (University of Massachusetts Amherst)*
- **Learning the Process for Correlation Analysis** *Sebastian Siatkowski (UC Santa Barbara), Li-C. Wang (UC Santa Barbara), Nik Sumikawa, LeRoy Winemberg (NXP Semiconductors)*
- **Performance-Aware Reliability Assessment of**

Heterogeneous Chips *Athanasios Chatzidimitriou, Manolis Kaliorakis, Sotiris Tselonis, Dimitris Gizopoulos (U. of Athens)*

IP Session 5C: Automotive Test Solutions
HALL : Pompeian III

Organizer: *Peter Sarson (ams, AG)*
Moderator: *Wim Dobbelaere (ON Semiconductor)*

- **Automotive IC Testing with BOST Approach** *Ryoji Shiota (Socionext), Haruo Kobayashi (Gunma U.)*
- **Automotive Alternative Test** *Peter Sarson (ams AG), Constantinos Xanthopoulos (UTDallas)*
- **Test methodologies to minimize test cost for Automotive / Safety devices** *Santosh Kavalur (Texas Instruments)*

09:30AM - 09:50AM Break

09:50AM - 10:50AM **Sessions 6**

Session 6A: ATPG II
HALL : Pompeian I

Moderator: *Vivek Chickermane (Cadence)*

- **A Framework for Fast Test Generation at the RTL** *Kelson Gent, Akash Agrawal (Virginia Polytechnic Institute and State U.), Michael Hsiao (Virginia Tech)*
- **Efficient SAT-Based Generation of Hazard-Activated TSOF Tests** *Jan Burchard, Dominik Erb (U. of Freiburg), Sudhakar Reddy (U. of Iowa), Adit Singh (Auburn U.), Bernd Becker (U. of Freiburg)*
- **Using Piecewise-Functional Broadside Tests for Functional Broadside Test Compaction** *Irith Pomeranz (Purdue U.)*

Session 6B Hot Topic: Physical Attacks: Can Test Save Us?
HALL : Pompeian II

Organizers: Swarup Bhunia, Mark Tehranipoor *(U. of Florida)*
Moderator: *Swarup Bhunia (U. of Florida)*

- **New Realm in Physical Attacks** *Peter R Munguia (Intel Corporation)*
- **Simulation-Based Verification of EM Side-Channel Attack Resilience** *Michael Orshansky (U. of Texas at Austin)*
- **Attacks on FPGA Bitstream: Piracy & Tampering in Field** *Yousef Iskander (Cisco)*

IP Session 6C: DFT for Functional Safety
HALL : Pompeian III

Organizer: *Prashant Goteti (Intel Corporation)*
Moderator: *Sreejit Chakravarty (Intel Corporation)*

- **Autonomous Driving and IOT: Combining Functional Safety, Reliability, Availability and Security for a resilient connected world** *Riccardo Mariani (Intel Corporation)*
- **New paradigms for Functional Safety in advances CMOS nodes** *Vincent Huard (ST Micro)*
- **Low Overhead Design and Test Techniques for Application Specific Functional Safety** *V. Prasanth, Rubin Parekhji (Texas Instruments)*

10:50AM - 11:10AM	Break
11:10AM - 12:10PM	**Sessions 7**

Session 7A: Hardware Security
HALL : Pompeian I

Moderator: *Swarup Bhunia (U. of Florida)*

- **A Novel Design-for-Security (DFS) Architecture to Prevent Unauthorized IC Overproduction** *Ujjwal Guin, Zhou Ziqi, Adit Singh (Auburn U.)*
- **Dynamically Obfuscated Scan for Protecting IPs Against Scan-Based Attacks Throughout Supply Chain** *Dongrong Zhang, Xiaoxiao Wang (Beihang U.), Miao HE, Mark Tehranipoor (U. of Florida)*

- **FISCAL: Firmware Identification Using Side-Channel Power Analysis** *Deepak Krishnankutty (UMBC), Ryan Robucci, Nilanjan Banerjee (U. of Maryland Baltimore County), Chintan Patel (UMBC)*

Special Session 7B: Embedded Tutorial: MEMS Testing Challenges, Issues and Solutions
HALL : Pompeian II

Presenters: *Ray Sessego, Tehmoor Dar, Peter Jones (NXP Semiconductors)*

IP Session 7C: Automotive Quality Assurance
HALL : Pompeian III

Organizer & Moderator: Peter Sarson *(ams, AG)*

- **Adapting IEEE 1687 PDL for Writing Analog Tests** *Jeff Rearick (AMD)*
- **Testing of mixed signal automotive circuits: do we guarantee the spec or do we catch defects?** *Wim Dobbelaere (ONSemi)*
- **Meeting quality for Automotive Application with IO interfaces** *Salem Abdennadher (Intel Corporation)*

12:10PM - 01:30PM Lunch

01:30PM - 02:30PM **Sessions 8**

Special Session 8A HOT TOPIC: Future Extensions of IEEE Test Standards
HALL : Pompeian I

Organizer: *Jennifer Dworak (Southern Methodist U.)*
Moderator: *Yu Huang (Mentor Graphics)*

- **From 1687 to 1687.1** *Martin Keim (Mentor Graphics)*
- **Extending IEEE 1687 for Use on Analog / Mixed-Signal Chips** *Jeff Rearick (AMD)*
- **IEEE Std P1838: DFT Up and Down the Stack** *Adam Cron (Synopsys)*

	Session 8B: New Topic: Designing Versatile Semiconductor Solutions Optimizing Performance, Power, & Cost to Market Opportunities HALL : Pompeian II
	Organizers: *Bozena Kaminska (Simon Fraser U.) and Bernard Courtois (CMP)* **Speaker:** *Chafik Behidj (Global Foundries)*
01:30PM - 03:00PM	**Special Session 8C:** E.J. McCluskey Doctoral Thesis Competition (Presentations & Posters) HALL : Pompeian III
	Organizers: *Michele Portolan (TIMA Laboratory), Naghmeh Karimi (U. of Maryland Baltimore County)* **Moderator:** *Naghmeh Karimi (U. of Maryland Baltimore County)*
	Contestant: Robert Karam (U. of Florida), **Advisor:** Swarup Bhunia **Thesis title:** Energy-Efficient and Secure Reconfigurable Computing Architecture
	Contestant: Yu Liu (The U. of Texas at Dallas) **Advisor:** Yiorgos Makris **Thesis title:** Hardware Trojans in Wireless Cryptographic ICs
	Contestant: Cheng Xue (Carnegie Mellon U.) **Advisor:** R.D. (Shawn) Blanton **Thesis title:** Optimizing IC Testing for Diagnosability, Effectiveness and Efficiency
	Contestant: Yuming Zhuang (Iowa State U.) **Advisor:** Degang Chen **Thesis title:** Accurate and Robust Spectral Testing with Relaxed Instrumentation Requirements
03:00PM - 03:30PM	Break
03:30PM - 09:30PM	**Social Event**

Wednesday, April 12, 2017

07:30AM - 08:30AM	Registration and Breakfast
08:30AM - 09:30AM	**Sessions 9**

Session 9A: Analog, Mixed Signal and RF Testing **II**
HALL : Pompeian I

Moderator : *Haralampos Stratigopoulos (UMPC-LIP6)*

- **A low-cost method for separation and accurate estimation of ADC noise, aperture jitter, and clock jitter** *Shravan Chaganti (Iowa State U.), Li Xu (Texas Instruments), Degang Chen (Iowa State U.)*
- **Analysis of an efficient on-chip servo-loop technique for reduced-code static linearity test of pipeline ADCs** *Guillaume Renaud, Marc Margalef-Rovira, Manuel Barragan, Salvador Mir (TIMA Laboratory)*
- **Knob Non-Idealities in Learning-Based Post-Production Tuning of Analog/RF ICs: Impact & Remedies** *Yichuan Lu, Georgios Volanis, Kiruba Subramani, Angelos Antonopoulos, Yiorgos Makris (UT Dallas)*

IP Session 9B: Innovative Practices in Asia I: From Quality Perspective
HALL : Pompeian II

Organizers: *Kazumi Hatayama (Gunma U.), Masahiro Ishida (Advantest)*
Moderator: *Masahiro Ishida (Advantest)*

- **Utilizing Switch-Level Test Generation to Improve Accuracy and Efficiency of Cell-Aware Fault Modeling** *Harry H. Chen (Presenter), Simon Y-H. Chen (MediaTek Inc.), Po-Yao Chuang, Cheng-Wen Wu (National Tsing Hua U.)*
- **Soft-Error Rate Evaluation Utilizing Low-Energy Neutron Beam** *Takumi Uezono (Presenter), Tadanobu Toba, Kenichi Shimbo,*

Fumihiko Nagasaki, and Kenji Kawamura (Hitachi)

- **Meeting quality for Automotive Application with IO interfaces** *Salem Abdennadher (Intel Corporation)*

IP Session 9C: DFT and Data for Diagnostics
HALL : Pompeian III

Organizer: Kun Young Chung (Qualcomm)
Moderator: Stefano Di Carlo (Politecnico di Torino)

- **Using Cell Aware Diagnosis to Speed up Yield Ramp for FinFET Technology** *Huaxing Tang (Mentor Graphics)*
- **Integrated Yield Learning with Logic and Memory Volume Diagnostics** *John Kim (Synopsys)*
- **DFM-aware fault model** *Arani Sinha (Intel Corporation)*

09:30AM - 09:50AM | Break

09:50AM - 10:50AM | **Sessions 10**

Session 10A: Test Economics and Test Standards
HALL : Pompeian I

Moderator : *Jennifer Dworak (Southern Methodist U.)*

- **Structured Scan Patterns Retargeting for Dynamic Instruments Access** *Ahmed Ibrahim, Hans Kerkhoff (U. of Twente)*
- **Test-Cost Optimization in a Scan-Compression Architecture Using Support-Vector Regression** *Zipeng Li (Duke U.), Jon Colburn (NVIDIA), Vinod Pagalone (NVIDIA Corporation), Kaushik Narayanun (NVIDIA Corp.), Krishnendu Chakrabarty (Duke U.)*

IP Session 10B: Innovative Practices in Asia II: From Cost Perspective
HALL : Pompeian II

Organizer: *Kazumi Hatayama (Gunma U.), Masahiro Ishida (Advantest)*

Moderator: *Kazumi Hatayama (Gunma U.)*

- **Optical Interconnection Test Method** *Kazuki Shirahata, Tasuku Fujibe, Masahiro Ishida, Daisuke Watanabe, Tomoyuki Itakura, Hidenobu Matsumura, Hiroyuki Mineo, Shin Masuda, Dave Armstrong (Advantest America Inc.)*
- **Signal Generation with Specified Harmonics Suppression Using Only Single Digital Output Pin** *Masayuki Kawabata, Koji Asami (Advantest Corporation), Shohei Shibuya, Tomonori Yanagida, Haruo Kobayashi (Gunma U.)*
- **A Practical and Cost Effective Approach for 2.5D FPGA-Transceiver EMIB Testing** *Lai Pheng Tan, Shen Shen Lee, and Kian Hui Wong (Intel Corporation)*

IP Session 10C: Formal verification practices in industry
HALL : Pompeian III

Organizers: *Huawei Li & Xiaowei Li (ICT, CAS)*
Moderator: *Huawei Li (ICT, CAS)*

- **Formal Verification Techniques and Trends in Industry** *Jun Yuan (Arcas Tech)*
- **Finding Deep RTL Bugs Through Formal Verification** *Xiushan Feng (Samsung)*
- **Formal Verification Applied in GPU Designs** *Rachel Fan (AMD)*

10:50AM - 11:10AM	Break
11:10AM - 12:10PM	**Sessions 11**

Session 11A: Test Quality and Reliability
HALL : Pompeian I

Moderator : *Hans Manhaeve (Ridgetop)*

- **Asymmetric sizing: an effective design approach for SRAM cells against BTI aging** *Xuan Zuo, Sandeep Gupta (University of Southern California)*

- **Comprehensive Investigation of Gate Oxide Short in FinFETs** *Roya Dibaj (Carleton U.), Dhamin Al-Khalili (Dept. of Elec. & Comp. Eng. Royal Military College), Maitham Shams (Dept. of Electronics, Carleton U.)*

- **On-Line Diagnosis and Compensation for Parametric Failures in Linear State Variable Circuits and Systems Using Time-Domain Checksum Observers** *Md Momtaz, Suvadeep Banerjee, Abhijit Chatterjee (Georgia Institute of Technology)*

Session 11B Panel: Would you put your life in the hands of a Google Car?
HALL : Pompeian II

Organizer/Moderator: *LeRoy Winemberg (NXP Semiconductors)*
Panelists

IP Session 11C: SoC Testing
HALL : Pompeian III

Organizer: *Yu Huang (Mentor Graphics)*
Moderator: *Gurgen Harutyunyan (Synopsys)*

- **High Bandwidth DFT Fabric for SoCs** *Jon Easter (Intel Corporation)*

- **Modular Test Practices in High-End FPGA** *Chunsheng Liu (Intel Corporation)*

- **A SoC Test Methodology for DFT Engineering Performance Improvements** *Martin Keim (Mentor Graphics)*

12:10PM - 01:30PM	Lunch
01:30PM - 02:30PM	**Sessions 12**

Session 12A Hot Topic: 5G Test Challenges: A System-level Perspective
HALL : Pompeian I

Presenter: *Adam Smith (LitePoint)*

Session 12B: Embedded Tutorial **I** – Emerging Non-volatile memories: Trends, Technologies and Test Topics
HALL : Pompeian II

Organizer & Moderator: *Mehdi Tahoori (Karlsruhe Institute of Technology)*

- **Security and resiliency of non-volatile memories: How test can help?** *Swaroop Ghosh (Penn State U.)*
- **Spintoronics Memories: Past, Present and Future** *Tomishima Shigeki (Intel Labs)*

Session 12C: Embedded Tutorial **II**: Software Testing: Challenges and Emerging Solutions
HALL : Pompeian III

Organizer: *Dr. Indradeep Ghosh (Fujistu Labs)*
Moderator: *Stefano Di Carlo (Politecnico di Torino)*

- **Software test challenges: techniques and emerging trends** *Indradeep Ghosh (Fujistu Labs)*
- **Embedded Software Testing: Challenges and Approaches** *Yashwant Malaiya (Colorado State U.)*

35th IEEE VLSI TEST SYMPOSIUM - PROGRAM AT A GLANCE

MONDAY, APRIL 10, 2017			
07:30am - 08:30am	**REGISTRATION & BREAKFAST**		
08:30am - 10:30am	**PLENARY SESSION**		
11:10am - 12:10pm	**SESSION 1A:** Analog, Mixed Signal and RF Test I	**SESSION 1B:** Delay and Performance Test	**IP SESSION 1C:** Screening for Layout Sensitive Defects
12:10pm - 01:40pm	LUNCH		
01:40pm - 02:40pm	**SESSION 2A:** ATPG I	**SESSION 2B:** New Topic: Innovation for Emerging Smart IoT Systems	**IP SESSION 2C:** How is industry Simplifying Analog Test?
03:00pm - 04:00pm	**SESSION 3A:** Design for Test, Debug and Reliability	**Special SESSION 3B:** Hot Topic: Intelligent Physical Systems: Test, Diagnosis, Reconfiguration & Correction	**IP SESSION 3C:** Hardware Security
04:20pm - 05:20pm	**IP SESSION 4A:** Variation-tolerant design of circuits/systems	**SESSION 4B:** Early Life Failures	**IP SESSION 4C:** Data Analytics in Test

TUESDAY, APRIL 11, 2017			
07:30am - 08:30am	**REGISTRATION & BREAKFAST**		
08:30am - 09:30am	**SESSION 5A:** Memory Test & Repair	**SESSION 5B:** Reliability Analysis & Yield Optimization	**IP SESSION 5C:** Automotive Test Solutions
09:50am - 10:50am	**SESSION 6A:** ATPG II	**SESSION 6B:** Hot Topic : Physical Attacks: Can Test Save Us?	**IP SESSION 6C:** DFT for Functional Safety
11:10am - 12:10pm	**SESSION 7A:** Hardware Security	**Special SESSION 7B:** Embedded Tutorial: MEMS Testing Challenges, Issues & Solutions	**IP SESSION 7C:** Automotive Quality Assurance

35th IEEE VLSI TEST SYMPOSIUM - PROGRAM AT A GLANCE

12:10pm - 01:30pm	LUNCH		
01:30pm - 03:00pm	**Special SESSION 8A:** Hot Topic: Future Extensions of IEEE Standards	**SESSION 8B:** Designing Versatile Semiconductor Solutions Optimizing Performance, Power & Cost to Market Opportunities	**Special SESSION 8C:** E.J. McCluskey Doctoral Thesis Competition (Presentations & Posters)
03:30pm - 09:30pm	SOCIAL PROGRAM		

WEDNESDAY, APRIL 12, 2017			
07:30am - 08:30am	**REGISTRATION & BREAKFAST**		
08:30am - 09:30am	**SESSION 9A:** Analog, Mixed Signal and RF Testing II	**IP SESSION 9B:** Innovative Practices in Asia I: From Quality Perspective	**IP SESSION 9C:** DFT and Data for Diagnostics
09:50am - 10:50am	**SESSION 10A:** Test Economics and Test Standards	**IP SESSION 10B:** Innovative Practices in Asia II: From Cost Perspective	**IP SESSION 10C:** Formal Verification practices in Industry
11:10am - 12:10pm	**SESSION 11A:** Test Quality & Reliability	**Panel SESSION 11B:** Would you put your life in the hands of a Google Car?	**IP SESSION 11C:** SoC Testing
12:10pm - 01:30pm	LUNCH		
01:30pm - 02:30pm	**SESSION 12A:** Hot Topic: 5G Test Challenges: A System-level Perspective	**SESSION 12B:** Embedded Tutorial I: Emerging Non-volatile memories: Trends, Technologies and Test Topics	**SESSION 12C:** Embedded Tutorial II: Software Testing: Challenges and Emerging Solutions

This year our social event will start with a short (0.5 mile) walk from the conference venue to the famous Madame Tussauds Las Vegas Museum, where we will have a late-afternoon (4pm-6pm) reception in a private room. Besides access to all exhibits of the museum, we will also have the opportunity to mingle and enjoy drinks in a relaxed atmosphere.

Madame Tussauds Las Vegas is a wax museum located in the Las Vegas Strip at The Venetian Las Vegas casino resort in Paradise, Nevada. The attraction opened in 1999, becoming the first Madame Tussauds venue to open in the United States. It features over 100 wax figures of famous celebrities, film and TV characters, athletes, musicians and Marvel superheroes, as well a 4D movie theatre.

We will then take a longer (1.5m) stroll on the Las Vegas Strip, from Madam Tussauds Las Vegas Museum to the MGM Grand Las Vegas Hotel and Casino, where we will enjoy the famous show KÀ by Cirque du Soleil. For those who do not wish to walk, the Las Vegas Monorail can be picked up from Harrah's/The Linq station to the MGM Grand Station ($5 single-ride ticket).

KÀ tells the epic tale of twins on a perilous journey to fulfill their shared destiny. A masterpiece in storytelling, this ultra lavish production features mind-bending acrobatics, fierce martial arts, blazing pyrotechnics and jaw-dropping aerial adventures. After the show, attendees may either walk back to the Caesars Palace or take the Las Vegas Monorail back to the Flamingo / Caesars Palace Station.

Precise instructions and directions will be distributed at the symposium.

Organizers: *M. Portolan (TIMA Laboratory) & N. Karimi (U. of Maryland Baltimore County)*
Moderator: *N. Karimi (U. of Maryland Baltimore County)*
Named after the late Prof. E.J. McCluskey, a key contributor to the field of test technology, the 2017 TTTC's Doctoral Thesis Award serves the purpose to i) promote the most impactful doctoral student work, ii) provide the students with the exposure to the community and the prospective employers, and iii) support interaction between academia and industry in the field of test technology. TTTC's E.J. McCluskey Best Doctoral Thesis Award will be given to the winning student of the doctoral student contest and his or her advisor. The award consists of a certificate, an honorarium and an invitation to submit a paper on the presented work to the IEEE Design & Test magazine.

The contest is held in two stages: semi-finals and finals: In 2017, semifinals will be held at the IEEE VLSI Test Symposium (VTS), the IEEE European Test Symposium (ETS), the IEEE Latin American Test Symposium (LATS) and the Asian Test Symposium (ATS). The semi-final winners will compete against each other in the finals, held at the International Test Conference (ITC) 2017.

VTS 2017 Semifinalists:
1. Robert Karam (U. of Florida), **Advisor:** Swarup Bhunia
Thesis title: Energy-Efficient and Secure Reconfigurable Computing Architecture

2. Yu Liu (The U. of Texas at Dallas), **Advisor:** Yiorgos Makris
Thesis title: Hardware Trojans in Wireless Cryptographic ICs

3. Cheng Xue (Carnegie Mellon U.), **Advisor:** R.D. (Shawn) Blanton
Thesis title: Optimizing IC Testing for Diagnosability, Effectiveness and Efficiency

4. Yuming Zhuang (Iowa State U.), **Advisor:** Degang Chen
Thesis title: Accurate and Robust Spectral Testing with Relaxed Instrumentation Requirements

With generous support from the National Science Foundation, 12 US-based Masters or early-Ph.D. students who are neither authors nor presenters have been invited to participate at IEEE VTS'17. The objective of this program, which covers conference registration, lodging and partial travel costs, is to introduce these students to leaders from industry, academia, and government, and expose them to a series of organized and impromptu discussions regarding career trajectories and opportunities in the area of VLSI testing. The following applicants have been selected:

- Xiaoan Ding, U Chicago (Faculty Advisor: Yanjing Li)
- Madhuja Ghosh, NC State U (Faculty Advisor: Brian A. Floyd)
- Yi He, U Chicago (Faculty Advisor: Yanjing Li)
- Hui Jiang, Southern Methodist U (Faculty Advisor: Jennifer Dworak)
- Christiana Kapatsori, UT Dallas (Faculty Advisor: Yiorgos Makris)
- Prathyusha Kondlapudi, San Diego State U (Faculty Advisor: Ke Huang)
- Danqing Liu, UT Dallas (Faculty Advisor: Jeyavijayan Rajendran)
- Vinay C Patil, U Mass Amherst (Faculty Advisor: Sandip Kundu)
- Ashiq Adnan Sakib, North Dakota State University (Faculty Advisor: Scott C. Smith)
- Chuanhe (Jay) Shan, UC Santa Barbara (Faculty Advisor: Li-C Wang)
- Dimitrios Tychalas, New York U (Faculty Advisor: Michail Maniatakos)
- Naixing Wang, Purdue U (Faculty Advisor: Irith Pomeranz)

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35th IEEE VLSI Test Symposium (VTS 2017)
FRINGE MEETINGS

A number of TTTC professional groups interested in test will hold their meetings at VTS 2017. At press time, the following meetings were scheduled. These meetings are for members. If you would like to attend, please contact the person listed at the e-mail address given. Unless otherwise specified, all fringe meetings will be held in the Pompeian IV room.

Monday April 10th	
*12:10 pm - 1:40 pm	**Test Week Workshop Coordination** Yervant Zorian (zorian@synopsys.com)
02:15 pm - 03:00 pm	**TTTC Executive Committee** Chen-Huan Chiang (chenhuan.chiang@intel.com)
05:00 pm - 06:00 pm	**ITC Topic Coordinators Meeting** Peter Maxwell (Peter.Maxwell@onsemi.com)
05:00 pm - 06:00 pm	**TTTC Senior Leadership Board** Yervant Zorian (zorian@synopsys.com)
**06:00 pm - 08:00 pm	**IEEE VTS Technical Program Committee** Srivaths Ravi (srivaths.ravi@ti.com) Amit Majumdar (amit.majumdar@xilinx.com)

Tuesday April 11th	
09:00 am - 10:00 am	**TTTC Technical Meetings Review Committee** Michele Portolan (michele.portolan@imag.fr)
11:00 am - 12:00 pm	**Session 7D: Student Poster Presentations for E. J. McCluskey TTTC Doctoral Thesis Competition** Naghmeh Karimi (naghmeh.karimi@umbc.edu)
*12:10 pm - 01:30 pm	**TTTC Standards Group** Adam Cron (Adam.Cron@synopsys.com)

Wednesday April 12th	
10:00 am - 11:00 am	**IEEE VTS Organizing Committee** Yiorgos Makris (yiorgos.makris@utdallas.edu)
01:30 pm - 02:30 pm	**Session 12D: Town-Hall Meeting for NSF Student Program Participants** Naghmeh Karimi (naghmeh.karimi@umbc.edu)

**Meeting During Lunch Break*
***Meeting During Dinner in Verona/Turin/Trevi (By invitation only).*

NOTES

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