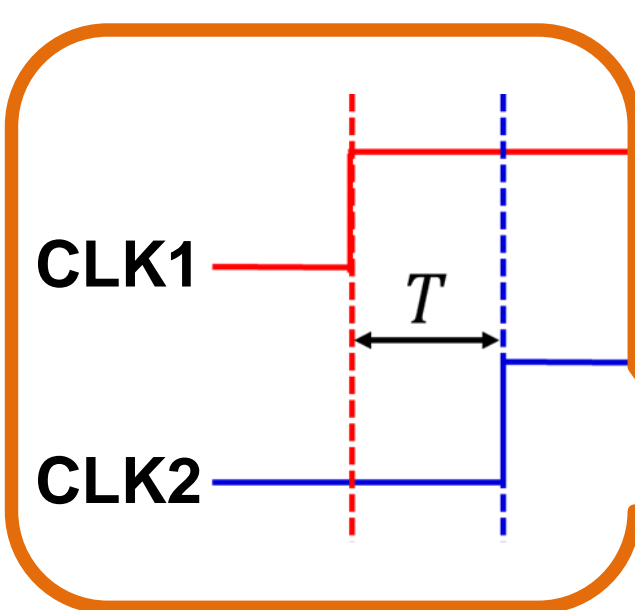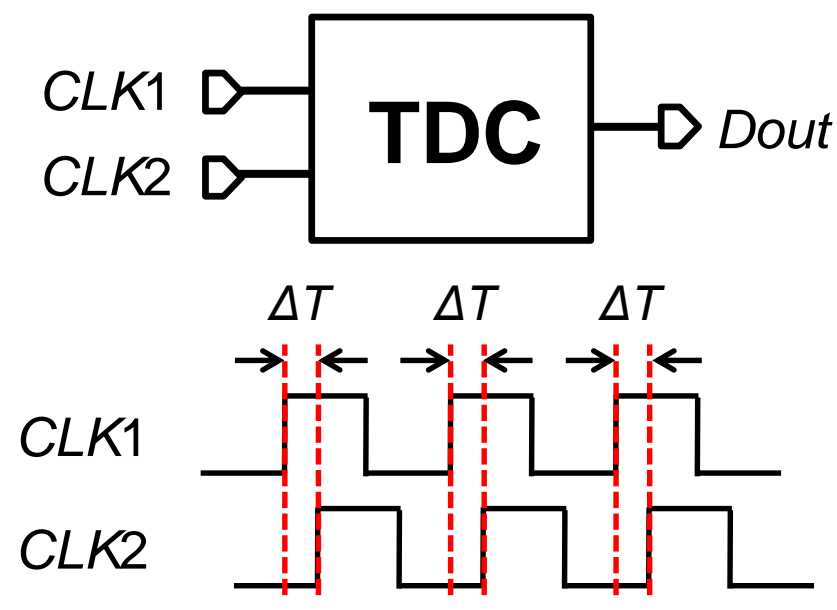# Self-Calibration and Trigger Circuit for Two-Step SAR TDC

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Introduction

Research Background

Time-to-Digital Converter (TDC)
measures the time and provides digital output

CLK1
CLK2
TDC
Dout

ΔT ΔT ΔT
CLK1
CLK2

· Can it be measured **more accurately**?
· How can we generate
repetitive signals of clk 1 and clk 2 with **one shot**?

Research Objective

Development of

highly - linear, fine time-resolution TDC

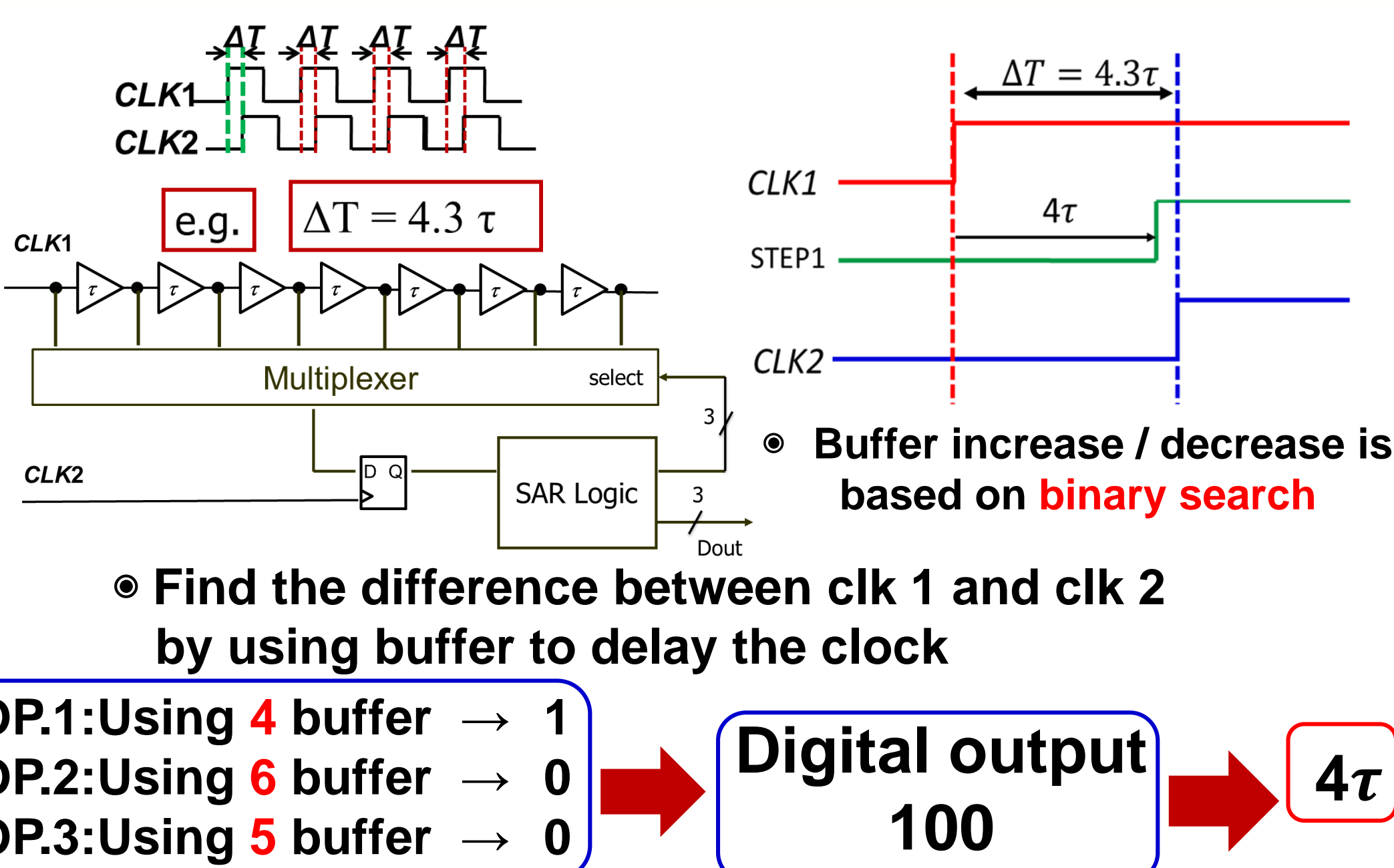for high-speed digital I/O interface

 timing measurement

Δt
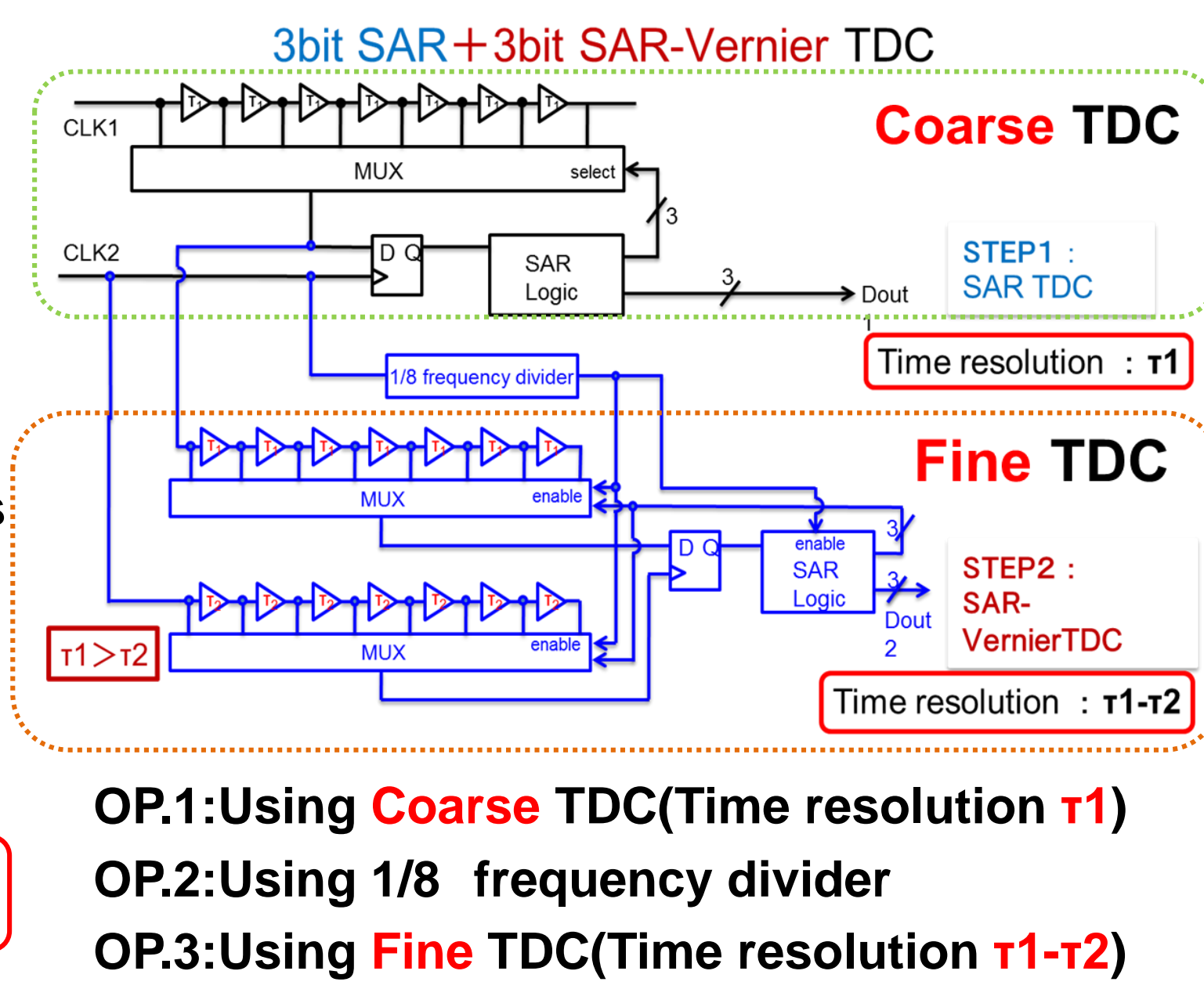START
STOP
TDC7200
TIME-TO-DIGITAL CONVERTER
TEXAS INSTRUMENTS
1010...

Our Innovation

Development of 2 key technologies

for time measurement

[I] Two-Step SAR TDC
Fine time resolution

[II] Self-Calibration
Linear TDC

[III] Trigger Circuit
One-shot timing measurement

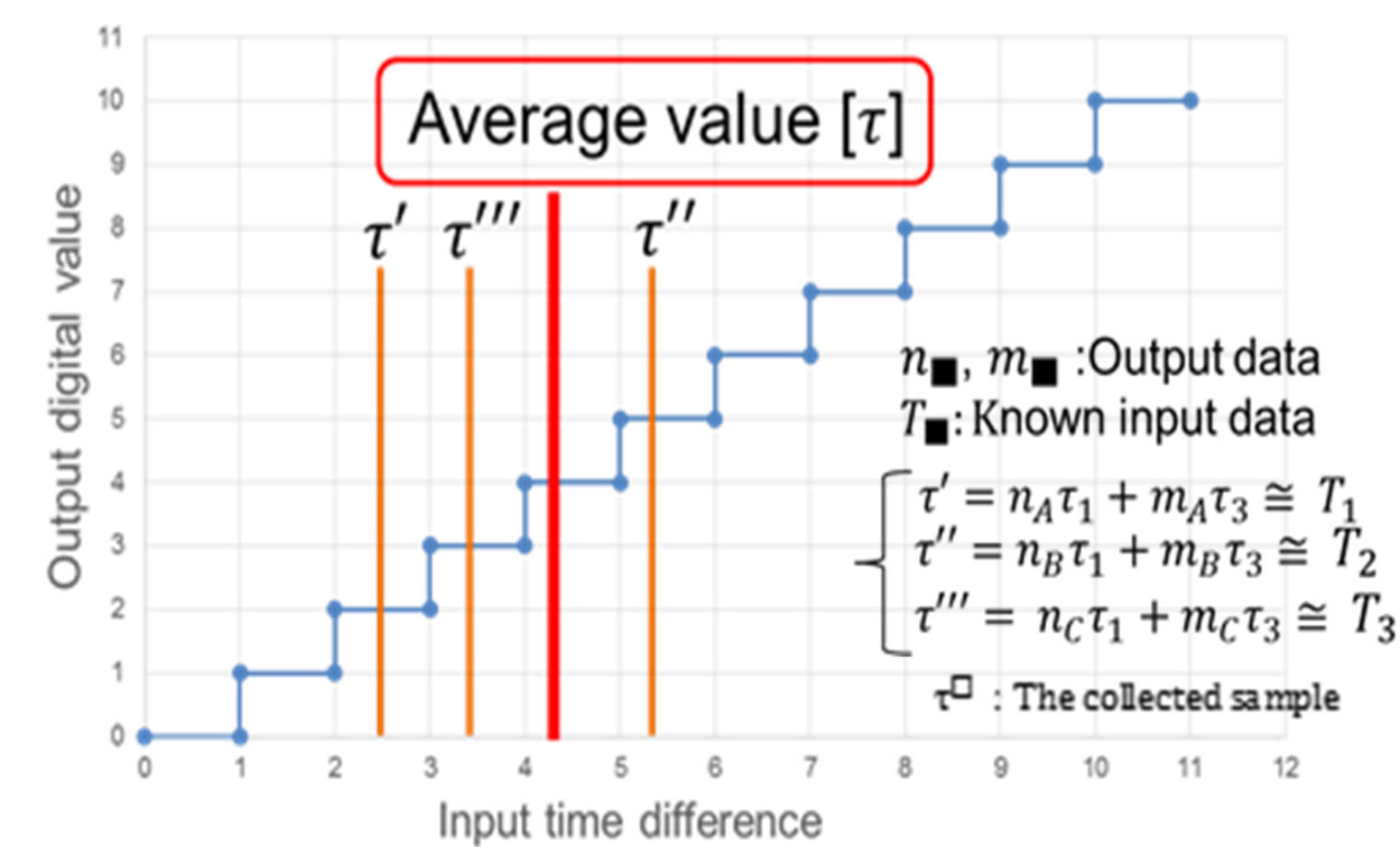## Fine time resolution

[I] TDC operation

ΔT ΔT ΔT ΔT
CLK1
CLK2

e.g. $\Delta T = 4.3 \tau$

CLK1
Multiplexer select
CLK2
D Q
SAR Logic
3
3
Dout

◎ **Find the difference between clk 1 and clk 2**
by using buffer to delay the clock

OP.1:Using **4** buffer → 1
OP.2:Using **6** buffer → 0
OP.3:Using **5** buffer → 0

Digital output 100 → 4τ

$\Delta T = 4.3\tau$
CLK1
4τ
STEP1
CLK2

◎ **Buffer increase / decrease is based on binary search**

Two-Step SAR TDC operation
(SAR TDC+Vernier type TDC)

3bit SAR＋3bit SAR-Vernier TDC

CLK1
MUX select
CLK2
D Q
SAR Logic
3
Dout
Coarse TDC
STEP1 : SAR TDC
Time resolution : τ1

1/8 frequency divider

MUX enable
MUX enable
$\tau 1 > \tau 2$
MUX enable
enable
D Q
SAR Logic
3
Dout 2
Fine TDC
STEP2 : SAR-VernierTDC
Time resolution : τ1-τ2

OP.1:Using **Coarse** TDC(Time resolution τ1)
OP.2:Using 1/8 frequency divider
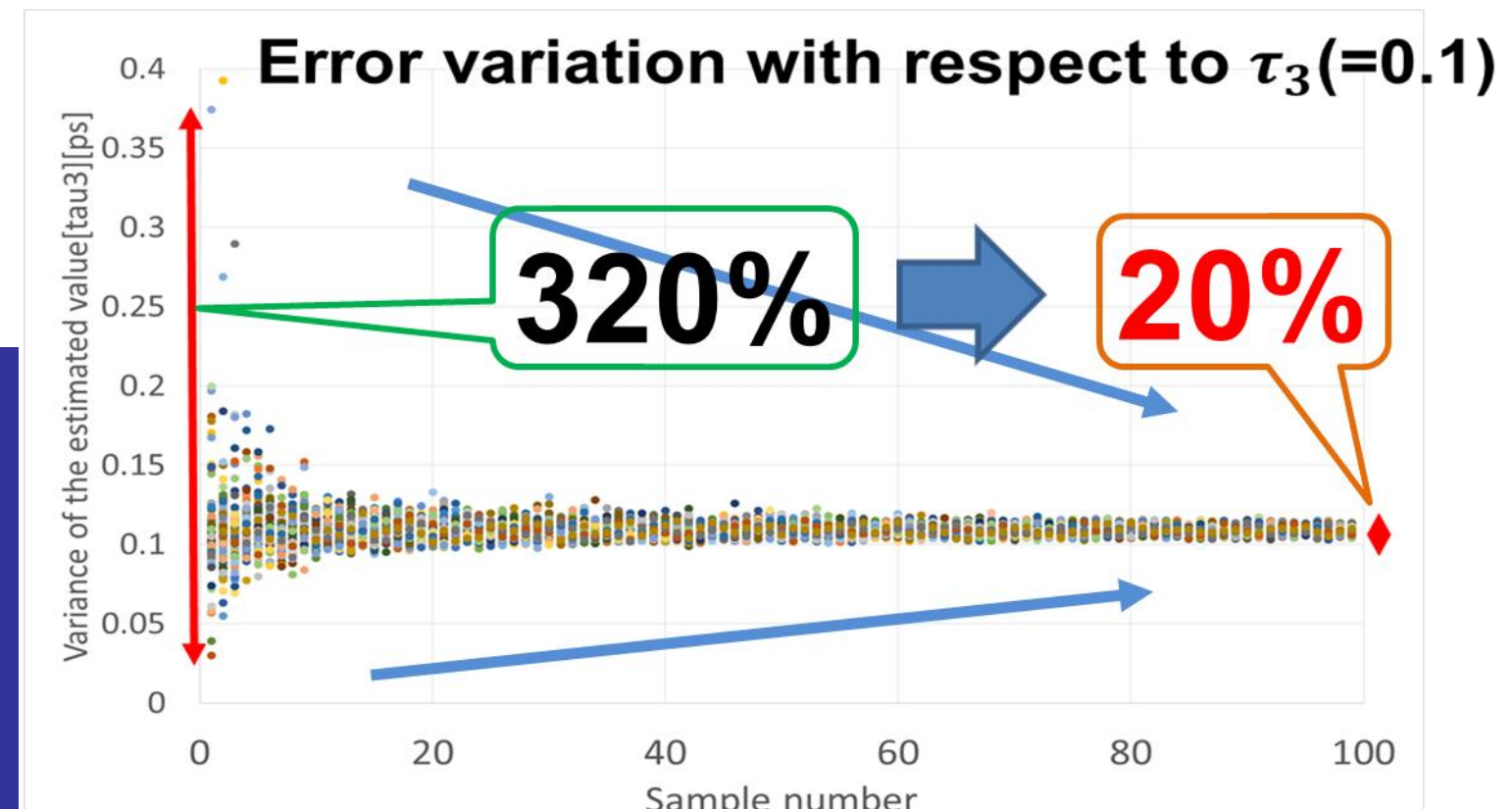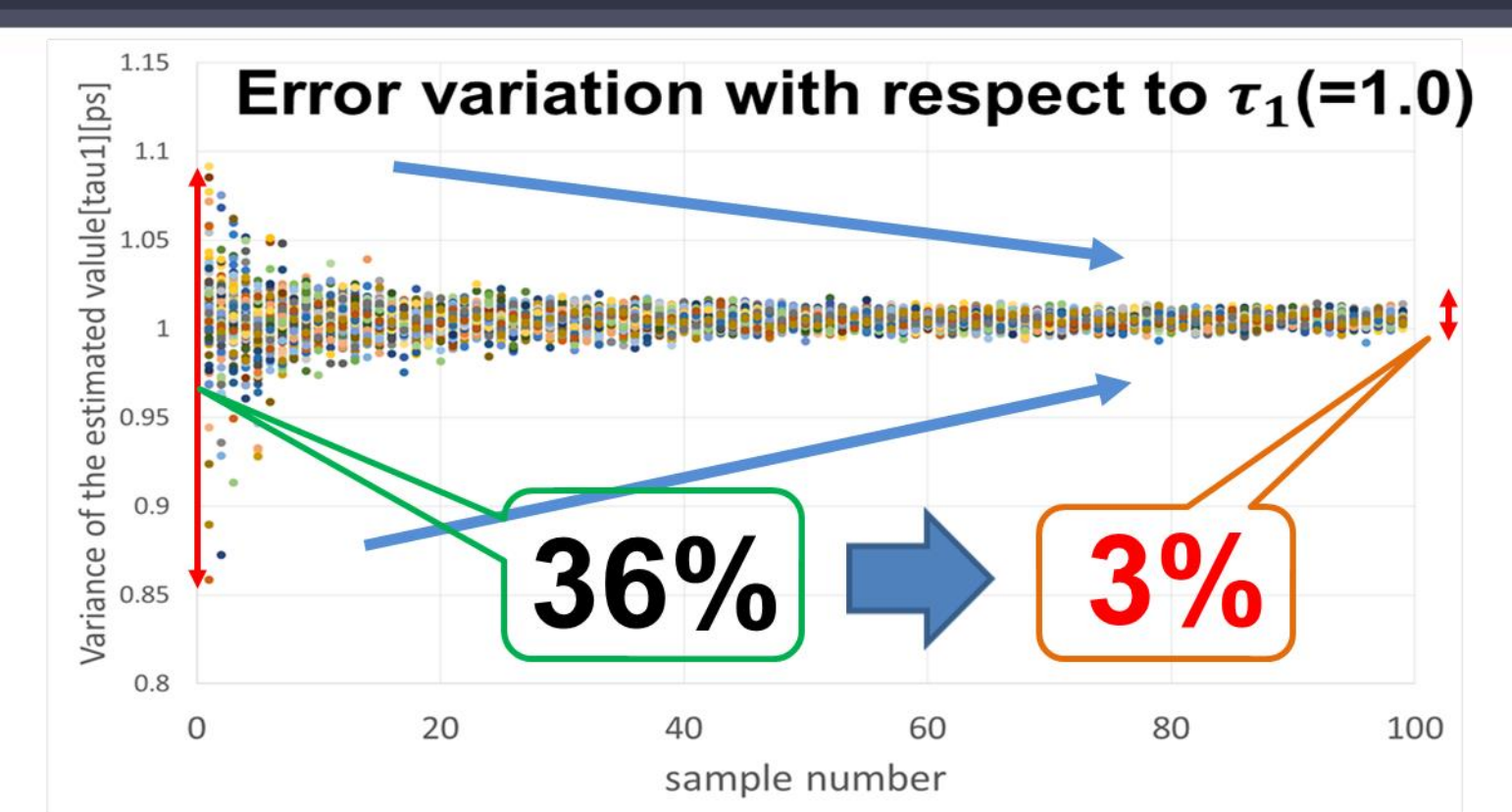OP.3:Using **Fine** TDC(Time resolution τ1-τ2)

Linear TDC

[II] Calibration algorithm
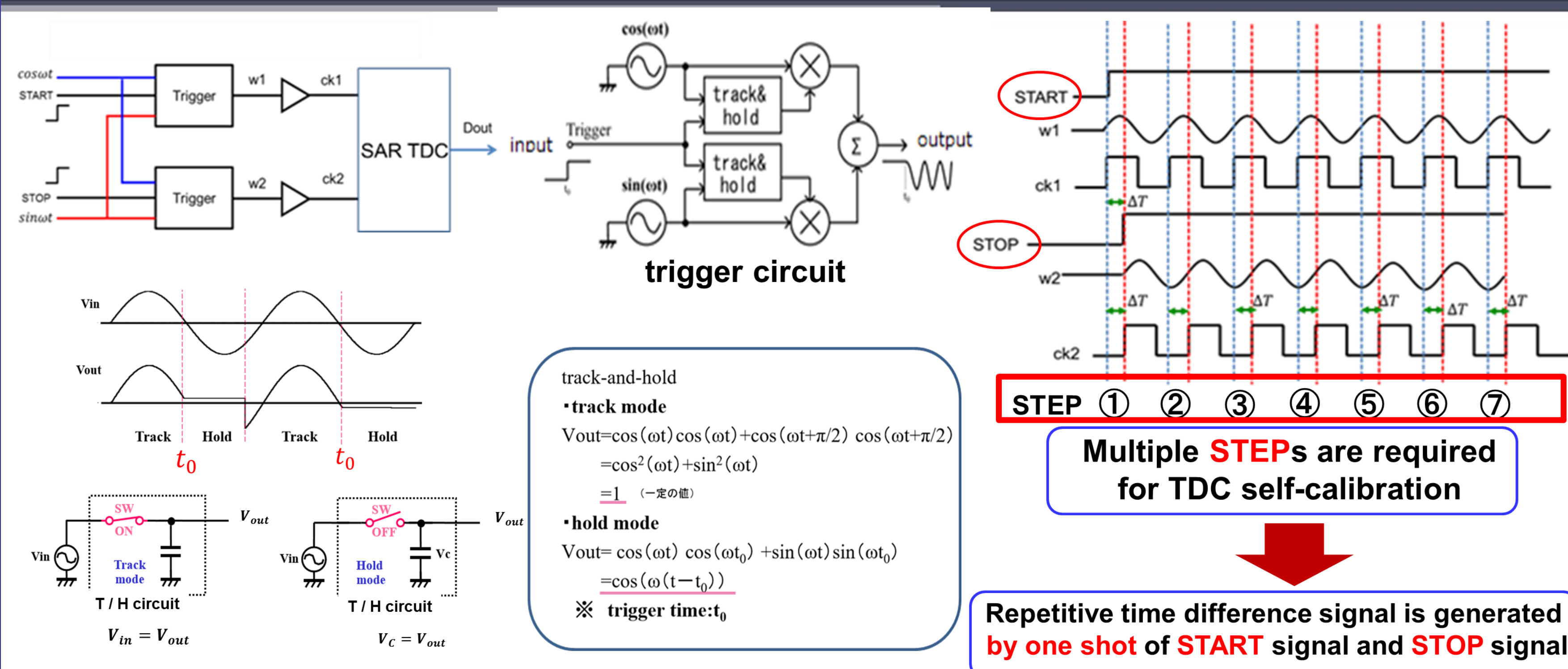
Explanation of the self-calibration algorithm

Average value [τ]

τ' τ''' τ''

Output digital value
Input time difference

$n_\blacksquare$, $m_\blacksquare$:Output data
$T_\blacksquare$: Known input data
$\tau' = n_A\tau_1 + m_A\tau_3 \cong T_1$
$\tau'' = n_B\tau_1 + m_B\tau_3 \cong T_2$
$\tau''' = n_C\tau_1 + m_C\tau_3 \cong T_3$
$\tau^\square$: The collected sample

·**Estimate the delay value of the actual delay element by increasing the number of samples**

Linear TDC

Simulation Result : Measurement error of estimated value

Measurement error of estimated value [τ_1]
· When the number of samples is "2"
About 3.7%
· When the number of samples is "100"
About 1.2%

Error ratio of the sample [%]
Sample number

Measurement error of estimated value [τ_3]
· When the number of samples is "2"
About 19.5%
· When the number of samples is "100"
About 9.0%

Error raito of the sample [%]
Sample number

Error variation with respect to τ_1(=1.0)
Variance of the estimated value[tau1][ps]
sample number
36% → **3%**

Error variation with respect to τ_3(=0.1)
Variance of the estimated value[tau3][ps]
Sample number
320% → **20%**

·**Increased reliability** by
increasing the number of samples
Sufficient reliability!

One-shot timing measurement

[III] Self-configuring circuit using trigger circuit

cosωt
START
Trigger
w1 ck1
STOP
Trigger
w2 ck2
sinωt
SAR TDC
Dout
input

cos(ωt)
track& hold
sin(ωt)
track& hold
Σ
output

trigger circuit

START
w1
ck1
ΔT
STOP
w2
ck2
ΔT ΔT ΔT ΔT ΔT

STEP ① ② ③ ④ ⑤ ⑥ ⑦

Multiple STEPs are required for TDC self-calibration

Vin
Vout
Track Hold Track Hold
t_0 t_0

Track mode
SW ON
Vin Vout
Track mode
T / H circuit
$V_{in} = V_{out}$

Hold mode
SW OFF
Vin Vout Vc
Hold mode
T / H circuit
$V_c = V_{out}$

track-and-hold
·**track mode**
Vout=cos(ωt) cos(ωt)＋cos(ωt+π/2) cos(ωt+π/2)
=cos²(ωt)+sin²(ωt)
=1 (一定の値)
·**hold mode**
Vout= cos(ωt) cos(ωt₀) +sin(ωt) sin(ωt₀)
=cos(ω(t−t₀))
※ trigger time:t_0

Repetitive time difference signal is generated by one shot of START signal and STOP signal

References

[1] Y. Arai, T. Baba, "A CMOS Time to Digital Converter VLSI for High-Energy Physics", IEEE Symposium on VLSI Circuits (1988).

[2] R. Jiang, C. Li, M. Yang, H. Kobayashi, et al., "Successive Approximation Time-to-Digital Converter with Vernier-level Resolution", IEEE IMSTW, Catalunya, Spain（July 2016).

[3] Tektronics, Automatic RF Techniques Group 56th Measurement Conference - Metrology and Test for RF Telecommunications, Boulder, Colorado (Dec. 2000).