Self-Calibration and Trigger Circuit for Two-Step SAR TDC

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Introduction

Research Background

Time-to-Digital Converter (TDC) measures the time and provides digital output

- Can it be measured more accurately?
- How can we generate repetitive signals of clk 1 and clk 2 with one shot?

Research Objective

Development of highly-linear, fine time-resolution TDC for high-speed digital I/O interface timing measurement

Our Innovation

Development of 2 key technologies for time measurement

[ I ] Two-Step SAR TDC
- Fine time resolution

[ II ] Self-Calibration
- Linear TDC

[ III ] Trigger Circuit
- One-shot timing measurement

Fine time resolution

[ I ] TDC operation

Two-Step SAR TDC operation (SAR TDC + Vernier type TDC)

[ II ] Calibration algorithm

Linear TDC

Optimization of the self-calibration algorithm

- Estimate the delay value of the actual delay element by increasing the number of samples

Simulation Result: Measurement error of estimated value

- When the number of samples is "2"
  - About 3.7%
- When the number of samples is "100"
  - About 1.2%

Error variation with respect to $\tau_1$ (1.0)

- About 19.5%
- About 9.0%

36% → 3%

Sufficient reliability!

References

